

# A SOFT-SWITCHED PWM INTERLEAVED BOOST-FLYBACK CONVERTER WITH POWER FACTOR CORRECTION

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**Abstract** – This paper proposes a soft switching interleaved Boost-Flyback converter employed as a preregulator stage providing power factor correction. The use of a soft commutation cell allows the main switches to be turned on and off under null current and null voltage conditions, respectively. Interleaving techniques imply the overall reduction of the Boost inductor size and also the minimization of the switching losses without increasing voltage and current stresses. This topology has the advantages of the Flyback converter, as auxiliary power supplies are not necessary. A theoretical analysis, including the description of the operating stages and relevant expressions is developed. Additionally, simulation and experimental results are presented.

**Keywords** — Power Factor Correction, Interleaved Converters.

## I. INTRODUCTION

The intensive use of electronic converters, mainly in industrial and residential applications, e.g., telecommunications, control and motor drives, instruments of measurements and switched-mode power supplies employed in personal computers has significantly increased the injection of harmonic currents in the power grid. Recently, there has been great interest on the reduction the harmonic content of the input current and also power factor correction (PFC). However, at high switching frequencies, switching losses and EMI levels become significant and must be considered in the design of converters. The losses during turning on and turning off are also increased at high frequencies, although soft-switching techniques are supposed to overcome this limitation. A prominent solution can be found on the zero-voltage transition PFC (ZVT-PFC) [1] converters and on the zero-current transition PFC (ZCT-PFC) converters [2]. The work described in [4] presents eight Boost topologies where switching cells operate in

discontinuous conduction mode (DCM) at relatively low frequency (25kHz per cell), and [5] presents a PFC interleaved Boost converter operating in continuous-inductor-current mode (CICM).

However, the configurations mentioned above develop considerable commutation and conduction losses, demanding complex control circuitry and implying reduced reliability of the converters.

The Boost PFC converter has been intensively used due to the dc voltage gain characteristics and reduced inductor volume and weight [7,8], since it is adequate as a preregulator stage. The work presented in [9] employs two switches that perform the same operation, what allows the choice of a greater switching frequency and also a smaller filter capacitor than that in [10]. In this case, the use of interleaving techniques results in even smaller filter inductors and filter capacitors.

Interleaving techniques consist in the interconnection of multiple switching cells where the operating frequency is the same, but the gating signals are sequentially phased over equal fractions of the switching period [3]. The converter described in [11] employs this strategy with power factor correction IC UC3854 [13], although the switching frequency is 100kHz. This paper presents two switching cells operating at 100kHz each i.e. the filter inductors and filter capacitors are designed for an operating frequency of 200kHz. It means that the sizes of the filter elements are substantially reduced in comparison with the case studied in [11].

An optimum alternative that leads to high power levels at high switching frequencies lies in the use of the nondissipative snubber described in [7] and [12]. However, such configuration employs two voltage sources, while the one proposed in this paper uses an interleaved Flyback converter to replace them. Additionally, the resonance does not demand two diodes as in [7] and [12], but a single inductor and a single diode instead. Within this context, this work presents two significant contributions i.e. the reduction of the size and the volume of the filter elements and the absence of auxiliary power supplies [14].

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## II. OPERATING PRINCIPLES OF THE INTERLEAVED BOOST-FLYBACK CONVERTER WITH THE NONDISSIPATIVE SNUBBER

In order to study the proposed topology, the operation of the converter shown in Fig. 1 is divided in six topological modes, according to Fig. 2. One must remember that operation of a single cell is considered due to the inherent analogy between the cells. The main waveforms are shown in Fig. 3.

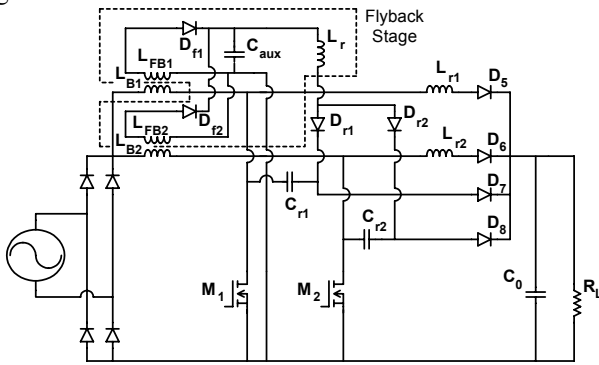


Fig. 1. Interleaved Boost-Flyback converter with power factor correction.

**First Stage ( $t_0, t_1$ ):** This stage begins at instant  $t_0$ , when switch  $M_1$  is turned on in ZCS mode, due to  $L_{r1}$  that demagnetizes through loop formed by  $C_0, D_6$  and  $M_1$ . The

Flyback stage maintains the resonance between  $C_{r1}$  and  $L_{r1}$  causing diode  $D_5$  to be forward biased. This stage finishes when the voltage across capacitor  $C_{r1}$  equals the output voltage.

**Second Stage ( $t_1, t_2$ ):** It begins when the voltage across capacitor  $C_{r1}$  is clamped to  $V_0$ , and the resonant inductor  $L_{r1}$  demagnetizes linearly through the loop formed by  $D_{r1}, D_7, C_0$  and Flyback stage. This stage is responsible for the PWM characteristics of the converter, and it finishes when switch  $M_1$  is turned off.

**Third Stage ( $t_2, t_3$ ):** This stage begins when switch  $M_1$  is turned off in ZVS mode. Resonant capacitor  $C_{r1}$  discharges linearly the stored energy through the loop formed by  $L_{b1}, C_0$  and  $D_7$ .

**Fourth Stage ( $t_3, t_4$ ):** Inductor  $L_{r1}$  oscillates with  $C_{r1}, D_5$  and  $D_7$  until it equals the load current. At the same instant, there is a resonance involving capacitors  $C_{r1}$  and  $C_{r2}$ , and inductor  $L_{r1}$ . Capacitor  $C_{r1}$  is charged negatively, while capacitor  $C_{r2}$  is fully discharged, as this stage finishes and switch  $M_2$  is turned on in ZCS mode.

**Fifth Stage ( $t_4, t_5$ ):** Capacitor  $C_{r1}$  oscillates with inductors  $L_{r1}$  and  $L_{r2}$  through the loop formed by  $D_5, C_0$  and Flyback stage until the current through  $L_{b1}$  equals the load current.

**Sixth Stage ( $t_5, t_6$ ):** During this stage, the voltage across resonant capacitor  $C_{r1}$  is clamped to the voltage assumed at the end of the previous resonant stage, until a new switching cycle begins.

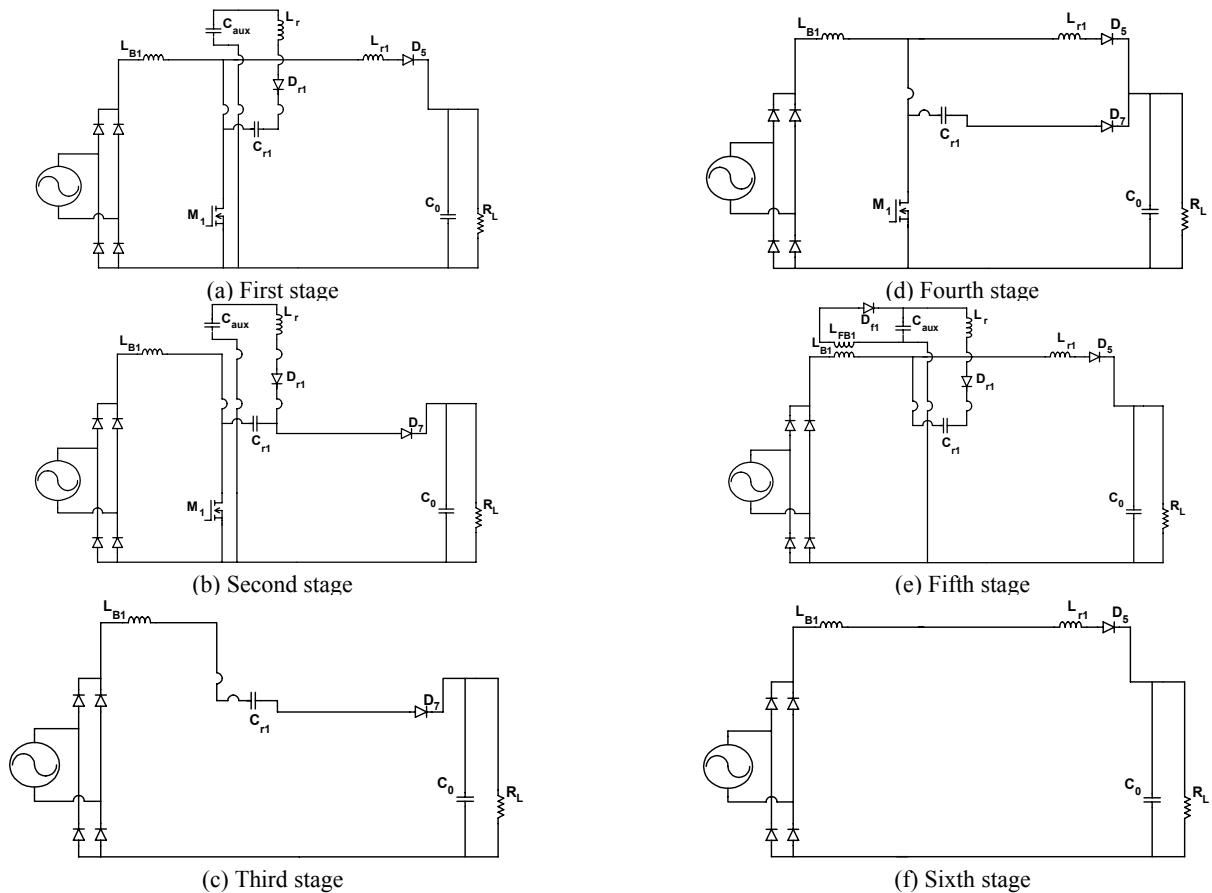


Fig. 2. Equivalent circuits describing the operation of the proposed converter.

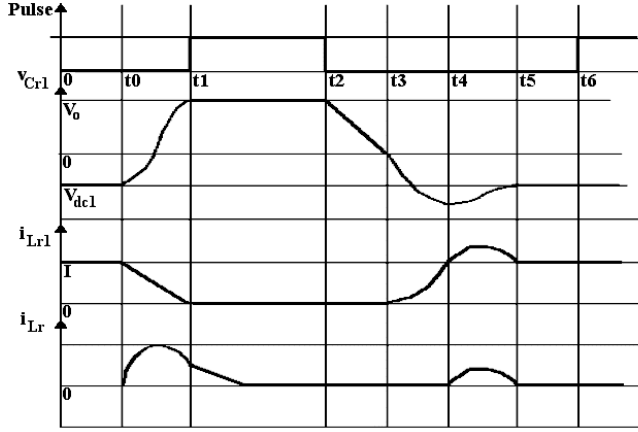


Fig. 3. Main theoretical waveforms.

### III. DESIGN PROCEDURE

The active components and resonant elements can be determined according to the expressions presented below. Further details on this procedure can be found in [15].

$$L_b = \frac{25000}{f_s P_{in}} \quad (1)$$

$$\frac{f_s}{f_0} = 0.08 \quad (2)$$

$$2\pi f_0 = \frac{1}{\sqrt{L_r C_r}} \quad (3)$$

$$\frac{L_r}{C_r} = \left( \frac{\alpha V_{Caux}}{I_0} \right)^2 \quad (4)$$

$$C_0 = \frac{P_0}{240\pi V_0 V_{Caux}} \quad (5)$$

The switches can be specified according to expressions (6) and (7).

$$I_{M1(avg)} = \frac{(K_f K_B)^2}{2D} + K_f K_B \left[ \frac{K_f}{D} + \frac{2K}{\alpha} + \frac{K_B(K-1)}{\alpha} \right] + \quad (6)$$

$$K_f \left( \frac{K_f}{2D} + \frac{K}{\alpha} \right) \cos^{-1} K2 + K_f \left[ \frac{2K-1}{\alpha} + \frac{\sqrt{2}}{2} \right]$$

$$I_{M1(rms)} = \frac{K_f K_D^2 (\cos^{-1} K2)^3}{3} +$$

$$2K_f K_D K_E \left[ (1-K2) \cos^{-1} K2 + \sqrt{1-K2^2} \right] + \quad (7)$$

$$K_f K_B K_M + \frac{K_f K_E^2}{2} \left[ \cos^{-1} K2 - k2\sqrt{1-k2^2} \right] +$$

$$\frac{(K_f K_B)^3}{3D^2} + \frac{(K_f K_B)^2 K_M}{D}$$

The diodes can be specified according to expressions (8) and (9).

$$I_{D(avg)} = 1 - K_f \left[ \frac{K}{\alpha} \left( (\cos^{-1} K2)^2 + 1 \right) + 2K1 + K_B - \frac{1}{\sqrt{2}} \right] \quad (8)$$

$$I_{D(rms)} = 1 + K_f \left\{ \frac{2K (\cos^{-1} K2)^2 [2K \cos^{-1} K1] + \frac{3\pi + 8}{4\sqrt{2}} + K1 \left( \pi \sqrt{\frac{2}{3}} - 4 \right)}{-K_B - \frac{K}{\alpha}} \right\} \quad (9)$$

The resonant diodes can be specified according to expressions (10) and (11).

$$I_{Dr(avg)} = \frac{K_f}{\alpha} \left[ K1 + K + \frac{K_B^2 (3-K)}{2} \right] \quad (10)$$

$$I_{Dr(rms)} = \frac{K_f}{\alpha^2} \left\{ \frac{(1+K1)^2}{2} \left[ \cos^{-1} K2 - K2\sqrt{1-K2^2} \right] + K_B^3 \left[ \frac{(K-1)^2}{3} - (K-1) + 1 \right] \right\} \quad (11)$$

Where:

$L_b$  – boost inductor;

$D$  – duty cycle;

$f_s$  – switching frequency;

$f_0$  – resonant frequency;

$C_r$  – resonant capacitor;

$L_r$  – resonant inductor;

$I_0$  – output current;

$P_0$  – output power;

$P_{in}$  – input power;

$V_0$  – output voltage;

$K$  – constant;

$\omega_{01}$  – resonance frequency;

$V_0$  – output voltage;

$V_{Caux}$  – voltage provided by the Flyback stage;

$\alpha$  – gain.

$$K_C = \pi \left( \frac{3}{2\sqrt{2}} + \sqrt{\frac{3}{2}} \right) \quad (12)$$

$$K_f = \frac{f_s}{\omega_{01}} \quad (13)$$

$$K_G = K_f \left[ \frac{K}{\alpha} + \pi K_C \right] \quad (14)$$

$$K_D = \frac{K_f}{D} + \frac{2K}{\alpha} \quad (15)$$

$$K_E = \frac{1+K1}{\alpha} \quad (16)$$

$$K_M = K_D \cos^{-1} K2 + \frac{K_B (K-1)}{\alpha} \quad (17)$$

The following analysis is based on the following assumptions:

- (i) All switches and diodes are ideal;
- (ii) Input voltage and output voltage are ripple-free;
- (iii) Inductors and capacitors are lossless and the output current is assumed continuous during the operation.

Initially, the transfer function between the input voltage and output voltages can be determined as:

$$G = 1 + \frac{DT_s}{(1-D)T_s - \left[ \frac{K}{\alpha\omega_{01}} + \frac{3\pi}{2\sqrt{2}\omega_{01}} + \sqrt{\frac{3}{2}} \frac{\pi}{\omega_{01}} \right]} \quad (18)$$

Where:

$T_s$  – switching period;

$DT_s$  – switching frequency.

$$K = \frac{V_0}{V_{Caux}} \quad (19)$$

$$\omega_{01} = \frac{1}{\sqrt{C_{r1}L_{r1}}} \quad (20)$$

$$D = \frac{\Delta T}{T_s} \quad (21)$$

$$\Delta T = t_{i+1} - t_i \quad (22)$$

From (18), one can see that the static gain depends on the ratio between the output voltage and the Flyback voltage. The duty cycle behavior as a function of the normalized current is presented in Fig.4, where the static gain assumes several values.

#### IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to illustrate the operation of the converter, some simulation and experimental tests were carried out employing the parameters set shown in Table I.

Simulation and experimental results are shown in Figs. 5 and 6, respectively. Fig 5 (a) and Fig 6 (a) evidence power factor correction when the input voltage is 220V<sub>rms</sub>, as the displacement power factor is 0.998 and 0.995, respectively. Fig 5 (b) and Fig 6 (b) present the waveforms referring to the resonant tank elements. Fig 5 (c) and Fig 6 (c) illustrate soft switching, where one can see that switch  $M_1$  is turned on and off under null current and null voltage conditions, respectively. Finally, Fig 5 (d) and Fig 6 (d) represent the current through Boost inductors  $Lb1$  and  $Lb2$ .

Fig.7 depicts the harmonic spectrum of the input current and input voltage.

Fig.8 shows the efficiency curve of the Boost-Flyback converter. It can be seen that the efficiency at rated load is quite high i.e. 98%.The graph also indicates that the use of the nondissipative snubber is prominent in front of the behavior of the hard-switched structure.

**Table I – Parameters set used in the tests.**

Parameter	Value
Boost inductors	$Lb1=Lb2=600\mu\text{H}$
Flyback inductor	$L_r=5\mu\text{H}$
Output capacitor	$C_0=330\mu\text{F}$
Auxiliary capacitor	$C_{aux}=220\mu\text{F}$
All diodes	MUR1560
Switches $M_1$ and $M_2$	IRFP460
Switching frequency	$f_s=100\text{kHz}$
AC input voltage	$V_i=80\text{-}240\text{V}_{\text{rms}}$
DC Output voltage	$V_0=400\text{V}_{\text{dc}}$
Output power	$P_0=2000\text{W}$
Output current	$I_0=5\text{A}$
Resonant inductors	$L_{r1}=L_{r2}=5\mu\text{H}$
Resonant capacitors	$C_{r1}=C_{r2}=8.2\text{nF}$

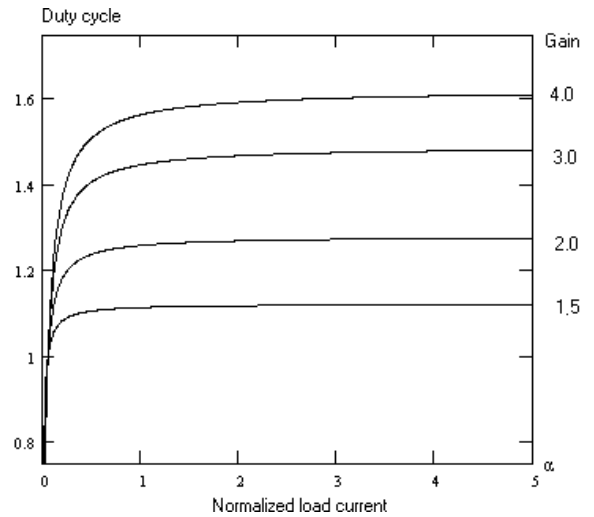
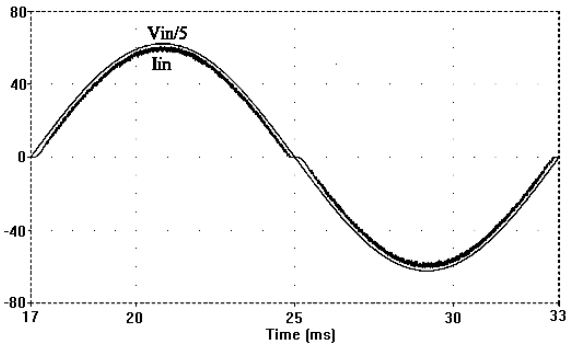


Fig. 4. Duty cycle versus normalized load current, when the static gain is varied.

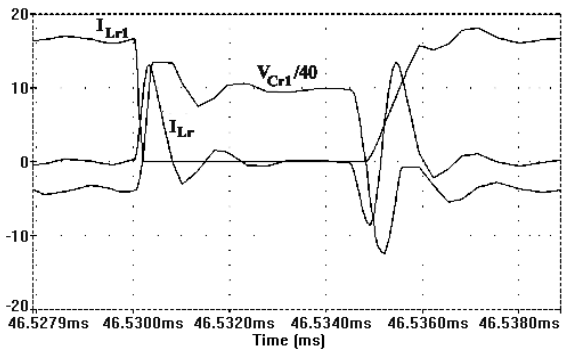
#### V. CONCLUSION

This paper has reported analytical, simulation and experimental results of a PFC interleaved Boost-Flyback converter. It has been demonstrated that the converter provides highly efficient power factor correction without commutation losses, using the same number of switches of the hard-switched structure. The proposed approach allows a good performance at high switching frequencies, as the use of soft-switching techniques provides satisfactory performances at high voltage and high power, due to the reduced conduction and switching losses.

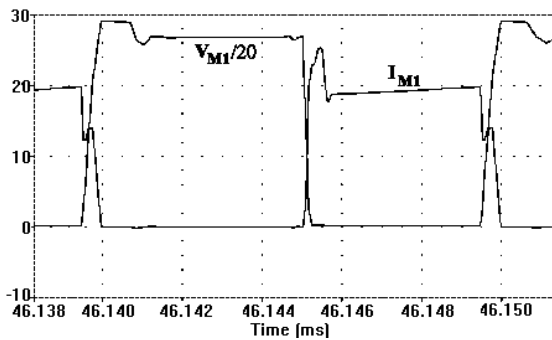
The behavior of the converter is analyzed, where it can be seen that the main switches are turned on and turned off in ZCS and ZVS modes, respectively. An experimental prototype of the converter was implemented, as the experimental results validate the theoretical study.



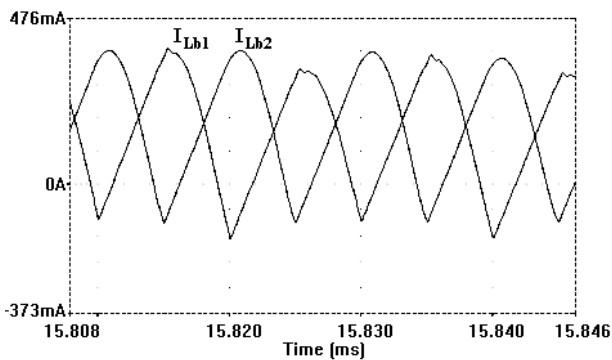
(a) Input voltage and input current



(b) Resonant tank waveforms

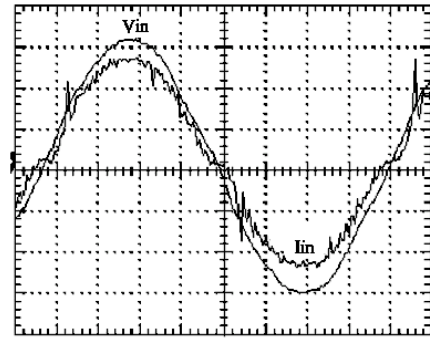


(c) Drain-to-source voltage and current waveforms of switch  $M_1$



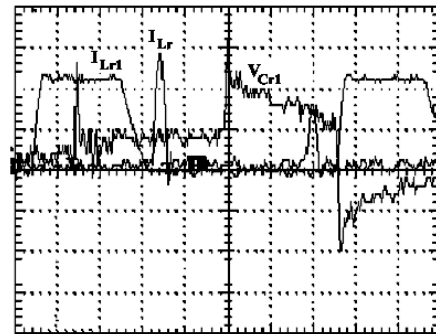
(d) Current through Boost inductors

Fig. 5. Waveforms obtained in simulation tests.



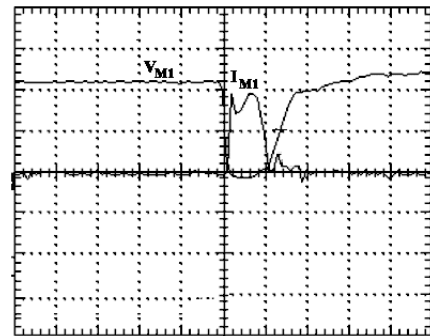
(a) Input voltage and input current

Scales:  $I_{in} - 100V/div.$ ;  $V_{in} - 20A/div.$ ; time - 2ms/div.



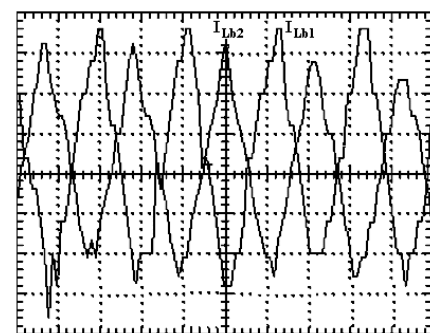
(b) Resonant tank waveforms

Scales:  $I_{Lr1} - 10A/div.$ ;  $I_{Lr} - 5A/div.$ ;  $V_{Cr1} - 200V/div.$ ; time - 2 $\mu$ s/div.



(c) Drain-to-source voltage and current waveforms of switch  $M_1$

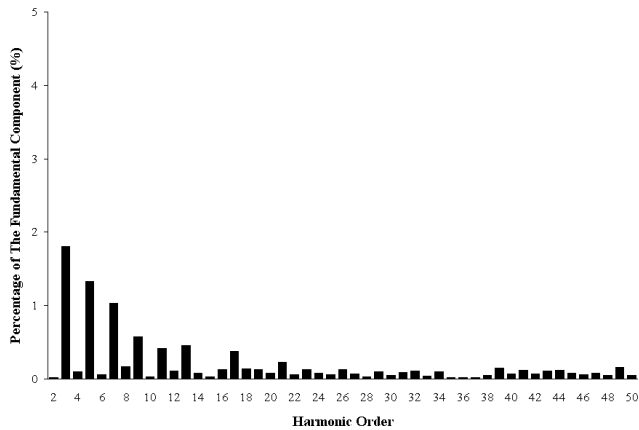
Scales:  $V_{M1} - 200V/div.$ ;  $I_{M1} - 10A/div.$ ; time - 2 $\mu$ s/div.



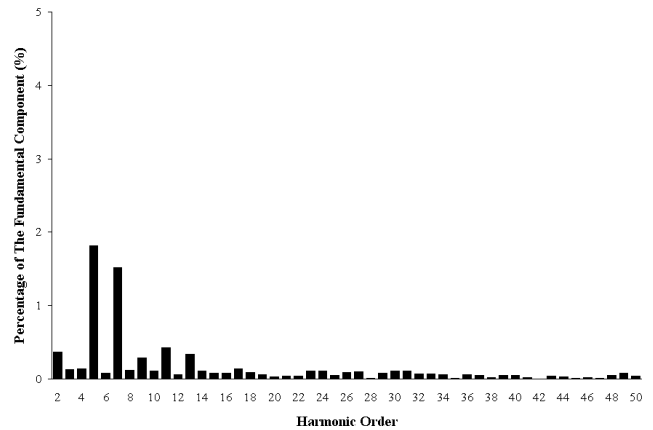
(d) Current through Boost inductors

Scales:  $I_{Lb1}, I_{Lb2} - 100mA/div.$ ; time - 10 $\mu$ s/div.

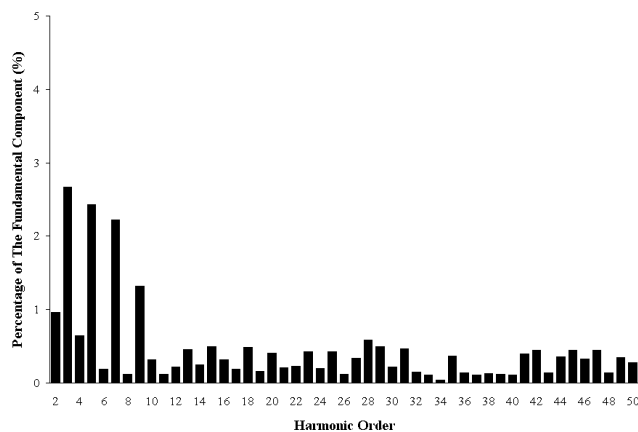
Fig. 6. Waveforms obtained in experimental tests.



(a) Input current – simulation results ( $THD_I=2.84\%$ )



(b) Input voltage – experimental results ( $THD_V=2.83\%$ )



(c) Input current – experimental results ( $THD_I=4.85\%$ )

Fig. 7. Harmonic spectrum.

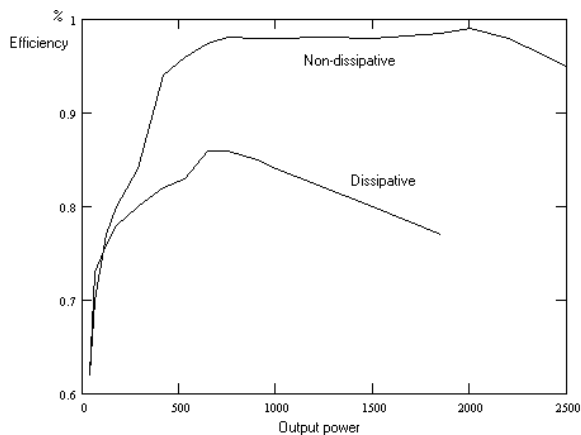


Fig. 8. Efficiency curve.

## VI. ACKNOWLEDGMENT

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## REFERENCES

- [1] G.C. Hua, F. C. Lee “Novel Zero-Voltage-Transition PWM Converters”, IEEE Power Electronics Specialists Conference, 1992, pp. 55-61.
- [2] G.C. Hua, F.C. Lee “Novel Zero-Current-Transition PWM Converters”, IEEE Power Electronics Specialists Conference, 1993, pp. 538-544.
- [3] B.A. Miwa, D.M. Otten, M.F. Schlecht “High Efficiency Power Factor Correction Using Interleaving Techniques”, Proceedings of APEC 1992, pp. 368-375.
- [4] L. Balogh, R. Redl “Power-Factor Correction with Interleaved Boost Converter in Continuous-Inductor-Current Mode”, Proceedings of APEC 1993 (IEEE Catalog n0, pp. 168-174).
- [5] F.C. Lee “High-Frequency Quasi-Resonant Converter Technologies”, Proceedings of the IEEE, vol. 76, no. 4, April 1988, pp. 337-389.
- [6] F.C. Lee, J. Zhang, J. Sheo, M. Xu, M.M. Jovanovic “Evaluation of Input Current in the Critical Mode Boost PFC Converter for Distributed Power Systems”, Proceedings of APEC 2001, pp. 130-136.

- [7] J.A. Corrêa Pinto, A.A. Pereira, V.J. Farias, L.C. Freitas, J.B. Vieira Jr. "A New Boost Converter Using A Non-Dissipative Snubber", Proceedings of PESC 1996, pp 397-401.
- [8] C.A. Gallo, J.A. Corrêa Pinto, V.J. Farias, L.C. Freitas, E.A.A. Coelho, J.B. Vieira Jr. "Soft-Switched PWM High-Frequency With PFC Converter Using Boost-Flyback Converter Interleaved", COBEP'01, Record pp. 675-679, Florianópolis, Santa Catarina, Brazil.
- [9] J. Kin, D.Y. Lee, H.S. Choi, B.H. Cho, "High Performance Boost PFC Pre-Regulator with Improved Zero-Voltage-Transition (ZVT) Converter", Proceedings of PESC 2001, pp. 337-342.
- [10] J. Chen, D. Maksimovic, R. Ericson, "A New Low-Stress Buck-Boost Converter for Universal Input PFC Application", Proceedings of PESC 2001, pp. 343-349.
- [11] I. Barbi, C.M.T. Cruz, "Unit Power Factor Active Clamping Single Phase Three Level Rectifier", Proceedings of APEC, 2001, pp. 331-336.
- [12] J.A. Corrêa Pinto, A.A. Pereira, V.J. Farias, L.C. Freitas, J.B. Vieira Jr. "A Power Factor Correction Preregulator AC-DC Interleaved Boost with Soft-Commutation", Proceedings of PESC 1997, pp. 121-125.
- [13] C.S. Silva, "Power Factor Correction with The UC3854". Unirode Application Note.
- [14] C.A. Gallo, J.A. Corrêa Pinto, V.J. Farias, L.C. Freitas, E.A.A. Coelho, J.B. Vieira Jr. "Soft-Switched PWM High-Frequency with PFC Converter Using Boost-Flyback Converter Interleaved", Proceedings of IEEE INTELEC 2002, pp. 356-360, Montreal, Quebec, Canada.
- [15] J.A. Corrêa Pinto "Analysis, Design and Implementation of a High Power Factor Switched-Mode Power Supply with Soft Switching Employing an Interleaved Boost Converter as a Preregulator Stage", Uberlândia, Minas Gerais, Brazil, 1997. MSc Thesis – Federal University of Uberlândia.

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