Control System for Multi-Inverter Parallel Operation in Uninterruptible Power Systems

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***Abstract* – This paper proposes a network communication system applied in a control strategy for parallel-connected multi-inverters, which is based on a distributed control system and a redundant communication system. The control system is produced by a Phased-Locked Loop (PLL) synchronism algorithm, a voltage controller and a parallelism controller. All control systems are based on instantaneous values and in the parallelism control the inverters share a single voltage reference signal. The communication system, which is the main focus of the paper, is based on two buses: one analog, which is a measurement taken from the electrical grid; and one digital, comprised of a Controller Area Network (CAN). The former allows the reference voltage of all inverters to be in synchronism and the latter keeps the reference voltage in synchronism even during a grid power outage. There is a PLL algorithm in each Voltage Source Inverter (VSI), which ensures the synchronism between the internal reference and external signal received from the grid or from the CAN. The proposed networked control system was verified in three 5 kVA three-phase VSIs operating in parallel. Experimental results with static and dynamic tests and with electrical grid interruption and return, were obtained. The networked control system is redundant and it provides increased reliability, thus it can be applied in the parallel operation of an on-line Uninterruptible Power Supply (UPS).**

***Keywords* – CAN, Parallel, PLL, VSI.**

I. INTRODUCTION

In recent decades, the number of critical loads that require a power supply with high-reliability and redundancy has increased. These power supplies can be obtained with the parallel-connection of uninterruptible power supplies (UPSs), as demonstrated in Figure 1. As it is well-known, the parallelism of UPS is a problem related to the parallel operation of voltage source inverters (VSIs) which presents complications due to the complexity and the greater number of variables involved, especially in a three-phase system.

The control strategies for the parallel operation of VSIs can be divided into two categories: with and without communication. Traditional strategies without communication are based on the frequency and voltage droop [1]–[4]. This approach provides increased redundancy, however, extended and complex controllers have to be implemented and errors associated with load sharing, poor transient response and poor division of current harmonics occur. Also the system becomes complex, what can decrease its reliability. Interesting strategies to minimize these disadvantages have been reported [3]–[14], as the virtual impedance concept [3], [4], stability analysis [5], robust droop control [7], universal droop control [9], and improvements of virtual impedance and droop controls for different applications of VSI [13], [14]. Some works also integrate to the droop control a level of communication, which improves its performance [10], [11]. In this case, the control uses usually a low bandwidth communication and when the communication fails, the system can continue to operate with no communication. The strategies related to communication include central control [15], [16], master-slave control [17]–[19] and distributed control [20], [21]. These strategies are more effective regarding load sharing, but achieving high reliability and redundancy is still a problem due to the communication among units. For example, in central and master-slave control systems, the inverters cannot work independently, therefore, the reliability and redundancy in these systems are poor. However, with distributed control it is possible to improve: (i) the reliability when adequate control and communication systems are used; and (ii) the redundancy when an $n+1$ structure is applied to the VSIs and the communication system.

There are two main types of communication systems: (i) analog signal communication [12], [15], [22]–[25]; and (ii) digital signal communication [10], [11], [20], [26]–[29]. Analog signal communication presents good transient response. However, with analog communication it is easier to be interfered and its isolation is complicated. In the case of a digital signal, the communication among inverters is based on the communication bus (for example, a Controller Area Network (CAN) bus) and the anti-interference capability and reliability are increased. However, due to the limitation of the communication capacity (low bandwidth) of the bus, there are difficulties associated with implementing instantaneous control.

This paper proposes an improved master-slave control strategy by integrating a redundant communication system to the distributed control proposed in [22], [23], [30]. This strategy utilizes only internal variables from each VSI to control the parallel operation and its main attribute is that it just has to synchronize the output voltage reference with all inverters. In [22] and [23], the inverters use an analog signal communication to receive this information (a 60 Hz sinusoidal waveform), which was generated from of a sample of the electrical grid. However, if a grid interruption occurs, the analog communication will fail. In [30], a robust

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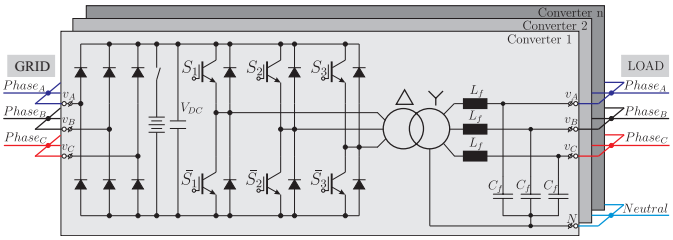

Fig. 1. High-reliability and High-redundancy UPS employing parallel connection of VSI modules.

digital synchronism Phased-Locked Loop (PLL) algorithm was added to the strategy control, which can keep the internal voltage reference even during a grid interruption, but it does not guarantee the synchronism among the inverters. For this study, a grid interruption or a outage is when there is no power in the grid and the three-phase voltages are zero.

The communication system, which is the main focus of this paper, is a redundant communication system based on two buses: one analog, which is a measurement taken from the electrical grid (as used in [22] and [23]) and synchronized by PLL algorithm (proposed in [30]); and another digital, comprised of a CAN bus. Both systems have features of high bandwidth communication. This paper reports a study on the way in which the two communication systems operate together to improve the reliability and the redundancy of the distributed control strategy. A random logic that defines one VSI (a master) to monitor the CAN bus and a strategy to change the master inverter when the current is turned off are also proposed herein. The study verifies the integration between the communication system and the parallelism control system through expressive experimental results.

II. CONTROL SYSTEM

This section presents important details about the whole control system. Thus the improved master-slave strategy, communication network, and PLL are approached herein.

A. Control Strategy

The control strategy employed [22], [23] can be classified as a improved master-slave and it consists of two control loops, a voltage controller and a parallelism controller, as seen in Figure 2. Both are implemented in an orthogonal stationary frame and employ instantaneous values, which provide the decoupling between orthogonal α and β axes in three-phase systems and offer an appropriate dynamic response for parallelism control.

The voltage controller is responsible for regulating the output voltage, with feedback by the LC filter capacitor voltage (output voltage), and it is a digital proportional-integral-derivative controller (PID). The parallelism controller ensures the load is shared equally among the inverters, with feedback by the LC filter inductor current. The parallelism controller consists of a gain (K_{IL}) in the current feedback loop [22], [23].

The employed control is based on the resistive virtual impedance concept, but unlike works as [1] the control employs the inductor current feedback, and not the output current. In this case, the virtual impedance is emulated in series with the inductor, which provides dampness to the

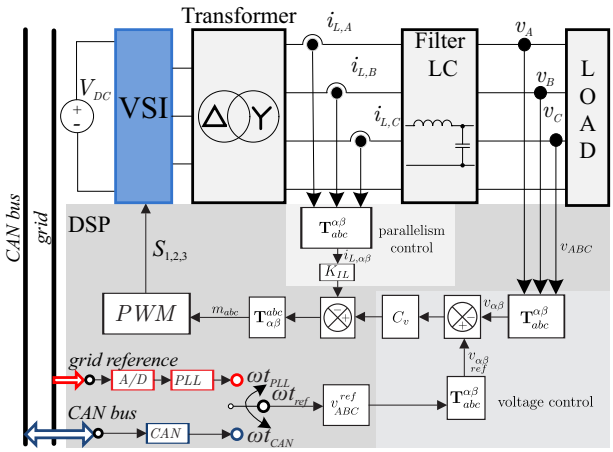

Fig. 2. Power and control scheme for a three-phase VSI module.

system. Furthermore, researches as [1] have adopted complex virtual impedances and herein it is proposed a resistive virtual impedance (named as KIL). It should be noticed that the proposed parallelism control, shown in Figure 2, does not need information regarding how the other inverters are working, as power, current or even the number of VSI parallel-connected. It should be recapped that the improved master-slave has to use a network to share information about all units, which allow all units to achieve the same goal.

There is only one condition under which this strategy can work properly, that is, the voltage references of all VSI must be synchronized. Therefore, the only external data which has to be exchanged among the inverters is related to the phase of the voltage reference. This advantage makes the inverters independent of each other with regard to connecting or disconnecting from the system. With the main aim being to improve the reliability of UPS system, two communication buses are proposed: one analog and another digital, as demonstrated in Figure 2 and discussed in the next section.

A block diagram with details of the control strategy implemented in one VSI is shown in Figure 3. As previously mentioned in this paper, the parallelism control consists of a virtual resistance (K_{IL}). When the K_{IL} value increases, the current division among the inverters will be better. On the other hand, a high value of the virtual resistance will reduce the output voltage regulation. Then, taking this into account, it is designed a $K_{IL} = 0.1pu = 0.97\Omega$, and the voltage PID controller was designed employing the classical control theory.

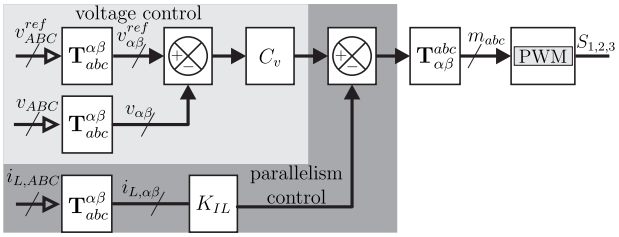

Fig. 3. Block diagram of control strategy with emphasis in $\alpha\beta$ voltage controller and also the $\alpha\beta$ parallelism controller.

B. Communication System

There are two buses which perform the communication between the modules, one being an analog bus and the other one a digital communication bus. The analog bus is the voltage reference sampled from the electrical grid ,which is measured in each module rectifier input. This implementation avoids the use of an external connection between the modules, reducing the number of connections required.

The electrical grid supplies energy to the V_{DC} voltages of each module (see Figure 2) in normal operation mode. If a interruption occurs in the electrical grid, a battery pack in each module (UPS) will maintain the V_{DC} sources. During periods when there is a power interruption in the grid, the analog bus does not work and another bus has to be enabled to maintain the system operation. For this situation, a digital communication bus is proposed to keep all modules synchronized even when there is a grid interruption. The digital communication ensures that (i) one module sends its voltage reference and (ii) the other modules receive this reference. Each inverter has a PLL circuit that synchronizes its internal reference with the received reference.

The system operates in manner very similar to a master-slave system, but unlike a master-slave control, where all modules depend on the master to operate properly, the proposed communication system does not have this dependency, this is, all modules are on the same hierarchical level.

Thus, the system is referred to as improved master-slave. The master module is responsible for sending the phase reference that synchronizes the inverters. The data shared among the inverters are detailed in the Table I.

TABLE I

Digital Data Shared Among the Inverters.

Data	Description	Data length
Phase Reference (ωt_{CAN})	contains the phase reference	2 Bytes
Master	contains the master number	1 Byte

The phase reference (ωt) is sent by the master to all other modules connected to the system and it contains the reference that ensures all inverters are synchronized. This data must be sent at a high rate, several times in a grid cycle, although there is no need to send it every switching period. A VSI can receive a new phase reference after a few switching periods. This advantage is obtained because the PLL keeps its reference synchronized for a long time comparatively with switching frequency [30]. The master data contains the identifier number of the module and this is a request to change the master module. This data is only sent when the present master module is disconnected from the parallelism (occurrence of a failure or intentional module shut down) or there is a master change request by the user. In these cases, another VSI becomes the master. The complete system can be observed in Figure 4, where both communication buses and the common AC load bus are represented.

C. Digital Synchronizing Phased-Locked Loop (PLL) Circuit

The addition of the PLL provides a sine reference with reduweced distortion, even during disturbances, such as an unbalanced line or harmonic distortion. The PLL that has been

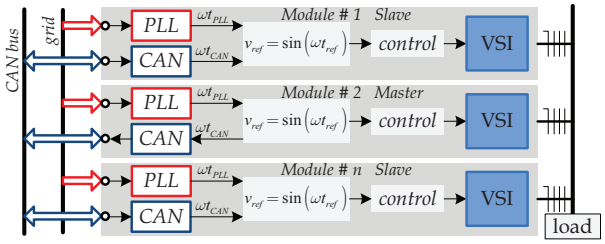

Fig. 4. Proposed communication system with two redundant channels: a CAN bus and a grid reference synchronized by a PLL.

used is a conventional Stationary Reference Frame PLL (in the literature is called type-2 PLL) [31]. The Figure 5 shows the PLL block diagram.

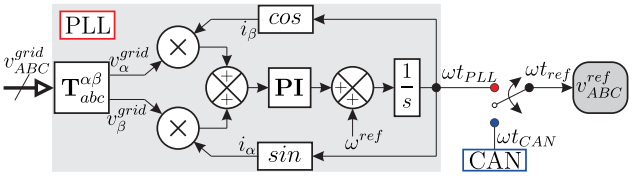

Fig. 5. Representation in block diagram of PLL synchronism circuit.

When the PLL is locked its phase output (ωt) will be synchronized with the Voltage Reference bus, which implies that all VSI references are synchronized. When there is an electrical interruption, the PLL input and thus the proportional-integral (PI) controller input will be zero.

In this situation, the frequency from the ωt should remain constant, but this does not happen due to the differences between the inverters and the controllers, mostly clock differences. Hence, the phase tends to diverge after a few switching periods. For that reason, it is important to use a communication system to keep the voltage references in all VSIs synchronized even when a PLL is employed in each inverter.

III. PROPOSED COMMUNICATION STRATEGY

This section addresses a few important characteristics of the proposed communication network. Firstly, implementation details on the analog and digital communication buses are given. The operation of the buses and the influence of the transmission time in the parallel operation of the inverters are then explained.

A. Voltage Reference (Grid)

The voltage reference bus is an analog reference, sampled from the electrical grid through a signal transformer.

The voltage reference sample is applied at the input of the PLL, which generates a phase reference that is synchronized with the positive sequence of the grid. The reference phase generated by the PLL is used to restore the three-phase voltage references, without harmonic distortion, which are then employed in the voltage control.

The voltage references generated by the PLL are synchronized with the electrical grid and consequently the references of all inverters are in phase, allowing the inverters to be connected in parallel.

Even after a grid interruption the inverters can use their own internal reference provide by PLL for a period of time,

without significantly affecting the load sharing. The internal references will diverge after a grid interruption, however, this will occur very slowly, what gives the control time to identify the power interruption and start using the reference received from the master VSI.

B. Communication Protocol - CAN

The communication protocol used was the Controller Area Network (CAN), mainly due to its noise immunity and multimaster characteristic.

This protocol is ideal for applications in noisy and harsh environments, when reliable communication is required. It can achieve a communication rate of up to 1 Mbps, with a maximum bus length of 40 m, and transmit from 0 to 8 bytes of data.

The noise immunity is achieved by using a differential twisted pair with low impedance terminations (120Ω). The data frame size sent by the CAN is determined by the identifier, that is, 12 bits for the standard identifier (CAN 2.0A) and 32 bits for the extended identifier (CAN 2.0B), and the number of bytes in the data. From the total numbers of bits sent the CAN transmition time can be calculated by

$$T_{CAN} = N_{bits}/BaudRate. \quad (1)$$

When a node connected to the bus starts sending a message, it becomes the master. All of the other nodes become slaves and they receive the message sent by the master node. In addition, the protocol automatically defines the priority of the messages through the message identifier (the closer to zero the higher the priority).

The advantages of using the CAN can be summarized as follows:

- it is a multi-master protocol in which any node can send and receive data;
- it presents high reliability due to the noise immunity, both being characteristics which make it suitable for application in the parallel operation of VSI.

C. Redundant System: CAN + V_{grid}

In order to achieve a reliable redundant system, as required for UPS applications, there are two communication network buses to ensure the reference synchronism in the system. The first bus is a sample from the electrical grid and the second one is a digital communication bus based on the CAN protocol. Hence, the proposed strategy employs two buses to improve the reliability, which is very important when UPS are parallel-connected. The system can not stop when a interruption occurs in the utility mains or the communication system. Thus, two buses work as an N+1 redundant system. When the grid is turned-on, the system uses the grid as reference. If a grid interruption occurs, the system will use the exchanged information by the CAN to synchronize the VSIs.

The use of the electrical grid as the voltage reference (analog signal communication) ensures that all inverters are synchronized with each other and with the electrical grid, which is of interest for online UPS applications. The electrical grid supplies energy to the VSIs in normal operation mode and thus it can be used as a reference signal to synchronize the VSIs. A digital PLL is employed, which guarantees the synchronism with the electrical grid even under unbalanced grid conditions or when there is a phase fault. In addition, the PLL avoids propagation of the grid harmonic distortion to the V_{ref} and, consequently, to the output voltage. It also keeps generating the ωt_{PLL} even in a total power outage of the grid.

The CAN bus (digital signal communication) ensures the synchronism during a power outage, since the PLL output ωt_{ref} starts to diverge due to the clock differences among the microcontrollers.

Both buses are active at all times and the choice between the ωt_{PLL} from the PLL or the ωt_{CAN} received by the CAN depends if there is or not a grid power. Therefore, there are two operation modes: normal mode (when the grid is on) and outage mode (when a grid interruption occurs). These two operation modes are described below:

- **Normal Mode**: each inverter generates its own ωt_{PLL} via the PLL, synchronizing the internal reference with the electrical grid, ensuring that all of the internal inverter references are synchronized. In this case, all VSIs use $\omega t_{ref} = \omega t_{PLL}$ (see Figure 6).

- **Outage Mode**: when a grid power interruption occurs the PLL input is zero and the frequency is maintained constant, but due to the differences between the controllers (clock, numeric errors etc.), it cannot be guaranteed that the inverters are synchronized in relation to the reference. Therefore, the slaves start to use the reference that the master sends by CAN(ωt_{CAN}) and thus all inverters use a single reference. In this mode, all slaves use $\omega t_{ref} = \omega t_{CAN}$ (see Figure 6).

The firmware control routine flowchart is shown in Figure 6. The control routine is executed once in each sample period, which is half the switching period, and it is started by a PWM interrupt (INT) at minimum and maximum carrier values.

After each interruption the control variables (V_{ABCN} and $I_{L,ABC}$) and the voltage reference bus (V_{grid}) are sampled and after the processor finishes converting the samples, it is verified whether or not there is a grid interruption. In the case of an outage, all the V_{grid} samples are zeroed to avoid noise in the PLL input.

The PLL, which generates the internal phase reference (ωt_{PLL}), is then calculated and if the module is the master, it sends the reference ωt_{CAN}, which is its internal reference compensated by the transmission delay ($\omega t_{CAN} = \omega t_{PLL} + \delta\omega t$), and it will use the ωt_{PLL} as the phase reference (ωt_{ref}). If the module is a slave, it compares the internal reference with that received by the CAN and if the difference is smaller than a tolerance ($\Delta\omega t$), it will use the ωt_{PLL}, otherwise it will use the ωt_{CAN} as the phase reference and correct the ωt_{PLL} (see Figure 6). This tolerance is the discrete step of the ωt, and basically depends on the sampling frequency, for this paper it is considered a tolerance of $\Delta\omega t = 1.07°$.

It should be noticed that both communication buses are active all the time, and the transition between the normal mode and outage mode will occur when the voltage phase reference from the PLL (ωt_{PLL}) and the CAN (ωt_{CAN}) start to diverge ($|\omega t_{CAN} - \omega t_{CAN}| > \Delta\omega t$), the other way around, the transition from the outage mode to normal mode occurs when

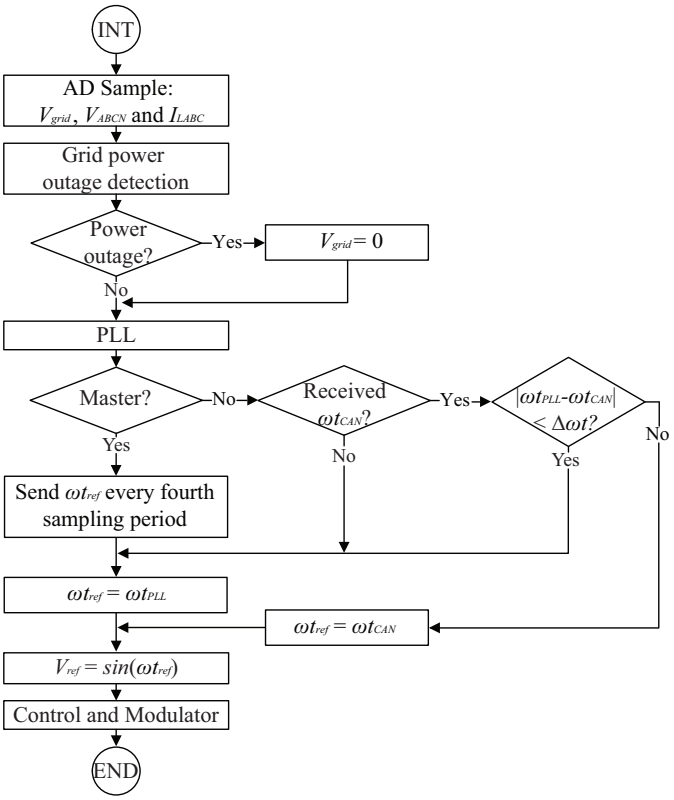

Fig. 6. Block diagram with flowchart of firmware control routine.

the references converge ($|\omega t_{CAN} - \omega t_{CAN}| < \Delta\omega t$).

Finally, the inverter uses the phase reference (ωt_{ref}) to generate the three-phase reference and execute the control routines calculating the new duty cycle.

To elucidate how the control and communication work, they are represented over time in Figure7, which shows the actual ωt from the grid and the discrete phase generated by the PLL (ωt_{PLL}), the PWM carrier and the pulse that generates the interrupt (INT) synchronized with the carrier.

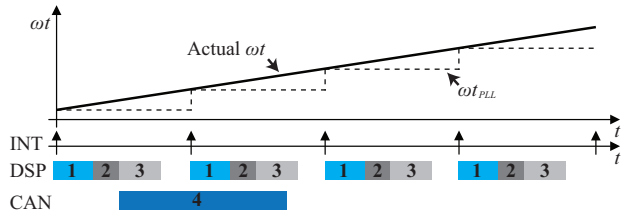

Fig. 7. Representation of control and communication over time.

The bars at the bottom of the Figure 7 represent the CPU processing (DSP) and the transmission of the ωt_{CAN} by the CAN bus. The bar (1) represents the sampling time, the bar (2) the PLL calculation and the bar (3) the control routine. The CAN transmission time is represented by the bar (4).

In some cases the CAN transmission time may be longer than the sampling frequency, as represented in Figure 7. A slave VSI can receive the ωt_{CAN} from the master at any point of the operation since there is no synchronism among the module carriers.

D. Master Election

The system will always have one master module and all other modules parallel connected to the system will be slaves. However when the master module is shut down, disconnected or suffers a failure, the system will be temporarily without master. In this case, the previous master stops sending the reference, after an arbitrary time, it is considered half cycle of the grid (8.33 ms), the slaves detect the master absence.

Once any slave module detects the master disconnection it will send its own identifier number, trying to become the new master of the system, after that the others slave modules will send back the module identifier number confirming the new master, which will start sending the reference.

In addition to that, when a module receives a reference from the CAN, it is automatically configured as a slave, ensuring that there is never more than one master in the system.

E. Time Delay

When there is no grid interruption, the PLL generates a discrete ωt, which is synchronized with the positive sequence continuous ωt from the electrical grid and, in this case, the ωt_{PLL} is increased by discrete steps, defined by

$$\Delta\omega t = \frac{f_{grid} \cdot 2\pi}{f_{sample}}. \tag{2}$$

In this case, the inverters use different values of ωt_{ref} ($\omega t_{ref} = \omega t_{PLL}$) due to the discretization and the carrier phase shift, what generates different instantaneous values of ωt_{PLL} inside each VSI. However, in a same time period, the mean values for ωt_{PLL} are equal in all VSIs, guaranteeing the synchronism among the inverters. It is important to note that the phase difference between the carriers is constantly changing due to small differences in the processor clock frequency.

The normal mode operation is represented in Figure 8, where the actual ωt is the grid phase which is discretized and restored through the V_{grid} sample and, in this case, the carrier delay is 90^o when the difference between the internal VSIs ωt_{PLL} is maximum.

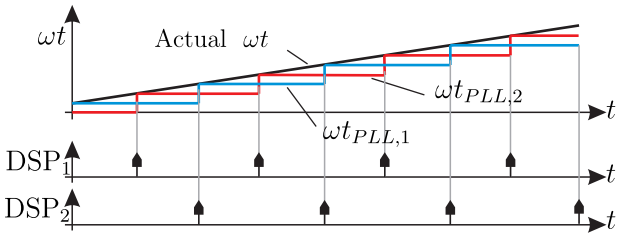

Fig. 8. Difference in ωt of master and slave operating operating synchronously with grid.

As previously shown, the master CAN takes a certain time (T_{CAN}) to send the message containing the ωt_{CAN} to the slave, and this delay must be compensated. Therefore, the master adds a constant value ($\delta\omega t$) to the ωt_{PLL} and thus defines ωt_{CAN} as

$$\omega t_{CAN} = \omega t_{PLL} + \delta\omega t. \tag{3}$$

The value of $\delta\omega t$ is a multiple of the ωt_{PLL} increase ($\Delta\omega t$) and this value is calculated by

$$\delta\omega t = \left\lceil \frac{T_{CAN}}{T_{sample}} \right\rceil \Delta\omega t. \tag{4}$$

When the system operates in the outage mode, all inverters use the same reference value, but time shifted, i.e., the references are not perfectly synchronized.

Although the references are time shifted, they will always be limited by the maximum lag (ΔT_{lagMAX}) and the maximum lead ($\Delta T_{leadMAX}$), expressed by

$$T_{CAN} \equiv \Delta T_{LagMAX} (mod\ T_{sample}) \tag{5}$$

while

$$\Delta T_{LeadMAX} = T_{sample} - \Delta T_{LagMAX}, \tag{6}$$

where $\equiv$ is the congruence symbol. Hence, in (5) ΔT_{LagMAX} is the residue of division between T_{CAN} and T_{sample}.

The boundaries to the lag and lead are dependent on the sample period (T_{sample}) and transmission time, the faster the sampling rate the smaller the boundaries will be. The transmission time influences the difference between the lead and lag time limits. When the transmission time is a multiple (n) of the sample period, the $\Delta T_{leadMAX}$ assumes its maximum value and the ΔT_{lagMAX} is zero, what means the slaves are always injecting more power into the output common AC bus. The opposite occurs when the transmission time is $(n+1)$ times the sample period and, in this case, the master supplies a bigger share of the load.

The best case of operation in the outage mode is when the CAN transmission time is exactly $(n+\frac{1}{2})$ times the sample time, since this implies that ΔT_{lagMAX} is equal to $\Delta T_{leadMAX}$. In this case, the slave ωt variation is centralized with the master ωt_{PLL}, balancing the load sharing over time, even if the instantaneous value is not balanced (see Figure 9). This occurs since the point of operation (carrier delay) is constantly changing, due to the differences in the processor clock frequencies.

The Figure 9 shows the characteristics of the operation in outage mode. The master sends the reference after sampling the control variables and calculates the PLL (1 and 2) and the slaves use the reference received before the end of the PLL calculation. If a slave does not receive the data, it increases its reference by $\Delta\omega t$. The Figure 9 (a) shows the maximum lag which occurs when a slave receives the reference just after calculating his own PLL reference. Thus, it will use the value received in the next ωt_{ref} calculation cycle. The Figure 9 (b) shows the maximum lead, which occurs when a slave receives the data just before the end of PLL calculation. In this case, it uses the value received in the current calculation cycle. Cases (a) and (b) are opposites and are the maximum boundaries and the reference (ωt_{CAN}) received by the slaves is always between these two limits. These boundaries can be seen in Figure 9 (c). In (a), (b) and (c), period of 50 μs and a transmission time of 60 μs are considered. In Figure 9 (d), the best case is considered and boundaries for a sampling time of 50 μs and a transmission time of 75 μs are shown.

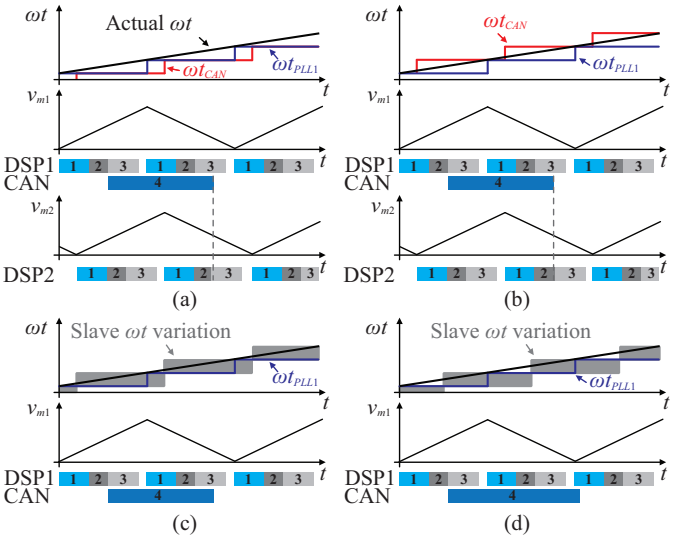

Fig. 9. Boundaries and variation of ωt between master and slave in Outage mode. (a) maximum lag boundary. (b) maximum lead bondary. (c) slave ωt_{ref} variation. and (d) slave ωt_{ref} variation for the best case.

IV. EXPERIMENTAL RESULTS

A prototype with three modules of three-phase VSIs with 5 kVA (modules 1, 2 and 3) operating in parallel was implemented to verify the proposed networked control strategy. A photograph of three parallel-connected modules can be seen in Figure 10, while the design specifications are in Table II, it is emphasized that the filter inductance L_F is composed by the transformer leakage and an additional inductor resulting in the $540\mu H$ total filter inductance.

The proposed networked control system for parallel-connected multi-inverters was tested with three VSI modules parallel connected. Firstly, the dynamic test results, which show the system response when a change from the analog to digital communication occurs and vice versa, are presented. These disturbances act as connection or disconnection of power modules, as well when a grid interruption occurs. After that, steady-state operation results are reported. These tests were obtained for conditions without load, with resistive load and also with non linear load, when the UPS is operating in the normal and outage modes.

A. Steady-state Tests

The steady-state tests were carried out with 3 VSI modules parallel-connected. In the first test, the system operates without load, which is the worst case for the parallel VSI operation.

The Figure 11 (a) shows the output voltages v_A, v_B and

TABLE II
Project Parameters for a VSI Module

Parameter	Symbol	Value
LC filter capacitance	C_F	18 μF
LC filter inductance	L_F	540 μH
Switching frequency	f_{sw}	10080 Hz
Sampling frequency	f_s	20160 Hz
RMS output line voltage	V_{FN}	220 V
Output frequency	f	60 Hz
Transformer ratio (line to line)	n	190/380
VSI output power	$S_{3\phi}$	5 kVA
DC bus voltage	V_{DC}	540 V
Transmission time CAN bus	T_{CAN}	60 μs
Virtual resistance	K_{IL}	0.97 Ω
Voltage controller	$C_V[z]$	$\frac{1.80z^2-2.98z+1.22}{z^2-0.499z+0.501}$

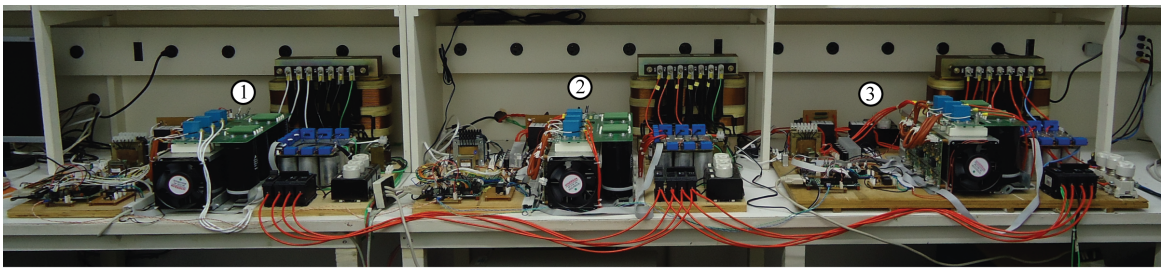

Fig. 10. Laboratory prototype implemented with three modules of three-phase 5 kVA VSIs parallel connected.

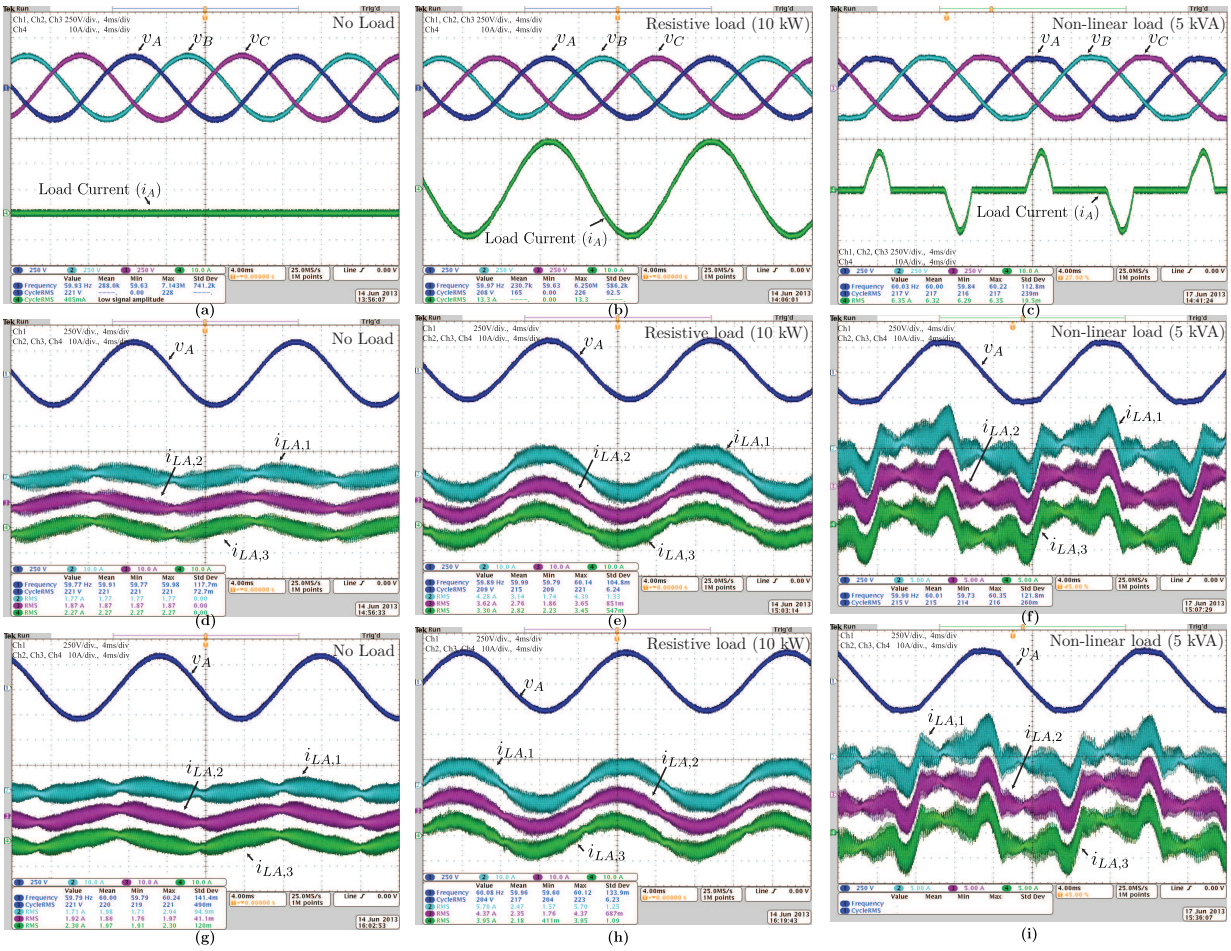

Fig. 11. Experimental results in steady-state of three VSI modules, in normal mode and outage mode, considering three conditions of the load (no-load, resistive load, non-linear load):voltage output and load current for (a) no load, (b) resistive load 10 kW and (c) non-linear load 5 kVA. Output voltage phase A and 3 modules currents under normal mode (d) no load, (e) resistive load 10 kW and (f) non-linear load 5 kVA. Output voltage phase A and 3 modules currents under outage mode (g) no load, (h) resistive load 10 kW and (i) non-linear load 5 kVA.

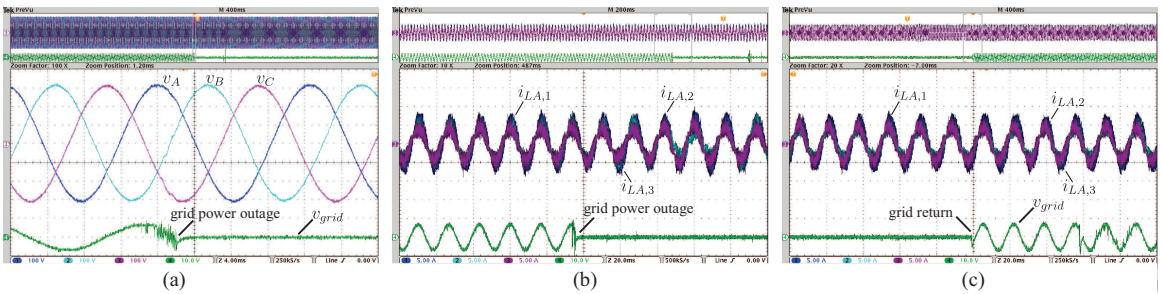

Fig. 12. Experimental results of voltages and currents when a outage and return of electric grid happen: (a) output voltage when there is a grid interruption. (b) output current when there is a grid interruption. (c) output current when the grid return.

v_C (supplied by three VSIs), which are at the nominal values and adequately regulated by the voltage control. The system was tested in the normal and outage modes. The inductor currents $i_{LA,x}$ from the three inverters (same phase A) are presented in Figure 11 (d) operating in the normal mode and in Figure 11 (g) in the outage mode, where the phase A output voltage (v_A) is also shown. The parallelism strategy works adequately because the inductors currents flow is symmetrical and equilibrated. As above mentioned no-load condition is the worst case to parallelism strategy, and as demonstrated in Figure11 (a), (d) and (g), the inductors currents are just to supply the losses and reactive energy for the filters. Therefore, even in no-load condition, the parallelism strategy works successfully in normal mode and also in grid outage mode.

The second test was carried out with a resistive load supplied by the three parallel modules. The Figure 11 (b) illustrates the output voltage, which remains regulated, and the load current in phase A. The system was also tested in the normal and outage modes. The load current sharing for phase A can be seen from the inductor L_A currents, which are shown in Figure 11 (e) and (h) for both modes. These tests were made in a redundant structure N+1 in terms of inverters, thus the power supplied by each VSI was around 60% of its total capability. The parallelism control strategy provides a good performance in relation to the current level. Thus, if the current level to increase, the current sharing will be better. In both tests under resistive load the communication buses kept the system in operation with similar results.

The last test was conducted with a non-linear load. The Figure 11 (c) shows the output voltages, which are distorted due to the load type. However, they are still regulated accordingly. This result also shows the phase A current drained by the load. Once again, the system was tested in the normal and outage modes and the current sharing remains adequate, as seen in the Figure 11 (f) and also in Figure 11 (i).

One challenge in control strategies with communication is the reliability that is low due to communication when compared with droop control. Hence, the tested communication system can increase the reliability of the distributed control proposed in [22], [23], [30] by a networked control system, which makes the control strategy adequate for on-line UPS. Furthermore, the communication system keeps the output voltage synchronized with the electrical grid, which is a challenge in strategies without communication. Voltage and frequency deviations are problems in strategies as droop control and a solution that improves this issue is also to employ a networked control system [13], [14].

B. Dynamic Tests

1) Grid Outage Transient: The Figure 12 (a) and 12 (b) show the system behavior in a outage of the electrical grid. Tests were carried out with resistive load and the inverters were fed by batteries during all tests of electrical grid interruption. To emulate the grid outage the system feed was open with a circuit breaker, which generated the noise in the grid voltage signal, however it is observed that this noise does not affect the load share, neither the output voltage. In Figure 12 (a) the output voltage when there is a grid interruption can be observed, as expected, the voltage is less affected by changes in the reference.

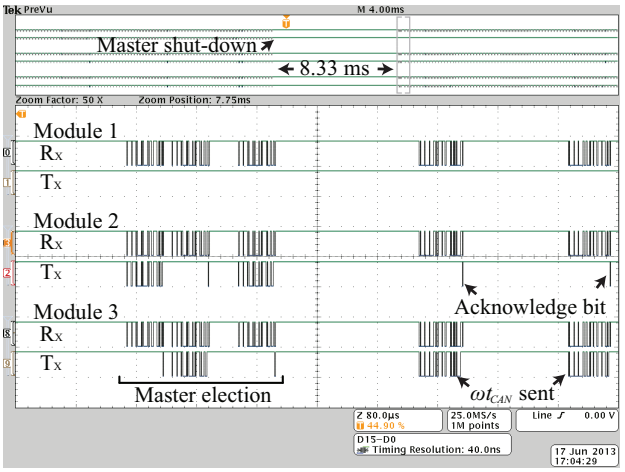

Fig. 13. Determination of master and sending of reference by the CAN bus.

The current sharing is more sensitive to differences in the references. Thus, in the Figure12 (b) it can be observed there is a small transient in the currents of the three modules when there is a grid interruption. When the grid return, the transient is smooth as well, as shown in Figure 12 (c) where the currents $i_{LA,1}$, $i_{LA,2}$ and $i_{LA,3}$ do not appear to change significantly. After the grid return, the master synchronizes its reference with the grid. During this time all inverters keep following the reference received by CAN. When an inverter detects that its reference (received or generated) is synchronized with the grid, it switches to the analog bus and it starts to employ the reference from PLL algorithm and synthesizing v_{ABC}^{ref} by ωt_{PLL}.

2) Master Election: The Figure 13 shows the behavior of the data sent by the CAN bus when the master module is shut down, disconnected or suffers a failure. In this case, the previous master (module 1) is shut down and stops sending the reference. The slaves respond by attempting to become the master, sending the message containing its number.

The random candidate for master sends its module number to other inverters, but it is not a master yet. It waits for confirmation from other modules that they accept its lead. In the test shown in Figure 13, module 3 asks to be the master and after three data frames module 2 confirms that module 3 is the new master. This may be observed after the definition of the new master, module 3 starts sending ωt_{CAN} via T_x, module 2 receives the data from R_x and when the transmission finishes module 2 acknowledges the data and sends the acknowledge bit via its T_x to the master (module 3).

V. CONCLUSIONS

This paper proposed an improved master-slave control system for multi-inverter parallel operation. The control is based on a distributed control strategy where the only information shared among the inverters is the voltage reference.

To increase the reliability of this control strategy a redundant communication network was proposed, which ensures proper operation and load sharing during several

different modes of operation, such as: (i) with or without the grid, (ii) transients during a grid interruption or the return of the power and (iii) connection/disconnection and failure of the VSI power modules. The proposed management system guarantees that there is no hierarchy in the network. In the normal mode (with the grid), each inverter employs the analog bus reference as its voltage reference. In the outage mode (without the grid), the inverters use the digital bus reference sent by CAN, which is sent by a master module. If the master is disconnected from the system, another random module becomes the master. Hence, differently from master-slave or central control communication strategies, in this paper it was proposed a novel concept in which all inverters modules are in the same hierarchical level. There is a master module while the others are slaves. When the master is disconnected, hence a random new master is elected in transparent way of load point of view. Both communication systems (analog and digital) work with a high bandwidth, which allows a good performance of the control. The experimental tests have demonstrated that voltage control, the parallelism control and also the proposed communication strategy work successfully. The transition between different operation modes does not significantly affect the load sharing among the parallel connected inverters. Therefore, the proposal system keeps the inverters operating in parallel, with or without the grid, with adequate performance. In the proposed networked control strategy, the system redundancy is improved. The structure of parallel-connected inverters based on the proposed network control system provides an increase in redundancy and reliability which is very attractive for online UPS applications.

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