FPGA-BASED SPACE VECTOR MODULATION OF AN INDIRECT MATRIX CONVERTER

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***Abstract* – The insertion of powers sources onto the grid require an energy processing stage between generator and electrical grid, which adapts amplitude and frequency levels for alternating current (AC) quantities. The Indirect Matrix Converter is a candidate for such operation, although one of the greatest challenges of the topology lies in a way to command the switches while controlling the structure power-flow, as well as the synchronism between source–converter and converter–grid. Hence this paper presents a different view on the converter modelling and proposes a FPGA-based method to perform the Space Vector Modulation (SVM) and synchronism algorithms minimizing the resource consumption, focusing on digital processing algorithms and resource sharing to reduce resource consumption and the number of multipliers employed, ideal for implementation in low-cost FPGAs. Experimental results are shown using a prototype, demonstrating the efficacy of the implementation and verifying the converter behaviour.**

***Keywords* – AC-AC Conversion, FPGA, Indirect Matrix Converter, Matrix Converters.**

NOMENCLATURE

A, B, C	*High-side* phases.
a, b, c	*Low-side* phases.
r	*High-side* subscript.
i	*Low-side* subscript.
$\vec{x}_r$	Vector pertaining to the rectifier stage $\in \mathbb{R}^3$.
$\vec{x}_i$	Vector pertaining to the inverter stage $\in \mathbb{R}^3$.
$\vec{v}_r$	*High-side* converter voltages.
$\vec{v}_i$	*Low-side* converter currents.
$\vec{i}_r$	*High-side* converter voltages.
$\vec{i}_i$	*Low-side* converter currents.
$\vec{u}$	Input voltages.
$\vec{i}^s$	*High-side* voltage source currents.
f_r	*High-side* frequency
f_i	*Low-side* frequency
L_f	*High-side* Inductance
C_f	*High-side* Capacitance
R_f	*High-side* Resistance
L_m	*Low-side* Inductance
R_m	*Low-side* Resistance
s	Switching function.
$\mathbf{s}$	Switching vector.
δ	Averaged switching function.
u_{pn}	Instantaneous virtual DC-link voltage.
i_{pn}	Instantaneous virtual DC-link current.
$\mathbf{T}_M$	Indirect Matrix Converter switching matrix.
$\mathbf{T}_r$	*High-side* switching matrix.
$\mathbf{T}_i$	*Low-side* switching matrix.
T_s	Switching frequency [s].
v_l	Highest amplitude line-to-line voltage.
v_m	Second highest amplitude line-to-line voltage.
m	Modulation Index.
X^{pk}	Electrical quantities amplitude/peak value.
$\tau^i_{1,l}$	Time of application of $\vec{I}_1$ while applying v_l.
$\tau^i_{1,m}$	Time of application of $\vec{I}_1$ while applying v_m.
$\tau^i_{2,l}$	Time of application of $\vec{I}_2$ while applying v_l.
$\tau^i_{2,m}$	Time of application of $\vec{I}_2$ while applying v_m.
A_0, A_1, B_1	IIR filter coefficients.
$\mathbf{A}, \mathbf{B}, \mathbf{E}$	State space matrices.
$\mathbf{Q}$	Auxiliar state space matrix.
$\langle \bullet \rangle_{T_s}$	Average value in a period T_s.

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I. INTRODUCTION

A vision shared by many experts is that future commercial and residential developments will be self-sufficient with respect to energy production, including micro-generaton units in electricity generation power sources. The interface between mechanical parts and electrical quantities is often implemented through electrical generators which employ variable electrical frequency while aiming to increase the process efficiency. In this context, the insertion of such power sources requires an energy processing stage between generator and electrical grid, which adapts amplitude and frequency levels for alternating current (AC) quantities.

The matrix converter is a static power converter able to process directly the AC electric quantities between two distinct AC systems without an intermediary DC stage. The main advantages of such topologies are the increased efficiency of the energy conversion and reduction of weight and volume of the power converter, while maintaining the ability to drain and inject sinusoidal currents for both AC systems.

According to [1], the most desired characteristics of a static power converter interfacing AC voltages and currents (AC–DC–AC, AC–DC–DC–AC, AC–AC) are:

- Low-cost and compact power circuit;
- Synthetization of the output voltage with arbitrary voltage and frequency;
- Input and output currents with a sinusoidal format, i.e., with a low harmonic distortion;
- Operation with a high power factor for any load condition;
- Bidirectional power flux and regeneration capabilities.

The Indirect Matrix Converter (IMC) topology has many different implementations: the traditional IMC [2], [3], the Sparse Matrix Converter [2], the Very Sparse Matrix Converter (VSMC) [4] and the Ultra Sparse Matrix Converter (USMC) [5]. The IMC has the same number of switches of the Conventional Matrix Converter (CMC), while the VSMC uses a different switch realization which reduces the number of switches and the SMC and USMC have a simpler implementation, substituting some switches for diodes while sacrificing the possibility of operating with a bidirectional power flux.

One of the greatest challenges of the topology is the way to command the switches and the control of the structure power-flow, as well as the synchronism of the converter, while reducing the number of resources used by the implementation. Low-cost *Field-Programmable Gate Arrays* (FPGAs) present a reduced number of multipliers and embedded memory.

The aim of this paper is to propose a method to perform the Space Vector Modulation (SVM) and synchronism algorithms while aiming to minimize memory and resource consumption through the use of digital signal processing algorithms and resource sharing while preserving the numerical stability using a FPGA to perform such algorithms.

II. MATRIX CONVERTER DYNAMIC MODELLING

This section describes a mathematical analysis of the indirect matrix converter shown in Figure 1. The topology can be divided into two different stages. The rectifier stage is composed by six four-quadrant switches and presents the same structure as a bidirectional Current Source Inverter (CSI), whereas the inverter stage is composed by six two quadrant switches in a three-phase bridge configuration similar to a Voltage Source Inverter (VSI).

A characteristic of the topology is the possibility to operate with power flux reversibility, i.e, the converter can operate as a voltage *step-down* (*Buck* mode) or as a voltage *step-up* (*Boost* mode), given that the VSI and CSI are also bidirectional. This interpretation can be explored in different applications, such as the following:

- *Buck* mode (Voltage *step-down*): The converter is supplied by a voltage source, and the load have a current source profile. This operation mode is widely used in variable voltage motor drives, as demonstrated in [6]–[8].
- *Boost* mode (Voltage *step-up*): As opposed to the previous mode, the converter is supplied by a current source, and the load demonstrate a voltage source profile. This mode can be used in grid tied applications, where the power flux flows from a variable frequency generator to the grid [3], [9], [10].

A. Switched Model

In this section, a dynamic switched model for the indirect matrix converter is presented. This model consider ideal switches which presents two distinct states: enabled and disabled. The subscript r henceforth denotes variables pertaining to the rectifier stage, and the subscript i to variables belonging to the inverter stage.

The *high-side* and the *low-side* voltage and current vectors can be defined by (1) and (2).

$$\vec{v}_r = \begin{bmatrix} v_A & v_B & v_C \end{bmatrix}^T \quad \vec{i}_r = \begin{bmatrix} i_A & i_B & i_C \end{bmatrix}^T. \tag{1}$$

$$\vec{v}_i = \begin{bmatrix} v_a & v_b & v_c \end{bmatrix}^T \quad \vec{i}_i = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T. \tag{2}$$

Similarly, the voltage and current input vectors and the voltage output vector can be defined by (3) and (4).

$$\begin{aligned} \vec{u}_r &= \begin{bmatrix} u_A & u_B & u_C \end{bmatrix}^T \\ \vec{i}_r^{\,s} &= \begin{bmatrix} i_A^s & i_B^s & i_C^s \end{bmatrix}^T \end{aligned}. \tag{3}$$

$$\vec{u}_i = \begin{bmatrix} u_a & u_b & u_c \end{bmatrix}^T. \tag{4}$$

The IMC model previously presented has twelve ideal switches. According to the switched model based on Figure 1, a switching function s_{kj} can be expressed for the state of each switch S_{kj}, as described by (5), where $k \in \{A,B,C,a,b,c\}$ and $j \in \{p,n\}$.

$$s_{kj} = \begin{cases} 1, & \text{Switch } S_{kj} \text{ enabled} \\ 0, & \text{Switch } S_{kj} \text{ disabled.} \end{cases}. \tag{5}$$

Therefore, it is possible to obtain switching vectors for the rectifier and inverter stage, as defined by (6).

$$\begin{aligned} \mathbf{s}_r &= \begin{bmatrix} s_{Ap} - s_{An} & s_{Bp} - s_{Bn} & s_{Cp} - s_{Cn} \end{bmatrix} \\ \mathbf{s}_i &= \begin{bmatrix} s_{ap} - s_{an} & s_{bp} - s_{bn} & s_{cp} - s_{cn} \end{bmatrix} \end{aligned}. \tag{6}$$

For simplicity, the switching vectors can be redefined as in (7), where $s_k \in \{-1,0,1\}$.

$$\begin{aligned} \mathbf{s}_r &= \begin{bmatrix} s_A & s_B & s_C \end{bmatrix} \\ \mathbf{s}_i &= \begin{bmatrix} s_a & s_b & s_c \end{bmatrix} \end{aligned}. \tag{7}$$

Consequently, the virtual DC-link voltage and current can be described as a function of the switching vectors, as shown in (8).

$$\begin{aligned} u_{pn} &= \mathbf{s}_r \vec{v}_r \\ i_{pn} &= \mathbf{s}_i \vec{i}_i \end{aligned}. \tag{8}$$

Similarly, the the *low-side* voltage and the *high-side* current vectors can be expressed by (9).

$$\begin{aligned} \vec{v}_i &= \mathbf{s}_i^T u_{pn} \\ \vec{i}_r &= \mathbf{s}_r^T i_{pn} \end{aligned}. \tag{9}$$

The *low-side* voltage and the *high-side* current vectors can be expressed in terms of the switching vectors pertaining to both rectifier and inverter stages by substituting (8) in (9), according to (10).

$$\begin{aligned} \vec{v}_i &= \mathbf{s}_i^T \mathbf{s}_r \vec{v}_r \\ \vec{i}_r &= \mathbf{s}_r^T \mathbf{s}_i \vec{i}_i \end{aligned}. \tag{10}$$

It is possible to obtain a switched transformation matrix for the indirect matrix converter, which directly relates voltage and current input and output, defined by (11).

$$\mathbf{T}_M = \mathbf{s}_i{}^T \mathbf{s}_r = \begin{bmatrix} s_a s_A & s_a s_B & s_a s_C \\ s_b s_A & s_b s_B & s_b s_C \\ s_c s_A & s_c s_B & s_c s_C \end{bmatrix}. \tag{11}$$

The modelling can then be divided between the rectifier and inverter stages. Since equations (10) and (11) describe a relation between the two stages, it is possible to simplify the switched model shown in Figure 1 using controlled voltage and current sources, as illustrated in Figure 2.

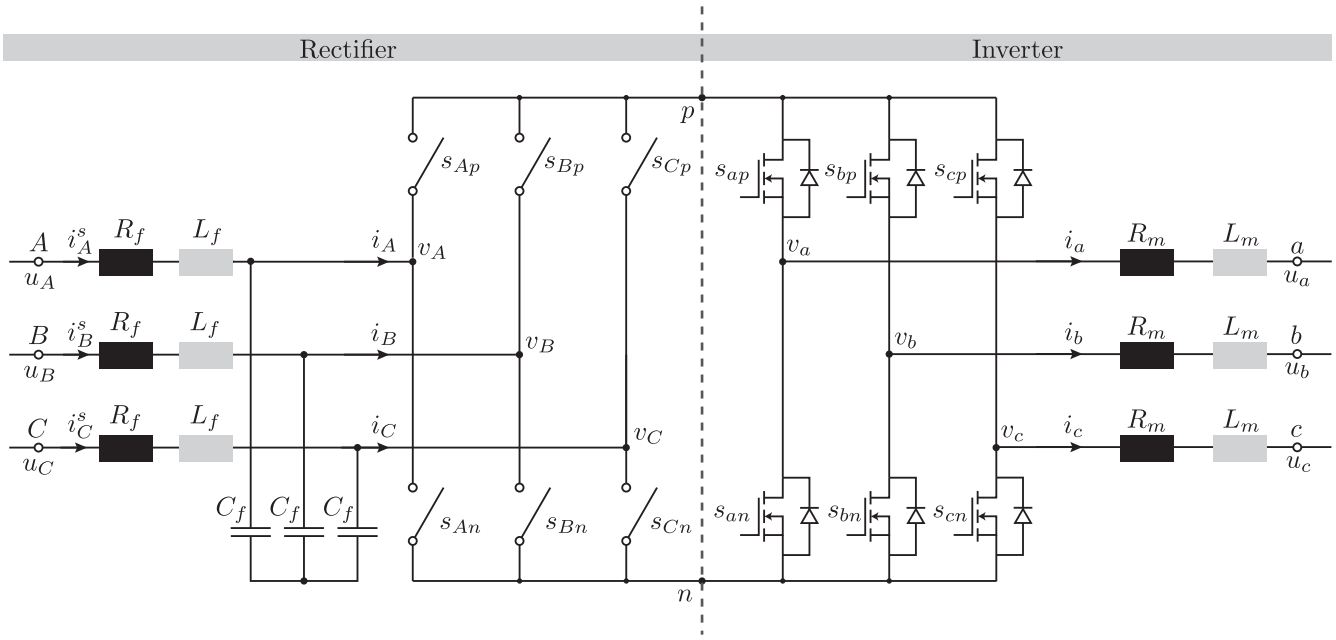

Fig. 1. Inverse matrix converter switched model, composed by twelve ideal switches, as well as filtering elements. The *high-side* voltage is defined by $\{u_A, u_B, u_C\}$ and the *low-side* voltage is defined by $\{u_a, u_b, u_c\}$.

Therefore, the system can be described by two separated state-space representation. The output voltages $\{u_a, u_b, u_c\}$ can be described according to the different load characteristics. For example, if a motor is connected to the *low-side*, its voltage equations can be coupled into the model. For a resistive load, the resistance value can be grouped with R_m and the voltage vector $\vec{u}_i$ is null valued.

Since the rectifier stage voltage vector $\vec{v}_r$ and the inverter stage current vector $\vec{i}_i$ are linearly dependent, two new switching matrices can be defined according to equation (12), resulting in (13). Rectifier voltage v_C and inverter current i_c can be expressed as a linear combination of the expressed vectors, hence the suppression in the new set of equations.

$$\mathbf{T}_r = \begin{bmatrix} s_a s_A - s_a s_C & s_a s_B - s_a s_C \\ s_b s_A - s_b s_C & s_b s_B - s_b s_C \\ s_c s_A - s_c s_C & s_c s_B - s_c s_C \end{bmatrix}. \qquad (12)$$
$$\mathbf{T}_i = \begin{bmatrix} s_a s_A - s_c s_A & s_b s_A - s_c s_A \\ s_a s_B - s_c s_B & s_b s_B - s_c s_B \end{bmatrix}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \mathbf{T}_r \begin{bmatrix} v_A \\ v_B \end{bmatrix}, \quad \begin{bmatrix} i_A \\ i_B \end{bmatrix} = \mathbf{T}_i \begin{bmatrix} i_a \\ i_b \end{bmatrix}. \qquad (13)$$

1) Rectifier Stage: The rectifier stage can be modelled as a fourth order system with three inputs and two state versus inputs. Since the inputs versus states given by the controlled current sources are coupled with the inverter stage, they are separated for a partial representation of the system, resulting in a time invariant system representation. The chosen state-space state variables, inputs state x input vector is demonstrated in (14).

$$\mathbf{x}_r = \begin{bmatrix} i_A^s & i_B^s & v_A & v_B \end{bmatrix}^T$$
$$\mathbf{u}_r = \vec{u}_r = \begin{bmatrix} u_A & u_B & u_C \end{bmatrix}^T. \qquad (14)$$
$$\mathbf{w}_r = \begin{bmatrix} i_A & i_B \end{bmatrix}^T$$

From the circuit shown in Figure 2, it is possible to obtain an expression for the inductor L_f voltages for phases pertaining to the set $\{A, B\}$, as demonstrated by (15).

$$\begin{bmatrix} v_{L_f,A} \\ v_{L_f,B} \end{bmatrix} = \begin{bmatrix} u_{AB} \\ u_{BC} \end{bmatrix} - \begin{bmatrix} v_{AB} \\ v_{BC} \end{bmatrix} - R_f \begin{bmatrix} i_A^s \\ i_B^s \end{bmatrix} + R_f \begin{bmatrix} i_B^s \\ i_C^s \end{bmatrix} + \begin{bmatrix} v_{L_f,B} \\ v_{L_f,C} \end{bmatrix}. \qquad (15)$$

Similarly, it is possible to obtain an expression for the capacitor C_f current, according to (16).

$$\vec{i}_{C_f,r} = \vec{i}_r^s - \vec{i}_r. \qquad (16)$$

From the circuit shown in Figure 2, it is possible to conclude that some voltages and currents of magnetic devices are linearly dependent. Such dependency is demonstrated in (17).

$$\begin{aligned} i_C^s &= -i_A^s - i_B^s \\ i_C &= -i_A - i_B \\ v_C &= -v_A - v_B \end{aligned}. \qquad (17)$$

Therefore, the rectifier stage circuit can be expressed by the state-space model described by (18), with state-space matrices defined by (19).

$$\dot{\mathbf{x}}_r = \mathbf{A}_r \mathbf{x}_r + \mathbf{B}_r \mathbf{u}_r + \mathbf{E}_r \mathbf{w}_r. \qquad (18)$$

$$\mathbf{A}_r = \begin{bmatrix} -\frac{R_f}{L_f}\mathbf{I}_2 & -\frac{1}{L_f}\mathbf{I}_2 \\ \frac{1}{C_f}\mathbf{I}_2 & \mathbf{O}_{2x2} \end{bmatrix} \quad \mathbf{B}_r = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \frac{1}{3L_f}. \qquad (19)$$
$$\mathbf{E}_r = \begin{bmatrix} \mathbf{O}_{2x2} \\ -\mathbf{I}_2 \end{bmatrix} \frac{1}{C_f}$$

2) Inverter Stage: Similarly to the methodology previously presented, a circuit representing the inverter stage is also presented in Figure 2. Furthermore, the rectifier stage can be modelled as a second order system with three inputs and three state versus inputs, which are coupled with the rectifier stage as shown previously. The chosen state-space state

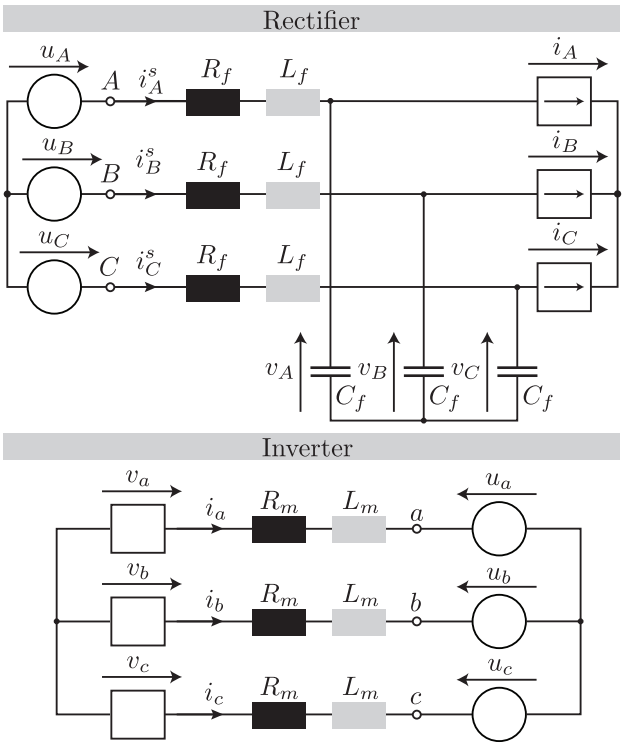

Fig. 2. Switched model circuit. The switched transformation matrix describes the coupling between both rectifier and inverter stages.

variables and stage input vector, as well as the state x input, are described by (20).

$$\begin{aligned} \mathbf{x}_i &= \begin{bmatrix} i_a & i_b \end{bmatrix}^T \\ \mathbf{u}_i = \vec{u}_i &= \begin{bmatrix} u_a & u_b & u_c \end{bmatrix}^T. \\ \mathbf{w}_i = \vec{v}_i &= \begin{bmatrix} v_a & v_b & v_c \end{bmatrix}^T \end{aligned} \tag{20}$$

The inductor voltage can be expressed by (21).

$$\begin{bmatrix} v_{L_m,a} \\ v_{L_m,b} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix} (\vec{v}_i - \vec{u}_i) - R_m \begin{bmatrix} i_a - i_b \\ i_b - i_c \end{bmatrix} + \begin{bmatrix} v_{L_m,b} \\ v_{L_m,c} \end{bmatrix}. \tag{21}$$

Furthermore, the phase c current can be expressed as a linear combination of the currents pertaining to the set $\{a,b\}$, according to equation.

$$i_c = -i_a - i_b. \tag{22}$$

Therefore, the inverter stage state-space model can be described by (23), with state-space matrices defined by (24).

$$\dot{\mathbf{x}}_i = \mathbf{A}_i \mathbf{x}_i + \mathbf{B}_i \mathbf{u}_i + \mathbf{E}_i \mathbf{w}_i. \tag{23}$$

$$\begin{aligned} \mathbf{A}_i &= -\tfrac{R_m}{L_m} \mathbf{I}_2 \qquad \mathbf{B}_i = \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \end{bmatrix} \tfrac{1}{3L_m} \\ \mathbf{E}_i &= \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix} \tfrac{1}{3L_m} \end{aligned} \tag{24}$$

B. Averaged Model

From the switched state-space model, it is possible to obtain an averaged model by defining an averaged switching function as in (25), where T_s is the switching time and $i \in \{A,B,C,a,b,c\}$. It is important to notice that the averaged switching function is bounded, as $\delta_i \in [-1,1]$.

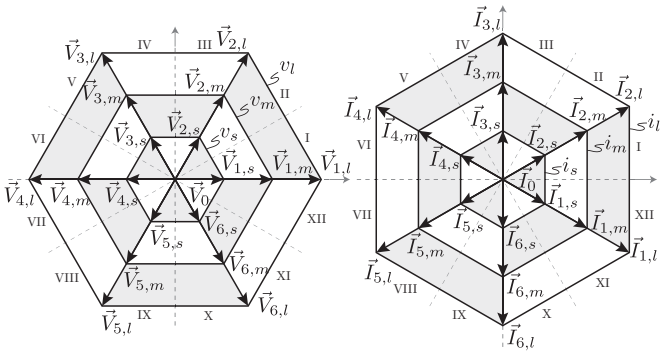

Fig. 3. Indirect matrix converter space-vector map, demonstrating the seventy-two possible switching states.

$$\delta_i = \left\langle s_{ip} - s_{in} \right\rangle_{T_s} = \int_t^{t+T_s} s_{ip}(t) - s_{in}(t) \mathrm{d}t. \tag{25}$$

Therefore, it can be shown that the whole system can be described by (26) [11], where $\mathbf{Q}_{ij}^{r,i}$ are the elements of matrices $\mathbf{Q}^{r,i}$ defined in (27). It is possible to notice that it is hard to find an equilibrium point for the system, as $\mathbf{Q}^{r,i}$ are time variant with a complex dynamic. The following sections present a modulation strategy for the IMC, while focusing on the practical implementation.

III. STATIC ANALYSIS

The static model of the IMC decompose the converter presents a different analysis for the two stages, hence obtaining the vector map shown in Figure 3. The switching state for the rectifier and inverter stage are presented in Table I and Table II, respectively, assuming rectifier stage voltage and inverter stage current vector given by (28).

$$\begin{aligned} \vec{v}_r &= V_r^{pk} \begin{bmatrix} \cos(\varphi_r) & \cos(\varphi_r - 2\pi/3) & \cos(\varphi_r + 2\pi/3) \end{bmatrix}^T \\ \vec{i}_i &= I_i^{pk} \begin{bmatrix} \cos(\varphi_i) & \cos(\varphi_i - 2\pi/3) & \cos(\varphi_i + 2\pi/3) \end{bmatrix}^T \\ \varphi_{r,i} &= \omega_{r,i} t + \theta_{r,i} \end{aligned} \tag{28}$$

A. Modulation Strategy

Carrier-based modulation strategies have been explored by a few authors in [12]–[14] for operation under diverse conditions. This type of modulation uses carriers and pulse-width modulators to generate an averaged switching matrix with a pre-determined behaviour. The main advantage of carrier-based strategies is the reduced computational burden for DSP implementation. However, such strategies sometimes do not present some characteristics inherent to Space Vector Modulation (SVM), such as the possibility to operate with Zero-Current Switching (ZCS) or Zero-Voltage Switching (ZVS), or aim to present similar characteristics to some SVM strategies. The greatest advantage of SVM is the possibility to synthesize switching states and sequences which are non-trivial when compared to carrier-based strategies.

Also, some SVM modulation strategies do not require multi-step commutation for the rectifier stage, which usually adds another layer of complexity to the implementation. However, multi-step commutation for the IMC is much simpler than on the CMC, since the instantanous current

$$\begin{bmatrix} \langle \dot{i}_A^s(t)\rangle_{T_s} \\ \langle \dot{i}_B^s(t)\rangle_{T_s} \\ \langle \dot{v}_A(t)\rangle_{T_s} \\ \langle \dot{v}_B(t)\rangle_{T_s} \\ \langle \dot{i}_a(t)\rangle_{T_s} \\ \langle \dot{i}_b(t)\rangle_{T_s} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 & 0 & -\frac{1}{C_f}\mathbf{Q}_{11}^i & -\frac{1}{C_f}\mathbf{Q}_{12}^i \\ 0 & \frac{1}{C_f} & 0 & 0 & -\frac{1}{C_f}\mathbf{Q}_{21}^i & -\frac{1}{C_f}\mathbf{Q}_{22}^i \\ 0 & 0 & \frac{1}{3L_m}\mathbf{Q}_{11}^r & \frac{1}{3L_m}\mathbf{Q}_{12}^r & -\frac{R_m}{L_m} & 0 \\ 0 & 0 & \frac{1}{3L_m}\mathbf{Q}_{21}^r & \frac{1}{3L_m}\mathbf{Q}_{22}^r & 0 & -\frac{R_m}{L_m} \end{bmatrix} \begin{bmatrix} \langle i_A^s(t)\rangle_{T_s} \\ \langle i_B^s(t)\rangle_{T_s} \\ \langle v_A(t)\rangle_{T_s} \\ \langle v_B(t)\rangle_{T_s} \\ \langle i_a(t)\rangle_{T_s} \\ \langle i_b(t)\rangle_{T_s} \end{bmatrix} + \begin{bmatrix} \frac{2}{L_f} & -\frac{1}{L_f} & -\frac{1}{L_f} & 0 & 0 & 0 \\ -\frac{1}{L_f} & \frac{2}{L_f} & -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{2}{L_m} & \frac{1}{L_m} & \frac{1}{L_m} \\ 0 & 0 & 0 & \frac{1}{L_m} & -\frac{2}{L_m} & \frac{1}{L_m} \end{bmatrix} \begin{bmatrix} \langle u_A(t)\rangle_{T_s} \\ \langle u_B(t)\rangle_{T_s} \\ \langle u_C(t)\rangle_{T_s} \\ \langle u_a(t)\rangle_{T_s} \\ \langle u_b(t)\rangle_{T_s} \\ \langle u_c(t)\rangle_{T_s} \end{bmatrix}. \tag{26}$$

$$\mathbf{Q}^i = \begin{bmatrix} \delta_a\delta_A - \delta_c\delta_A & \delta_b\delta_A - \delta_c\delta_A \\ \delta_a\delta_B - \delta_c\delta_B & \delta_b\delta_B - \delta_c\delta_B \end{bmatrix}, \quad \mathbf{Q}^r = \begin{bmatrix} (2\delta_a - \delta_b - \delta_c)(\delta_A - \delta_C) & (2\delta_a - \delta_b - \delta_c)(\delta_B - \delta_C) \\ (2\delta_b - \delta_a - \delta_c)(\delta_A - \delta_C) & (2\delta_b - \delta_a - \delta_c)(\delta_B - \delta_C) \end{bmatrix}. \tag{27}$$

TABLE I
Rectifier Stage (CSI) Switching States

Type	Vector $\vec{I}_k$	S_{Ap} S_{An}	S_{Bp} S_{Bn}	S_{Cp} S_{Cn}	i_A	i_B	i_C	$\|\vec{i}_i\|$	$\angle\vec{i}_i$	u_{pn}
Active	$\vec{I}_1$	1 0	0 1	0 0	i_{pn}	$-i_{pn}$	0	$\frac{2}{\sqrt{3}}i_{pn}$	$-\frac{\pi}{6}$	v_{AB}
	$\vec{I}_2$	1 0	0 0	0 1	i_{pn}	0	$-i_{pn}$	$\frac{2}{\sqrt{3}}i_{pn}$	$\frac{\pi}{6}$	$-v_{CA}$
	$\vec{I}_3$	0 0	1 0	0 1	0	i_{pn}	$-i_{pn}$	$\frac{2}{\sqrt{3}}i_{pn}$	$\frac{\pi}{2}$	v_{BC}
	$\vec{I}_4$	0 1	1 0	0 0	$-i_{pn}$	i_{pn}	0	$\frac{2}{\sqrt{3}}i_{pn}$	$\frac{5\pi}{6}$	$-v_{AB}$
	$\vec{I}_5$	0 1	0 0	1 0	$-i_{pn}$	0	i_{pn}	$\frac{2}{\sqrt{3}}i_{pn}$	$-\frac{5\pi}{6}$	v_{CA}
	$\vec{I}_6$	0 0	0 1	1 0	0	$-i_{pn}$	i_{pn}	$\frac{2}{\sqrt{3}}i_{pn}$	$-\frac{\pi}{2}$	$-v_{BC}$
Null	$\vec{I}_7$	1 1	0 0	0 0	–	–	–	0	–	0
	$\vec{I}_8$	0 0	1 1	0 0	–	–	–	0	–	0
	$\vec{I}_9$	0 0	0 0	1 1	–	–	–	0	–	0

TABLE II
Inverter Stage (VSI) Switching States

Type	Vector $\vec{I}_k$	S_{ap} S_{an}	S_{bp} S_{bn}	S_{cp} S_{cn}	v_a	v_b	v_c	$\|\vec{v}_r\|$	$\angle\vec{v}_r$	i_{pn}
Active	$\vec{V}_1$	1 0	0 1	0 1	u_{pn}	$-u_{pn}$	$-u_{pn}$	$\frac{2}{3}u_{pn}$	0	i_a
	$\vec{V}_2$	1 0	1 0	0 1	u_{pn}	u_{pn}	$-u_{pn}$	$\frac{2}{3}u_{pn}$	$\frac{\pi}{3}$	$-i_c$
	$\vec{V}_3$	0 1	1 0	0 1	$-u_{pn}$	u_{pn}	$-u_{pn}$	$\frac{2}{3}u_{pn}$	$\frac{2\pi}{3}$	i_b
	$\vec{V}_4$	0 1	1 0	1 0	$-u_{pn}$	u_{pn}	u_{pn}	$\frac{2}{3}u_{pn}$	$-\pi$	$-i_a$
	$\vec{V}_5$	0 1	0 1	1 0	$-u_{pn}$	$-u_{pn}$	u_{pn}	$\frac{2}{3}u_{pn}$	$-\frac{2\pi}{3}$	i_c
	$\vec{V}_6$	1 0	0 1	1 0	u_{pn}	$-u_{pn}$	u_{pn}	$\frac{2}{3}u_{pn}$	$-\frac{\pi}{3}$	$-i_b$
Null	$\vec{V}_7$	1 0	1 0	1 0	u_{pn}	u_{pn}	u_{pn}	0	–	0
	$\vec{V}_8$	0 1	0 1	0 1	$-u_{pn}$	$-u_{pn}$	$-u_{pn}$	0	–	0

values are known for all the switches. *Dead-time* and *overlap-time* are still required for a safe converter operation.

Since the matrix converter has seventy-two possible switching states, space-vector modulation can be quite complex, since many different combinations of vectors are possible. The High-Voltage Zero-Current Switching (HVZCS) modulation scheme consists in applying the large and medium amplitude voltage vectors $\{v_l, v_m\}$ in the rectifier stage, limiting the number of possible vectors, as shown in Figure 4. The virtual DC link voltage is then formed by segments of line-to-line voltages v_l and v_m. The sequence in which these voltages are applied to the output does not alter the average value of the virtual voltage, hence a scheme illustrated by Figure 5 can be employed to minimize switching losses on the rectifier stage.

A modulation index directly tied to the converter gain can be expressed by (29). From this equation, it is possible to infer that the maximum converter gain, i.e, the maximum ratio between rectifier and inverter stage voltage amplitudes is approximately equal to 0.866 for *Buck* mode operation. An immediate implication is that this modulation scheme cannot be used to drive a three-phase motor with a rated voltage equal to the input voltage.

$$m = \frac{2}{\sqrt{3}}\frac{V_i^{pk}}{V_r^{pk}} \in [0,1]. \tag{29}$$

Using the modulation index defined in (29), the vector times

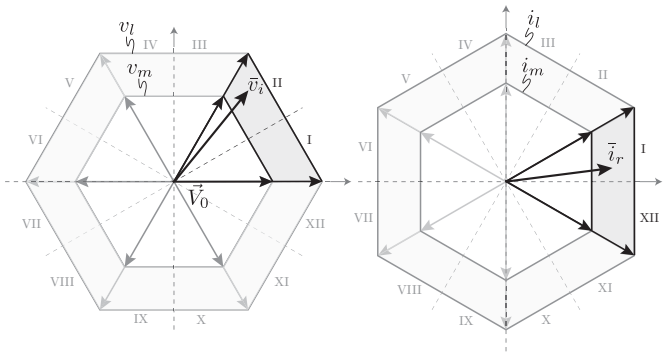

Fig. 4. Inverter and rectifier stage space vector map for different for the High Voltage Zero Current Switching (HVZCS) modulation.

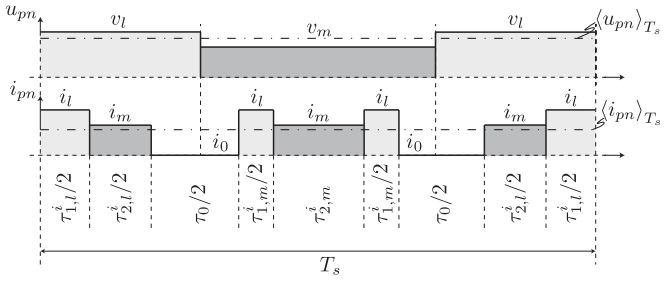

Fig. 5. High Voltage Zero switching commutation (HVZCS) using a nine-segment modulation scheme.

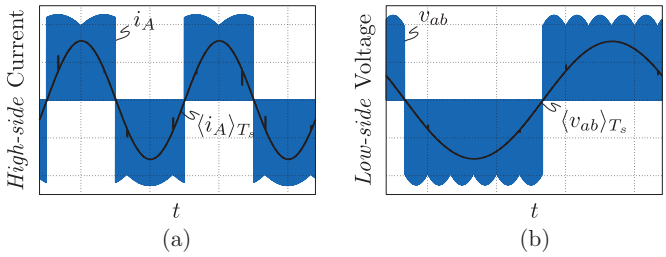

Fig. 6. Electrical quantities waveform for HVZCS modulation scheme for a modulation index of 0.8. (a) Rectifier stage current. (b) Inverter stage line-to-line voltage.

can be calculated according to (30) [4].

$$\begin{aligned}
\tau^i_{1,l} &= mT_s \cos\left(\varphi_r - \tfrac{\pi}{3}\right)\cos\left(\varphi_i + \tfrac{\pi}{6}\right)\\
\tau^i_{1,m} &= mT_s \cos\left(\varphi_r + \tfrac{\pi}{3}\right)\cos\left(\varphi_i + \tfrac{\pi}{6}\right)\\
\tau^i_{2,l} &= mT_s \cos\left(\varphi_r - \tfrac{\pi}{3}\right)\sin\left(\varphi_i\right)\\
\tau^i_{2,m} &= mT_s \cos\left(\varphi_r + \tfrac{\pi}{3}\right)\sin\left(\varphi_i\right)
\end{aligned} \quad . \tag{30}$$

The rectifier stage current and inverter stage voltage waveforms are shown in Figure 6 for a modulation index of 0.8, which shows the capability of the converter to synthesize sinusoidal electrical quantities with arbitrary frequency and amplitude.

IV. FPGA IMPLEMENTATION

Traditionally, modulation strategies and algorithms necessary for the operation of power converters are implemented using Digital Signal Processors (DSPs), as function libraries, look-up tables and Floating Point Units (FPUs) generally facilitate the implementation of such algorithms. However, more complex power converters might demand the use of an FPGA allied with the DSP, especially for space-vector modulation techniques and the capability to drive multiple switches. The communication between DSP–FPGA is usually implemented through SPI protocols, which are slow and very susceptible to external noise, reducing the converter reliability, as well as increasing the computational time.

One alternative is the use of System-on-a-Chip (SoC) implementations which have a microprocessor and a FPGA embedded on the same chip, enabling a parallel communication, albeit increasing the cost. Another alternative is to directly implement the algorithms in the FPGA, which usually represents a complex implementation while eliminating the need for a digital processor. This work aims to develop such solution, while aiming to reduce the resource usage of the FPGA. However, there is a need to develop some ideas of auxiliary algorithms to perform basic tasks, such as the calculation of trigonometric functions.

A. CORDIC Algorithm

The CORDIC (COrdinate Rotation DIgital Computer) is a digital signal processing algorithm which enables the implementation of hyperbolic and trigonometric functions without the use of long look-up tables, multipliers and dividers. This method consists of adders and rotations, presenting an extremely fast and simple FPGA implementation, ideal for low-cost solutions. This algorithm was initially proposed by J. Volder in 1959 [15], and since then has suffered a few modifications. However, the main idea is to perform a series of r vector rotations to obtain sine and cosine functions. The algorithm is described by (31), and further developed in Algorithm 1 [11].

$$\begin{aligned}
\vec{v}_N = \begin{bmatrix} x_N \\ y_N \end{bmatrix} &= k_N \left(\prod_{i=0}^{N} \begin{bmatrix} 1 & -\sigma_i 2^{-i} \\ \sigma_i 2^{-i} & 1 \end{bmatrix} \right) \begin{bmatrix} x_0 \\ y_0 \end{bmatrix} \\
z_N &= z_0 - \sum_{i=0}^{N} \sigma_i \theta_i, \quad \sigma_i = \operatorname{sgn}(z_{i-1})
\end{aligned} \quad . \tag{31}$$

A single pipelined CORDIC algorithm with a multiplexed input was implemented to perform the trigonometric functions for (30), as well as other functions to adequately operate the IMC, as further discussed.

B. Phase-Locked Loop

Phase-Locked Loops are synchronism algorithms originated in communication theory and are widely used in Power Electronics in grid-tied connections. These algorithms aim to estimate frequency and phase of electrical quantities, and are widely used in grid tied applications. There is a wide range of different strategies, although most follow a generic structure.

As previously discussed, the use of such algorithms are also fundamental for the correct operation of the indirect matrix converter, as the presented modulation strategies are dependent on the estimated phase to accurately synthesize the electric quantities. Therefore, a qPLL [16] unit was

implemented to accurately estimate the electric quantities phase for the SVM time calculation for both rectifier and inverter stages.

The implemented algorithm follows the block diagram described in Figure 7, where the constants $\{A_0, A_1, B_1\}$ are the coefficients of a first-order IIR line filter. A single PLL unit was implemented for two angle estimations, and the algorithm uses the same CORDIC unit as the SVM, hence the need for a Finite State Machine to control the design flow, as discussed later in this paper.

C. Finite-State Machine

As previously discussed, the correct operation of the IMC depends on an accurate estimation of the electric quantities phase, since the converter performs an interface between two distinct AC systems. Therefore, two phase-locked loop algorithm structures are hence used to estimate the rectifier stage voltage and inverter stage current phases. Since there is no need to estimate both angles at the same time using paralleled structures, a finite-state machine can be implemented to use the same structure for both estimations, which then occur sequentially.

After estimating the phase of electrical quantities in both rectifier and inverter stages, the vector times for the space-vector modulation must be calculated. The calculation of the vector times depend on the calculation of trigonometric functions and a pulse-width modulator to generate the nine-segment pattern previously presented. Since the vector time calculation uses the result of the PLL phase estimation, another finite-state machine must be implemented to manage the data flow. Since a CORDIC algorithm is already used in the PLL structure, the vector times are calculated using the same structure. The implementations are based on the Altera Cyclone IV EP4CE22F17C6N FPGA, which is present on the Terasic Cyclone IV DE0-Nano Development Kit. The voltage and current acquisitions were performed using a Texas Instruments TMS320F28335 Microcontroller, which communicates with the FPGA through a SPI interface. The DSP was only used for these acquisitions. A flowchart of the

Algorithm 1 Fixed-Point CORDIC Algorithm

Input: Initial Vector Coordinates $\{x_0, y_0\}$, Initial Angle z_0, Rotation Angles $\{\theta_0, \ldots, \theta_N\}$
Output: Output Vector Coordinates $\{v_0, v_1\}$, Output Angle z
$\theta \leftarrow \{\theta_0, \ldots, \theta_N\}$
$v \leftarrow \{x_0, y_0\}$
$z \leftarrow z_0$
for $i \leftarrow 0$ **to** N **do**
    $w \leftarrow v$
    if rotation mode **then**
        $\sigma \leftarrow \mathrm{sgn}(z_0)$
    else if vectoring mode **then**
        $\sigma \leftarrow -\mathrm{sgn}(w_0 w_1)$
    end if
    $v_0 \leftarrow w_0 - \sigma(w_1 >> i)$
    $v_1 \leftarrow w_1 + \sigma(w_0 >> i)$
    $z \leftarrow z - \sigma\theta_i$
end for

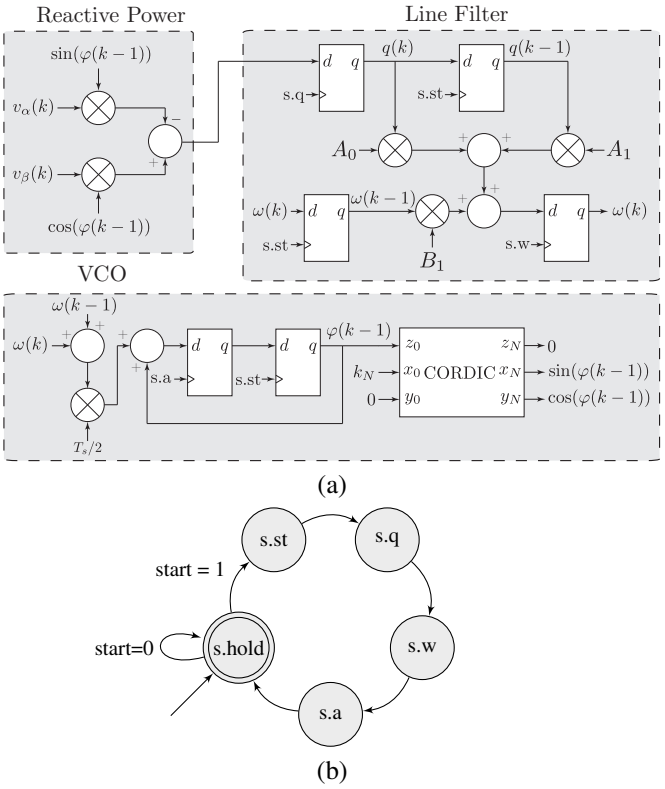

Fig. 7. (a) Register-Transfer Logic FPGA implementation of a qPLL using CORDIC. (b) Finite state machine of the proposed implementation.

implementation is presented in Figure 8.

The calculated time values are then modulated through a pulse-width modulator, generating a switching vector state, which is then translated into a switching signal through a decoder. The generated pulses are presented in Figure 9, and experimental results with parameters given by Table III are presented in Figure 10, demonstrating the functionality of the proposed implementation.

V. CONCLUSIONS

A mathematical model for the indirect matrix converter was obtained, and the state-space matrix for the complete system demonstrates a very non-linear behaviour, proving hard to

TABLE III
Experimental Result Parameters

Parameter	Symbol	Value
Modulation Strategy	–	HVZCS
Modulation index	m	0.8
High-side RMS phase voltage	V_r^{rms}	127 V
Low-side RMS phase voltage	V_i^{rms}	88 V
High-side frequency	f_r	60 Hz
Low-side frequency	f_i	50 Hz
High-side Inductance	L_f	250 μH
High-side Capacitance	C_f	16 μF
High-side Resistance	R_f	10 mΩ
Low-side Inductance	L_m	750 μH
Low-side Resistance	R_m	50 Ω (Y)
Switching Frequency	f_s	24.424 kHz

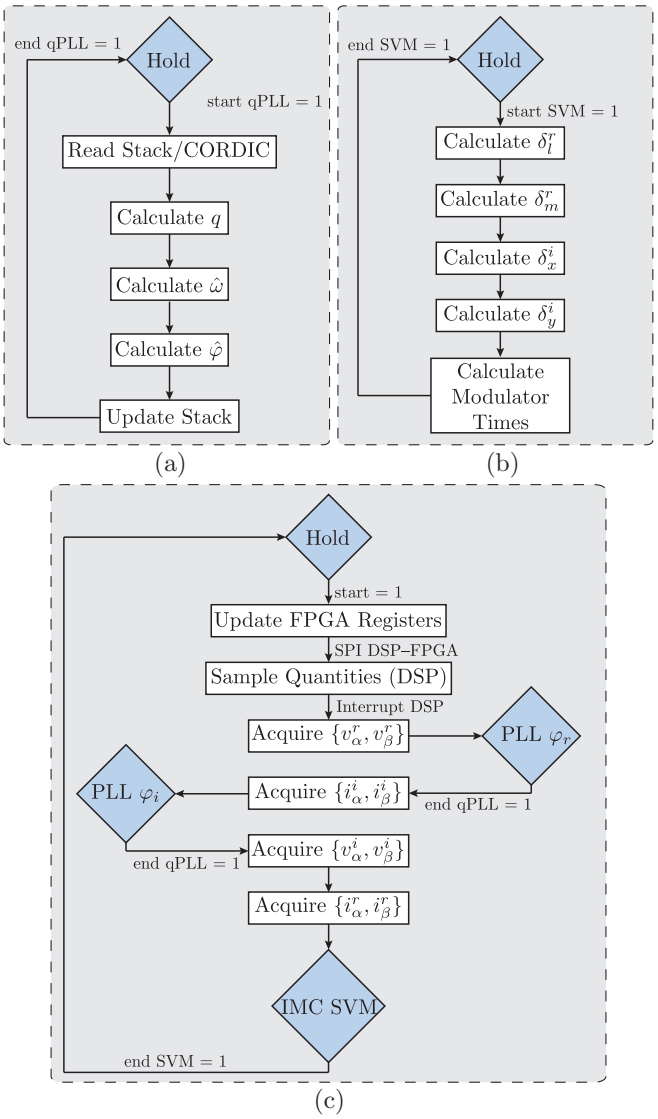

Fig. 8. Flowchart of the State Machine for the (a) PLL algorithm. (b) SVM time calculation (c) General finite-state machine behaviour.

select a single operation point for a linearization. The design of a linear controller might prove to be quite difficult, since the model does not present an equilibrium point. The behaviour of linear controllers are also hindered for non-linear loads. Therefore, many non-linear approaches are currently being studied to solve some of the converter problems, as well as guaranteeing a safe operation under grid faults.

A FPGA implementation of the modulation and synchronism strategies were proposed and verified experimentally. A reduced resource usage implementation was discussed, as many of the design structures were shared by different algorithms. The main disadvantage is the complexity of the finite state machine implemented to control the design behaviour, increasing the computational time. However, the execution time of the proposed strategy is much lower than the design constraints set by the switching frequency. Such implementation has a high sequential design flow, which tends towards the reduced resource usage based on a trade-off between using the FPGA capabilities and reducing the area of the design. An experimental result was

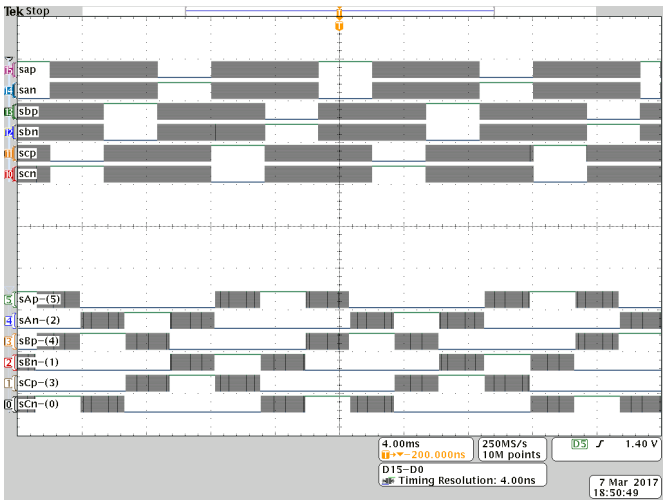

Fig. 9. Experimental result of the HVZCS modulation scheme pulses implementation for the switches of the rectifier and inverter stage. Channels D0–D7 show the switching signals for the rectifier stage, while Channels D10–D15 show the switching signals for the inverter stage.

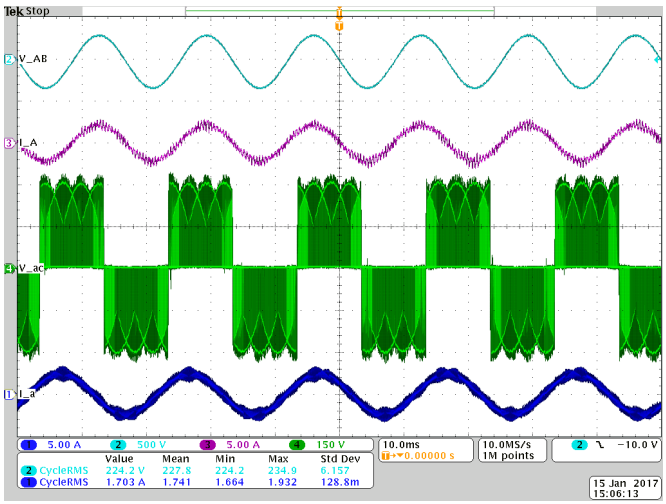

Fig. 10. Experimental result of an Indirect Matrix Converter operating in *Buck* mode with parameters given by Table III.

presented, demonstrating the modulation implementation and verifying the behaviour of the converter.

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