PWM CURRENT-SOURCE CONVERTER WITH DEADBEAT CONTROL

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***Abstract* - Current-source PWM converters are applied in high power electric drives and are proposed for HVDC (high voltage direct current) transmission systems tapping and for energy storage superconducting inductor systems.**
This paper proposes a current source inverter system for feeding an isolated three-phase load (no local power generation) with mains frequency (60 or 50 Hz) at MW power level from a DC line with current source characteristic. The converter is implemented with Graetz bridge topology, employing self-commutated electronic switches (GTOs, IGBTs etc.). The deadbeat controller is chosen for the converter, and its characteristics for this application are analyzed. The PWM modulation method is chosen to meet the controller demands. The PWM logic does comparisons and decisions in real time, not employing look-up tables.
System performance was measured and validated by the PSCAD/EMTDC™ electromagnetic transients simulation software. Linear (balanced and unbalanced) and non-linear loads were employed, in steady state and transient conditions.
The solution presented has its performance dictated by the switching frequency (hundreds of Hz) and voltage ripple at the AC side. The first limitation has technological characteristic, with satisfactory solution at mid term. The second limitation, as well as the first, has solution employing multiconverter configurations, for which simulation results are also presented in this paper.

1. INTRODUCTION

Current-source PWM converters are applied in high power electric drives [1] and are proposed for HVDC (high voltage direct current) transmission systems tapping [2] and energy storage superconducting systems [3][4].

This paper proposes a current source inverter system for feeding a isolated three-phase load (no local power generation) with mains frequency (60 or 50 Hz) at MW power levels from a DC source with current source characteristic. The converter topology is a Graetz bridge employing current-unidirectional, voltage bi-directional electronic switches (GTOs, IGBTs etc.).

The deadbeat controller is chosen for the converter, and its characteristics for the application are analyzed. The PWM modulation method [5] is chosen to meet the controller demands. The PWM logic does comparisons and decisions in real time, not employing look-up tables.

System performance was measured and validated by the PSCAD/EMTDC™ electromagnetic transients simulation software [6]. Cases with linear (balanced and unbalanced) and non-linear loads were simulated successfully, in steady state and transient conditions.

The solution presented has its performance dictated by the switching frequency (hundreds of Hz) and voltage ripple at the AC side. The first limitation has technological characteristic, with satisfactory solution at mid term. The second limitation, as well as the first, has solution employing multiconverter configurations, for which simulation results are also presented in this work.

2. SYSTEM AND CONVERTER

The adopted converter topology is a Graetz bridge, shown in Fig. 2.1(a). In order to provide a current path in parallel with the AC load, shunt capacitors are connected at the AC side. They also act as high pass filters for the PWM carrier frequency, resulting in sinusoidal voltages at the AC side.

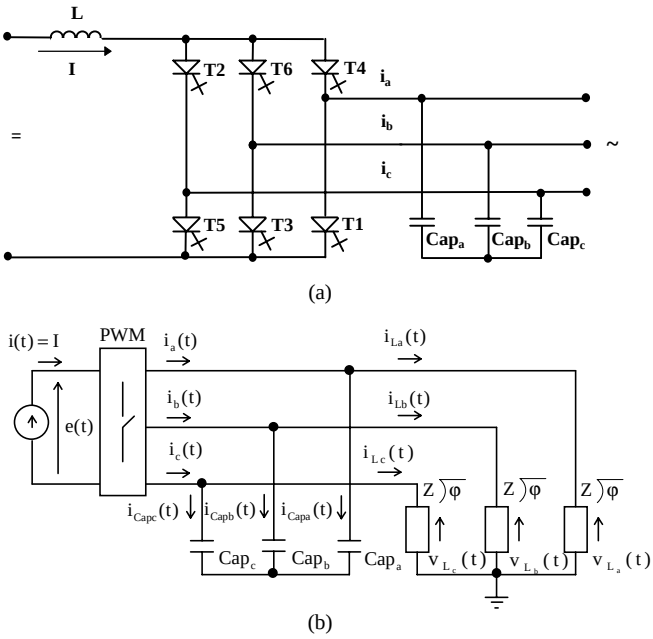

Fig. 2.1: (a) Graetz bridge converter with DC current source. The GTOs represent generic unidirectional current, self-commutated electronic switches (GTOs, IGBTs etc.). (b) Equivalent circuit with instantaneous values for DC/AC converter (PWM block), capacitors and load.

Static equations relate values of AC and DC sides, and are obtained with the equivalent circuit of Fig. 2.1(b). The switched converter, represented by the PWM block is fed by the constant current $i(t)=I$, and generates three currents i_a, i_b and i_c. Load is represented by $Z\angle\varphi$ impedances. Instantaneous average value concept is adopted in order to simplify modeling, taking aside switching effects. It is equivalent to consider PWM modulation frequency near infinite. The instantaneous average value of a voltage v is represented here by $\bar{v}$.

Instantaneous average voltage value at DC side and converter active power [5] are given by (2.1) and (2.2).

$$\bar{e}(t) = \frac{3}{2} \cdot M \cdot V_m \cdot \cos\varphi = E \qquad (2.1)$$

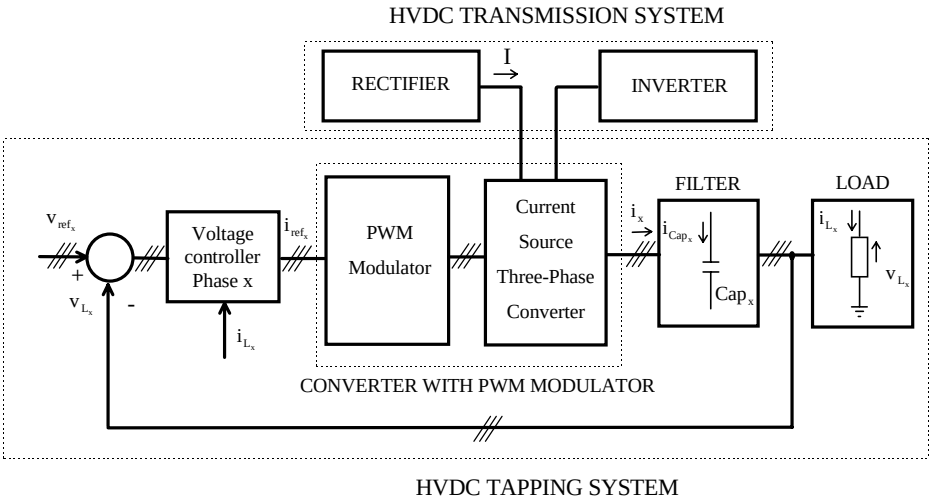

Fig. 2.2: Block diagram for a HVDC Tapping System as an application example for the three-phase current source converter.

$$\overline{p}(t) = \overline{e}(t) \cdot \overline{i}(t) = E \cdot I = \frac{3}{2} \cdot M \cdot V_m \cdot I \cdot \cos\varphi \qquad (2.2)$$

where M and V_m are respectively peak value of modulation index and phase voltage, per phase. The converter in this case is supposed ideal (lossless).

Filter capacitors are calculated [5] to carry 10% to 20% of total converter current (0,1 < k < 0,2), in order to minimize reactive current and to keep voltage ripple within limits. The maximum voltage ripple [5] at capacitor in generic phase x can also be calculated.

$$Cap = \frac{k \cdot M \cdot I}{\omega \cdot V_m} \qquad (2.3)$$

$$\Delta V_{capxmax} = \frac{I \cdot T_s}{4 \cdot Cap} \qquad (2.4)$$

where T_s is the PWM carrier period.

Block diagram for the system, considering as application example an HVDC system tapping, is given in Fig. 2.2.

3. LOAD VOLTAGE CONTROL STRATEGY - THE DEADBEAT CONTROLLER

The control objective is to generate, in each phase x, an $i_x(t)$ current in order to obtain sinusoidal voltage $v_{Cx}(t)$ at that phase, tracking a sinusoidal reference $v_{Refx}(t)$. As a three wire AC system is considered (see Fig. 2.1), each phase can be modeled independently, as seen in Fig. 3.1. One can notice that load dynamics does not appear directly, but as a measurable perturbation $i_{Lx}(t)$ (load current at phase x) at the control system.

3.1. Deadbeat controller

The step response of a discrete time feedback control system is considered ideally as deadbeat type if its output reaches its final value in a minimum time interval and stays there, meaning null steady state error at samplings instants. For a first order system, as the one at Fig. 3.1, one can impose system output variable following the reference with a delay of one sampling interval Δt. This delay is not important if one considers a regulation problem, where output is to be kept constant, following a constant reference. In this case, reference is sinusoidal, leading to a tracking problem. Direct application of the deadbeat philosophy would result in a output signal amplitude delayed of a sampling interval Δt. Load perturbation adds additional degradation to the controller performance. Thus, following considerations transform original deadbeat philosophy into another one with predictive characteristics, aiming the minimization of the referred delay error.

For analysis purpose, each phase can be modeled independently with its individual controller, imposing this way null value for average instantaneous phase current

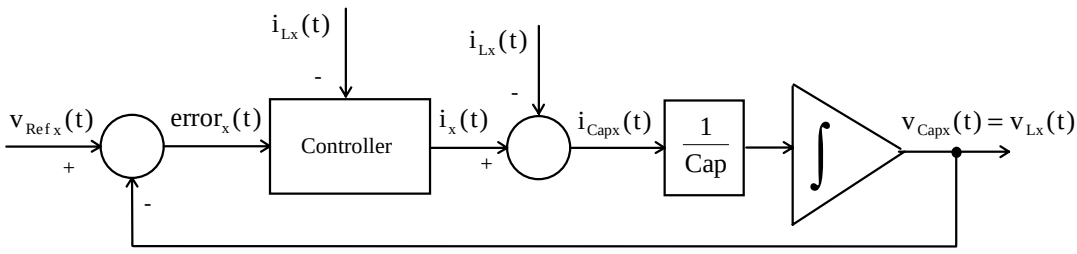

Fig. 3.1: Block diagram of the control structure, per phase.

sum: $\bar{i}_a(t)+\bar{i}_b(t)+\bar{i}_c(t)=0$ (3.1). In the following per phase analysis the subscripts *a*, *b*, *c* or *x* (generic phase) are suppressed in order to simplify notation. For a given instant *t* and sampling interval *Δt*, phase load voltage (equal to capacitor voltage) is given by (3.4), with $i_{Cap}=i-i_L$ (3.3):

$$v_L(t+\Delta t)=v_L(t)+\frac{1}{Cap}\int_t^{t+\Delta t} i(t)dt-\frac{1}{Cap}\int_t^{t+\Delta t} i_L(t)dt \qquad (3.4)$$

Reference signal v_{Ref} is sinusoidal, thus $v_{ref}(t+\Delta t)$ can be calculated. Therefore the non-causal equation $v_L(t+\Delta t)=v_{ref}(t+\Delta t)$ (3.5) can be imposed.

Within the sampling interval, converter output current is a pulsed signal with two levels ($+I$ and zero, or zero and $-I$), but with local average value $\bar{i}$ equal to the reference signal $\bar{i}_{ref}$, imposed by the controller to the PWM block. Replacing i by $\bar{i}_{ref}$ at (3.4) results (3.6), which provides the same values of (3.4) only at sampling instants.

$$v_L(t+\Delta t)=v_L(t)+\frac{1}{Cap}\int_t^{t+\Delta t}\bar{i}_{ref}(t)dt-\frac{1}{Cap}\int_t^{t+\Delta t} i_L(t)dt \qquad (3.6)$$

Value $i_L(t+\Delta t)$ is unknown, but with time interval *Δt* small enough, local average load current $\bar{i}_L$ can be considered constant: $\bar{i}_L(t+\Delta t)=\bar{i}_L(t)$ (3.7).

From the previous assumptions, one can obtain (3.8), which models load voltage as straight lines, as in Fig. 3.2.

$$v_L(t+\Delta t)=v_L(t)+\frac{\bar{i}_{ref}(t)}{Cap}\cdot\Delta t-\frac{i_L(t)}{Cap}\cdot\Delta t \qquad (3.8)$$

Controller implementation requires the sampling of load voltage and current ($v_L(t)$ and $i_L(t)$) at the instant *t*, as well as reference voltage value $v_{ref}(t+\Delta t)$. Reference current $\bar{i}_{ref}(t)$ can be calculated, adopting the hypothesis that load current $i_L(t)$ is kept constant between instants *t* and *t+Δt*, imposing zero error for load voltage at instant $t+\Delta t$.

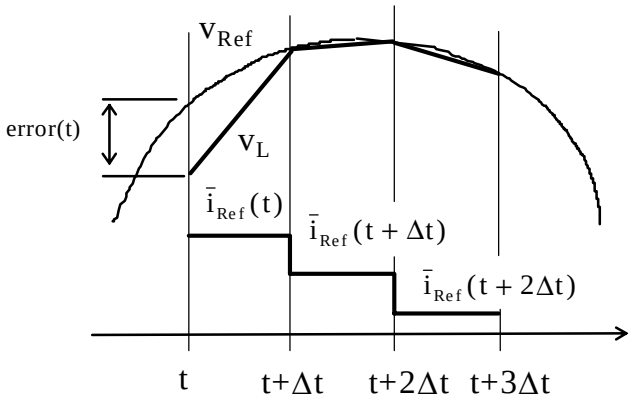

Fig 3.2: Behavior of load and reference voltages, as well as reference current, of the PWM block.

$$v_{ref}(t+\Delta t)=v_L(t+\Delta t) \qquad (3.9)$$

From (3.8) one can obtain:

$$\bar{i}_{ref}(t)=\frac{\left[v_{ref}(t+\Delta t)-v_L(t)\right]\cdot Cap}{\Delta t}\cdot\Delta t+i_L(t) \qquad (3.10)$$

The procedure is repeated for each sampling instant.

Adopted assumptions, as load current hypothesis (see (3.8) and (3.9)), lead to non-zero error at the end of sampling interval, which increases with sampling period. For higher values of *Δt*, another error source is the effect of zero order samplings on the load voltage behavior between sampling intervals [7]. Thus, load voltage regulation due to load variation could be deficient, and needs to be compensated with an additional control loop, shown in Fig. 3.3. Reference $V_{Ref(peak)}$ (peak value of reference voltage v_{Ref}) is compared with peak value of the fundamental component (first harmonic) of load voltage V_{L1}, and the resulting error signal is applied to a PI controller, with dominant closed loop pole imposing voltage correction in a time interval of about one to two reference signal cycles. This allows PI controller output having the corrected peak

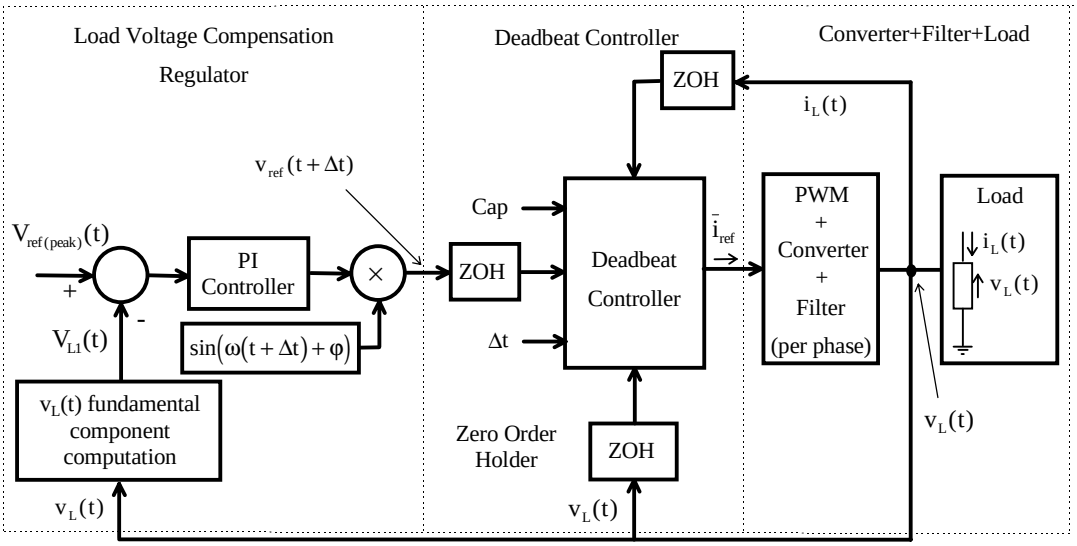

Fig. 3.3: Block diagram, per phase, showing load voltage compensation regulator, deadbeat controller, PWM converter+filter+load.

value of reference signal, which is multiplied with a unity peak value sinusoidal signal with delay φ, shifted by a sampling interval time Δt to obtain the reference voltage estimation $v_{Ref}(t+\Delta t)$.

3.2. PWM modulation requirements by deadbeat controllers

Converter output current $i(t)$ is a pulsed signal generated by the PWM block from a reference $\bar{i}_{ref}(t)$. It can be represented by its instantaneous average value $\bar{i}(t)=\bar{i}_{ref}(t)$ in a time period Δt. This assumption does not constitutes an error source for calculating $\bar{i}_{ref}(t)$, because (3.11) imposes zero error for the output voltage for each sampling instant, allowing a deadbeat response. It can be confirmed by (3.7), noticing that relationship imposed by (3.11) is satisfied.

$$\int_{t}^{t+\Delta t} i(t)dt = \int_{t}^{t+\Delta t} \bar{i}(t)dt = \int_{t}^{t+\Delta t} \bar{i}_{ref}(t)dt = \bar{i}_{ref}(t)\cdot\Delta t \qquad (3.11)$$

Until now nothing was imposed about the system behavior between samplings. If, in a given sampling interval Δt, average value of $i(t)$ is equal to $\bar{i}_{ref}(t)$, PWM signal duty-cycle is unique and defined by (3.12).

$$D(t) = (\tau(t)/T_S) \qquad (3.12)$$

Once defined $\bar{i}_{ref}(t)$ and duty-cycle $D(t)$, current pulse position within sampling interval Δt, related to PWM modulation carrier, has to be defined (see Fig. 3.4). The three cases of Fig. 3.4 have the same average current value $\bar{i}(t)=\bar{i}_{ref}(t)$, satisfying deadbeat criteria. However, cases (a) and (c) have instantaneous average value of load voltage $\bar{v}_L(t)$ differing from the desired v_{ref}. Centered pulse, as shown in case (b), imposes load voltage oscillation with null mean value within sampling interval Δt, assuring load instantaneous average value $\bar{v}_C(t)$ to be equal to reference voltage $v_{ref}(t)$. PWM modulation proposed by [5] has centered pulse, being adequate for a deadbeat controller as described here.

The adopted deadbeat method does not require anti-aliasing filtering, needed by other digital or analog control strategies in order to eliminate the oscillatory component of load voltage $v_L(t)$.

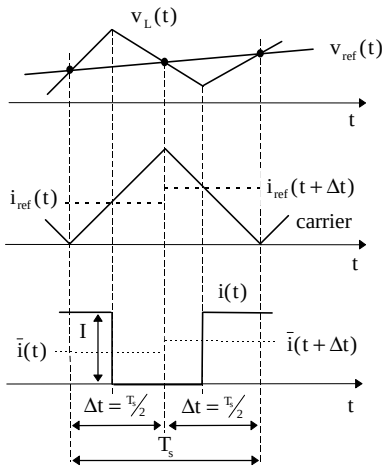

Fig. 3.5: PWM asymmetric modulation with sampling period Δt equal to half of switching period T_S.

To this point, it was considered that sampling period Δt was equal to PWM switching period T_S. However, Fig. 3.4(b) shows that with centered pulse, load voltage error is zero at instants T_S and $T_S/2$. By adopting a sampling period Δt equal to half of the switching period T_S, one can obtain a reduction on errors associated with sampling period, which is an advantage in high power converters with limited switching frequencies, imposed by semiconductor switches constraints. This alternative is only possible if the converter can impose $\bar{i}_{ref}$ for each semi-period of switching interval T_S. An asymmetric PWM modulation, shown in Fig. 3.5, is needed for that, allowing converter current average value changing at each sampling period Δt.

4. SIMULATION RESULTS

For simulation purposes, a converter with DC side values of 25kV and 2KA and load power of 50MW, power factor cosφ=0.8, was adopted. For a modulation index limited to 0.8, one obtains AC side phase peak voltage value of 26kV. The capacitor value is 24.5μF,

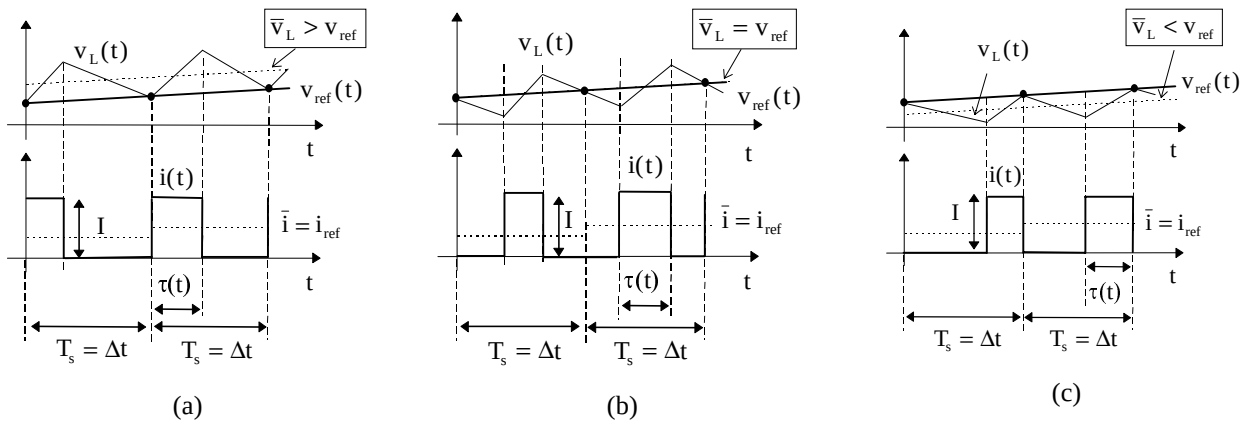

Fig. 3.4: Current pulse position within sampling interval ΔT, related to PWM modulation carrier: (a) right sided pulse; (b) centered pulse; (c) left sided pulse.

corresponding to 15% of the total converter current. Switching frequency is 1200Hz and the PI controller has parameters K_I=0.02s e K_P=1.0.

PSCAD/EMTDC™ electromagnetic transients simulation software [6] was used for power and control systems simulation. Fig. 4.1 shows line voltages waveforms and corresponding harmonic spectrum for line voltage Vab. Total harmonic distortion (THD(%)) is 21.2%.

Cases with linear (balanced and unbalanced) loads (R, RL and RC loads) and non-linear (non-controlled rectifier with RL load at DC side) loads were simulated successfully, in steady state and transient conditions. Unbalanced loads showed no visible effect in line voltages, which was expected, as per phase voltage control was adopted. Transient simulations included full and half power load insertions and disconnections (rejections). Full load rejection and connection resulted in less then 6% overvoltage and undervoltage, respectively. Both cases required less the ten cycles to return to nominal line voltages. Due to the lack of space, waveforms of these cases were not included here.

Resulting voltage ripple is relatively high, due to switching frequency and capacitor value. Switching frequency is limited by the high power electronic switches, and capacitor value increase reduces the total amount of active power available to the AC load. A solution for the problem is to adopt multiconverter configuration, with individual Graetz converters connected in series at the DC side and in parallel at the AC side, with PWM carriers regularly displaced among them. The multiconverter configuration reduces the voltage ripple by a $1/N^2$ factor [7][8], where N is the number of associated converters. Fig. 4.2 shows results from a multiconverter system with two converters. Line voltages waveforms and corresponding harmonic spectrum for line voltage Vab are presented. The same line voltage of former simulation was adopted, so numerical comparison with Fig. 4.1 is immediate. THD(%) is reduced to 5.8%.

5. CONCLUSIONS

In this work a current source type three-phase PWM converter with deadbeat controller was presented. The application example was a tapping system for a HVDC connection, designed to feed an isolated load with three-phase power at mains frequency.

The AC three wire system adopted allowed for a per phase modeling, in which the load is considered a measurable perturbation of the plant. The plant input is the AC capacitors sinusoidal voltages and its output is the converter reference currents. Due to the sampling nature of the PWM converter, a deadbeat controller was studied, and its characteristics, as well as PWM requirements, were obtained.

Computational simulations were done with the PSCAD/EMTDC™ electromagnetic transients simulation package, including power and control systems. Cases with linear (balanced and unbalanced) and non-linear loads were simulated successfully, in steady state and transient conditions.

Switching frequency and capacitor filter value limitations resulted in a relatively high output (AC) voltage ripple. A solution employing multiconverters was proposed

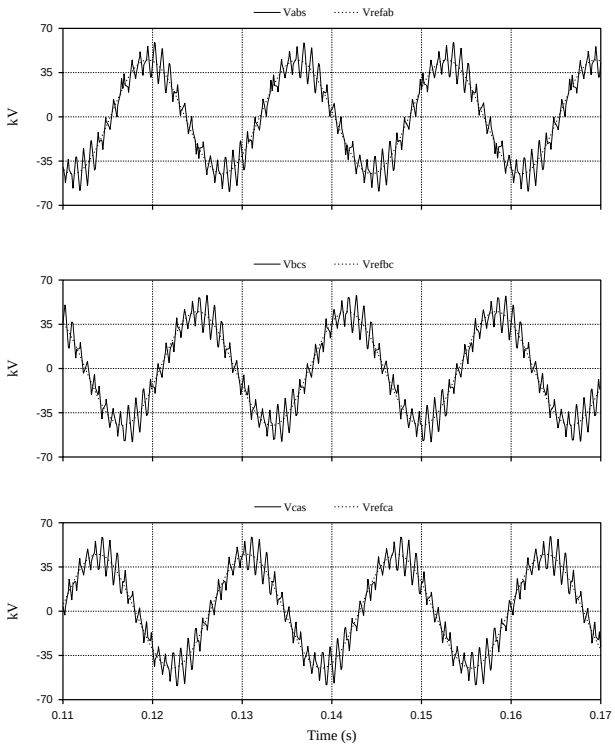

Fig. 4.1(a): Converter line voltages and corresponding references.

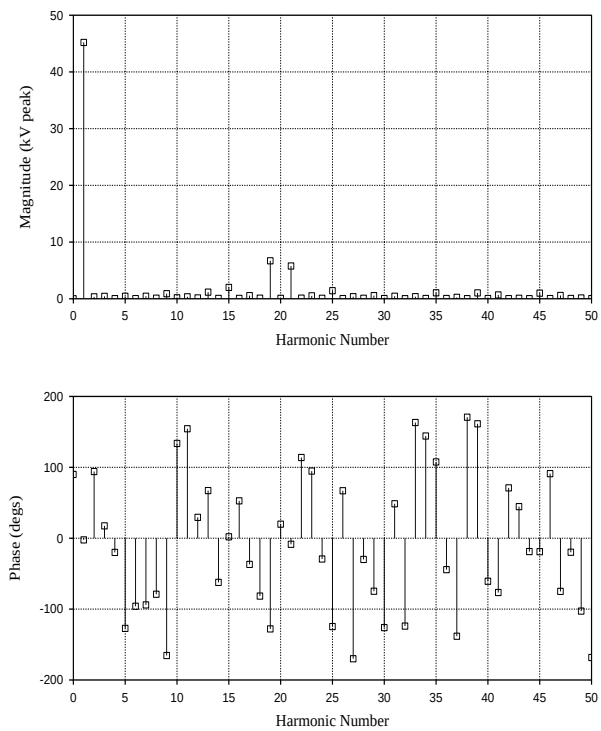

Fig 4.1(b): Harmonic spectrum (magnitude and phase) for line voltage Vab.

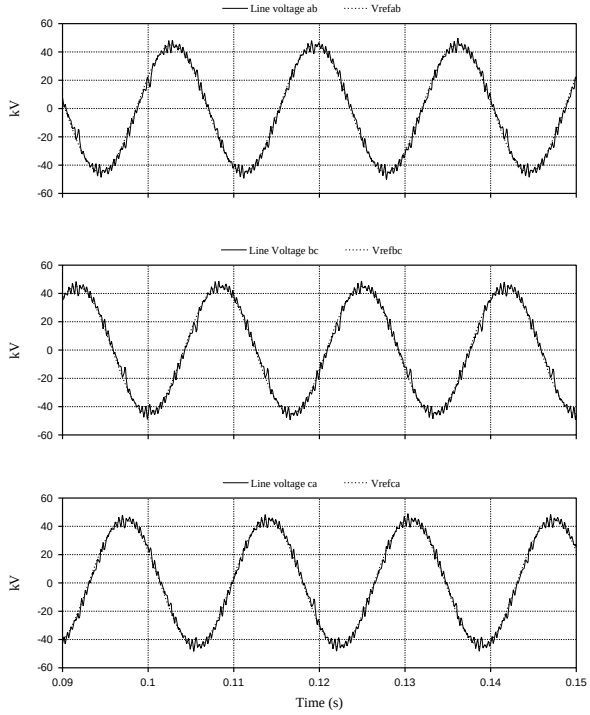

Fig. 4.2(a): Converter line voltages for the multiconverter system.

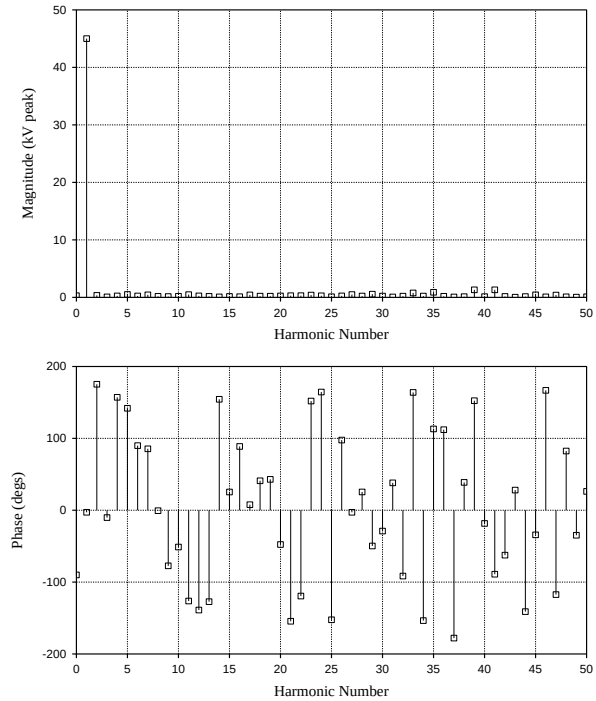

Fig 4.2(b): Harmonic spectrum (magnitude and phase) for line voltage Vab for the multiconverter system.

and a system with two converters was simulated, confirming its superior performance, compared with the single converter solution.

6. REFERENCES

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