A Static Synchronous Series Compensator Based on a Dual Multipulse Voltage Source Inverter Bridge

Pedro G. Barbosa(1) *and* *Edson H. Watanabe*(2)

(1) Universidade Federal de Juiz de Fora
Dept. de Energia Elétrica
P.O. Box 422
36.001-970 - Juiz de Fora - MG
{pedrog@lacee.ufjf.br}

(2) COPPE - Univ. Federal do Rio de Janeiro
Programa de Engenharia Elétrica
P.O. Box 68.504
21.945-970 - Rio de Janeiro - RJ
{watanabe@coe.ufrj.br}

***Abstract* - This paper describes the modeling of a Static Synchronous Series Compensator (SSSC) for a FACTS application. The proposed SSSC consists of two multipulse STATCOM which are connected in parallel with a common DC link capacitor. The three-phase series compensation voltages are obtained by the difference between the two output voltages of two STATCOM and the injected series voltages can be synthesized with any phase with respect to the line currents. The control algorithm of the SSSC uses the instantaneous power theory. The feasibility of the proposed compensator topology was verified by digital simulation using an Alternative version of Electromagnetic Transients Program Package (ATP/EMTP).**

Keywords - Reactive power compensators, Series compensators, FACTS devices.

I. INTRODUCTION

HISTORICALLY fixed series capacitors are widely used with long transmission lines to reduce the lines virtual length and increase its active power transfer capability. Recently, TSSC (Thyristors Switched Series Capacitors) and TCSC (Thyristors Controlled Series Capacitors) have been implemented to speed up the system dynamic response and avoid SSR (Subsynchronous Resonance) problems.

After the advent of GTOs (Gate Turn-off Thyristors), GCTs (Gate Commutated Thyristors) and IGBTs (Insulated Gate Bipolar Transistors) a number of new FACTS (Flexible AC Transmission Systems) [1] devices has been designed and investigated for reactive power compensation. These high power self-commutated switches are the main option to design high power Voltage Source Inverters (VSIs).

In this way, when VSIs are operated synchronously at the system fundamental frequency, they may be connected in parallel and in series with the transmission line, producing a controllable shunt reactive current and voltage respectively. They are the basis for new compensator topologies such as STATCOM (Static Compensator), SSSC (Static Synchronous Series Compensator) and UPFC (Unified Power Flow Controller) [2]-[11]. The objective of this work is to describe the fundamental operation of a Static Synchronous Series Compensator (SSSC) based on a Dual-Bridge VSI topology. The compensator characteristics and the basic principle of its control are tested and discussed through results obtained with an Alternative version of Electromagnetic Transients Program Package (ATP/EMTP).

II. BASIC PRINCIPLES OF THE SSSC

Fig. 1 shows the basic diagram of an Ideal Static Synchronous Series Compensator (SSSC) and a by-pass switch (*Sw*) connected in parallel. The current flowing through the line without losses of Fig. 1 is given by:

$$\boldsymbol{I} = \frac{(\boldsymbol{V}_S - \boldsymbol{V}_R) - \boldsymbol{V}_q}{jX_L}, \qquad (1)$$

where, V_S is the sending-end voltage; and V_R is the receiving-end voltage; X_L is the series line impedance and δ is the phase angle between V_S and V_R.

From (1), it is possible to conclude that the voltage drop across the line reactance ($\boldsymbol{V}_L$), and consequently the line current and the power P_S flowing through the line can be easily changed by controlling the series compensating voltage $\boldsymbol{V}_q$.

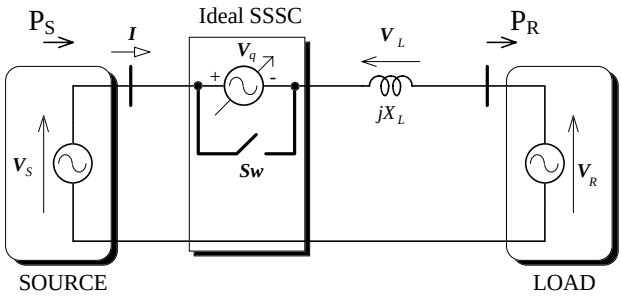

Fig. 1: Ideal Static Synchronous Series Compensator (SSSC) block diagram.

Figure 2 (a) and (b) shows the phasor diagram of the compensated AC system assuming that the SSSC is compensating only capacitive and inductive reactive power in series, respectively. Varying the magnitude and phase of the output voltage generated by the SSSC controls the reactive power. Thus, if the compensator output voltage lags $\pi/2$ *rad* the line current, the SSSC will drain a negative reactive power; and a positive reactive power is generated when its output voltage leads $\pi/2$ *rad* the line current.

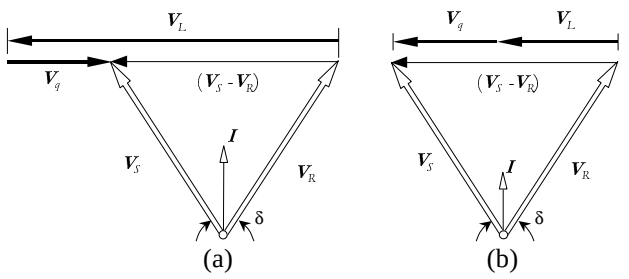

Fig. 2: Phasor diagram of the SSSC compensation characteristic: (a) capacitive and (b) inductive.

The SSSC shown in Fig. 1 can be a Voltage Source Inverter (VSI) with a capacitor in its DC side and connected to the transmission line through a series transformer [7]-[9] as shown in Fig. 3. The control block uses the powers p^* and q^* as its references signal and if only reactive power is to be compensated p^* is made zero and q^* has to be chosen to control the power flowing over the AC line.

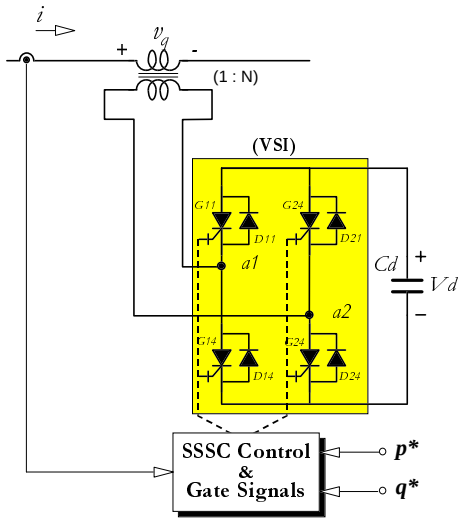

Fig. 3: Static Synchronous Series Compensator (SSSC) based on a Voltage Source Inverter (VSI).

Many papers propose PWM (Pulse Width Modulation) strategies to vary the magnitude and phase of the series voltage synthesized by SSSC [9],[10]. However, the main disadvantage of the usage of high-power PWM-VSI is that the switching losses become very critical. On the other hand, similar voltage waveforms could be obtained by using multipulse or multilevel inverters [11].

Two practical 48-pulse STATCOM prototypes with 80 *MVA*[3] and 100 *MVA* [4] were reported in Japan and the USA respectively and an UPFC with shunt and series compensation capabilities of ±160 *MVA* [5] entered full operation in 1998, in the United States.

III. QUASI 48-PULSE VSI

Multipulse VSI design is one way to obtain "*free-harmonic*" output voltages and currents. They can reach high voltages and reduce harmonic distortion because of their complex magnetic structure. Several 6-pulse Voltage Source Inverters have its output voltages combined to synthesize a staircase voltage waveform. If the number of 6-pulse VSI increases, the levels of the inverter output voltage improves, approaching a sinusoidal waveform. In these configurations the VSI switching frequency is kept low in order to minimize the semiconductor stress, switching losses and electromagnetic interference.

One approach to obtain a quasi 48-pulse STATCOM is to use four 12-pulse converters connected in series through its Y-Y and Y-Δ isolation transformers [8],[11]. Fig. 4 shows the proposed multipulse inverter configuration. In this figure, the fundamental output voltage of the first converter is time leading by +3π/48 *rad* with respect to an arbitrary reference. The following converters are time shifted, with respect to the first VSI, by π/24 *rad*. These magnetic structures give a quasi 48-pulse output voltage with minimized characteristic harmonics. The inverter configuration described here is one of the several different topologies that can be used to build a quasi 48-pulse VSI. This magnetic structure is much less complicated than in the case of a real 48-pulse converter [3] or [4].

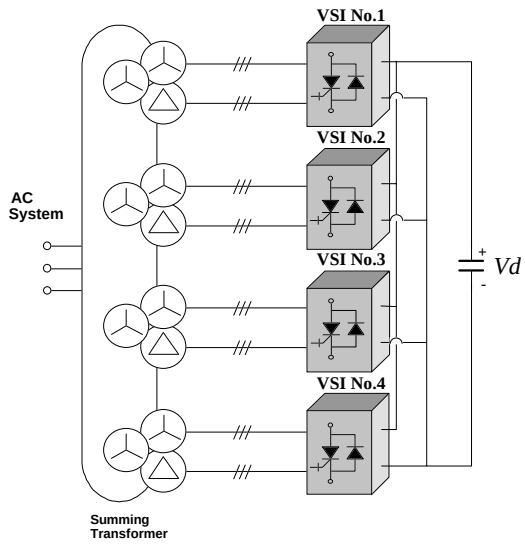

Fig. 4: Quasi 48-pulse high power VSI circuit diagram based on four 12-pulse inverters.

Fig. 5 (a) and (b) show an example of the synthesized output phase voltage and its harmonic spectrum, respectively. This 48-pulse output voltage has minimized the eleventh, thirteenth, twenty-third, twenty-fifth, thirty-fifth, thirty-seventh, forty-eighth and forty-ninth harmonics. The THD for the voltage waveform of Fig. 5(a) is 3.2 %.

In this way, a multipulse inverter can replace the PWM-VSI shown in Fig. 3. The multipulse inverter circuit is switched to produce a terminal voltage in quadrature with the AC line currents as described before. This strategy is achieved by controlling the phase of the SSSC output voltages in relation to the line current. In fact, by changing this phase, some active power can flow to or from the DC capacitor and therefore increase or decrease the DC voltage, making possible the magnitude control of the inverter output voltages and consequently the reactive power generated in series by the SSSC.

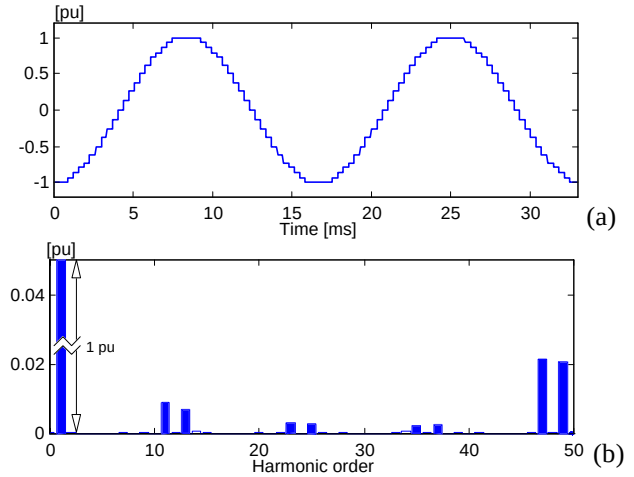

Fig. 5: (a) Quasi 48-pulse VSI phase voltage waveform and (b) harmonic components of staircase sinusoidal voltage.

IV. The Proposed Dual-Bridge SSSC: Theoretical Analysis

The single phase SSSC circuit shown in Fig. 3 is inherently two converters connected in parallel to the same DC link capacitor. This circuit can be redraw as in Fig. 6 where the switches of the VSIs No.1 and No.2 are operated to "generate" fundamental frequency voltages. The difference between them will be injected in series with the transmission line.

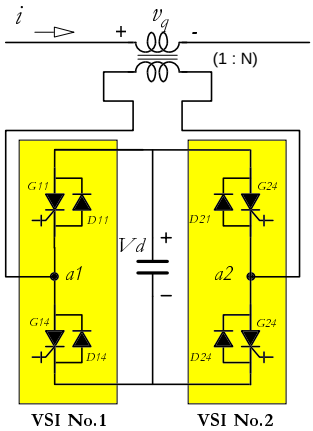

Fig. 6: Two-converter representation of single phase SSSC circuit.

Despite of the fact that multipulse inverter is the most adequate for high power applications, the magnitude of multipulse SSSC output voltage will depend on the DC capacitor voltage. This characteristic is not desirable because the power system has to deliver some active power to charge or discharge the inverter DC capacitor. To overcome this constraint each single converter shown in Fig. 6 may be replaced by a 48-pulse VSI.

Fig. 7 shows a Dual-Bridge multipulse SSSC proposed in this work to obtain a set of three phase series voltages. The dual-bridge SSSC is composed by two-shunt multipulse VSI with a common DC link. This DC link establishes an additional path to exchange some real (active) power between the two STATCOM. Thus, the series compensation voltages can be varied without any PWM switching scheme or DC capacitor charge or discharge.

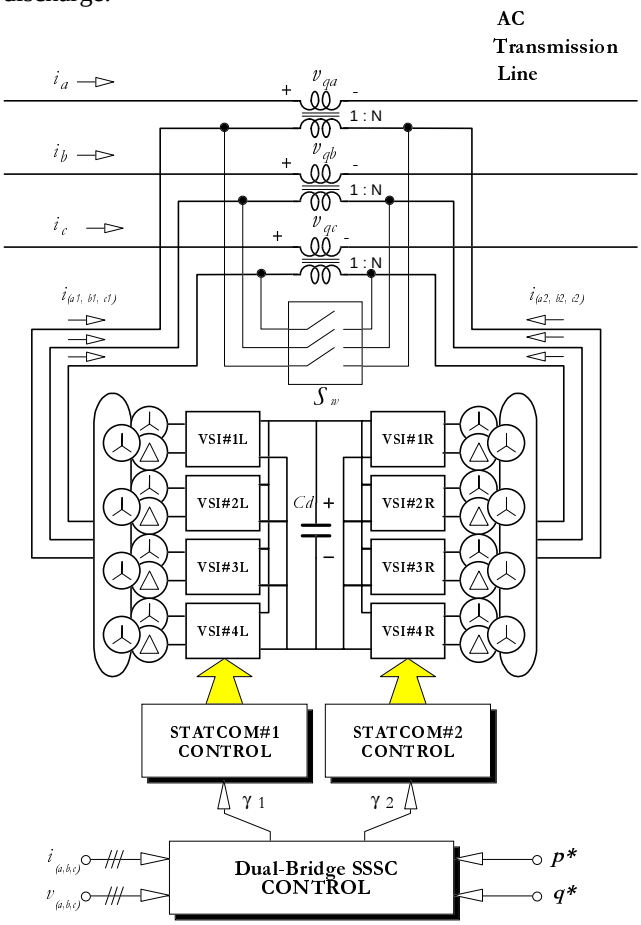

Fig. 7: Dual-Bridge SSSC block diagram based on quasi 48-pulse multipulse inverter.

Fig. 8 shows the phasor diagram of the SSSC series voltage in case of both STATCOM output voltages (V_1 and V_2) have their magnitude and phase varied. This characteristic implies in some modulation to control each VSI. However, equivalent results can be obtained controlling the sector angle (φ) and the phase angle between the VSI voltages ($\gamma = (\gamma_1 - \gamma_2)$), as shown in Fig. 9.

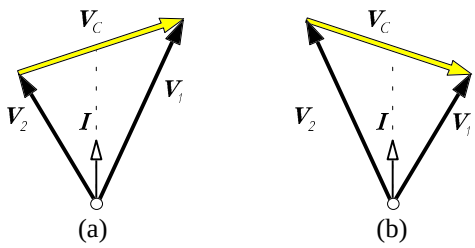

Fig. 8: SSSC phasor diagrams for capacitive characteristic: (a) absorbing real power and (b) delivering real power in series.

Fig. 10 shows the total harmonic distortion for the proposed SSSC topology for different phase angles between the two STATCOM voltages. From the above advantages the proposed Dual-Bridge SSSC is considered more suitable to built the series compensator in spite of having two times more VSIs.

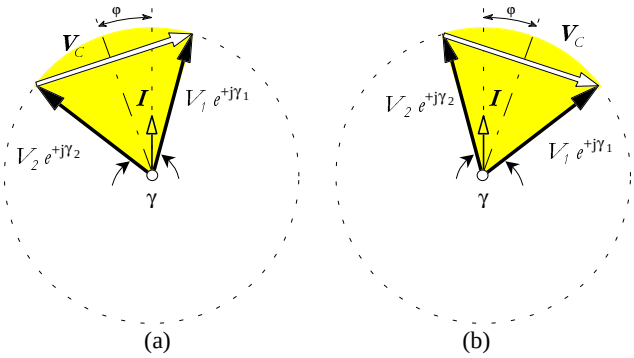

Fig. 9: Dual-Bridge SSSC phasor diagrams for capacitive characteristic: (a) absorbing real power and (b) delivering real power in series.

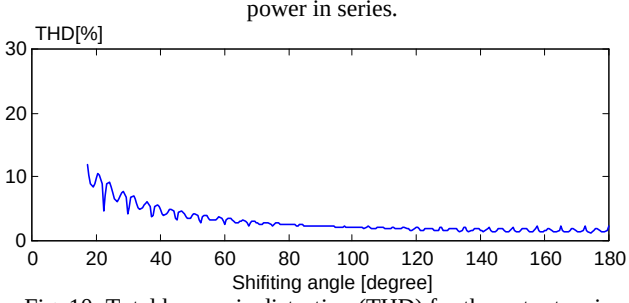

Fig. 10: Total harmonic distortion (THD) for the output series voltage of Dual-Bridge SSSC.

V. Dual-Bridge SSSC Control Strategy

The control algorithm of the Dual-Bridge SSSC uses the concepts of the instantaneous *p-q* power theory [12],[13]. Considering the set of three-phase series voltages and line currents shown in Fig. 7, the instantaneous real (p_c) and reactive (q_c) powers drained in series with the AC transmission line are given by:

$$\begin{bmatrix} p_c \\ q_c \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} v_{q\alpha} \\ v_{q\beta} \end{bmatrix}, \tag{2}$$

where, i_α and i_β are the instantaneous line currents (*A*); $v_{q\alpha}$ and $v_{q\beta}$ are the instantaneous SSSC compensating voltages (*V*), all in α-β reference frame (Appendix) [9]-[13].

Based on the topology proposed in Fig. 7, the compensating voltages can be written as $v_{q\alpha} = (v_{1\alpha} - v_{2\alpha})$ and $v_{q\beta} = (v_{1\beta} - v_{2\beta})$, *i.e.*, the difference between the STATCOMs #1 and #2 instantaneous phase voltages (*V*), respectively.

Then, the real and reactive powers injected in series by the SSSC can be divided between the left and right STATCOM contribution as follows,

$$\begin{bmatrix} p_c \\ q_c \end{bmatrix} = \begin{bmatrix} p_1 \\ q_1 \end{bmatrix} - \begin{bmatrix} p_2 \\ q_2 \end{bmatrix} = \\ = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} v_{1\alpha} \\ v_{1\beta} \end{bmatrix} - \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} v_{2\alpha} \\ v_{2\beta} \end{bmatrix}, \tag{3}$$

where, p_1 and q_1 are respectively the instantaneous real (*W*) and imaginary (*var*) powers on the left-hand side STATCOM terminals; p_2 and q_2 are respectively the instantaneous real (*W*) and imaginary (*var*) powers on the right-hand side STATCOM terminals.

Neglecting the voltage harmonics produced by each Quasi 48-pulse VSI of Fig. 7, two pair of equations can be written for the proposed compensator in α-β coordinates, as follows:

$$\begin{cases} v_{1\alpha} = \sqrt{3}\, kV_d \sin(\omega t + \gamma_1) \\ v_{1\beta} = -\sqrt{3}\, kV_d \cos(\omega t + \gamma_1) \end{cases}, \tag{4}$$

and

$$\begin{cases} v_{2\alpha} = \sqrt{3}\, kV_d \sin(\omega t + \gamma_2) \\ v_{2\beta} = -\sqrt{3}\, kV_d \cos(\omega t + \gamma_2) \end{cases}, \tag{5}$$

where, *k* is a factor for the multipulse VSI which relates the DC side voltage to the *rms* value of the phase voltage at the inverters AC terminals; V_d is the average DC side inverter voltage (*V*); ω is the angular fundamental frequency (*rad/s*); γ_1 and γ_2 are respectively the phase angles of the left and right hand side 48-pulse VSI output voltages (*rad*)

Assuming that the compensated AC transmission line is at steady state, the following equations can be written for the balanced three phase currents, in α-β coordinates.

$$\begin{cases} i_\alpha = \sqrt{3}\, I_L \sin(\omega t + \phi) \\ i_\beta = -\sqrt{3}\, I_L \cos(\omega t + \phi) \end{cases}, \tag{6}$$

where, I_L is the *rms* value of the line currents (*A*); ϕ is the generic phase angle (*rad*) of the line currents.

Substituting (4), (5) and (6) in (3), the instantaneous real and reactive powers at the STATCOM #1 and #2 terminals are given by:

$$\begin{cases} p_1 = 3\, kV_d I_L \cos(\gamma_1 - \phi) \\ q_1 = 3\, kV_d I_L \sin(\gamma_1 - \phi) \end{cases}, \tag{7}$$

and

$$\begin{cases} p_2 = 3\, kV_d I_L \cos(\gamma_2 - \phi) \\ q_2 = 3\, kV_d I_L \sin(\gamma_2 - \phi) \end{cases}, \tag{8}$$

Note that, from (7) and (8), if $\gamma_2 = -\gamma_1$, the instantaneous real powers p_1 and p_2 at terminals of the STATCOMs #1 and #2 have the same value. Then the instantaneous real power injected in series by the compensator is zero, *i.e.*, $p_c = (p_1 - p_2) = 0$. In contrast to the behavior presented above, the instantaneous reactive powers q_1 and q_2 have opposite signals. Hence the instantaneous reactive power drained in series by the proposed SSSC is equal to $q_c = (q_1 - (-q_2)) = (q_1 + q_2)$. In this way, the algorithm proposed here to control the SSSC produces a compensator able to synthesize a virtual capacitive (if, $q_1 < 0$ and $q_2 > 0$) or inductive (if, $q_1 > 0$ and $q_2 < 0$) variable reactance in series with the ac transmission line by controlling the phase angles γ_1 and γ_2.

Figure 11 shows the control block diagram of the Dual

Bridge SSSC. The variables with superscript (*) represent the reference powers that should be supplied to the compensator control block and can be positive, negative or zero. The frequency and phase angle of the source line current (θ) is obtained from a digital PLL (*Phase Locked-Loop*) implemented as shown in [11]. The instantaneous three phase line currents and compensator voltages are used to calculate the instantaneous real and reactive powers at the SSSC terminals. The error between the desired (q^*) and measured (q_c) reactive powers is fed in a PI controller of which the output is the reference phase angle (γ) between the voltages generated by STATCOM #1 and #2. In fact, by changing this phase angle, the magnitude and phase of series compensating voltages can be increased or decreased, making possible the continuous control of the reactive power injected in series by the SSSC without the DC capacitor voltage charge or discharge, as explained before.

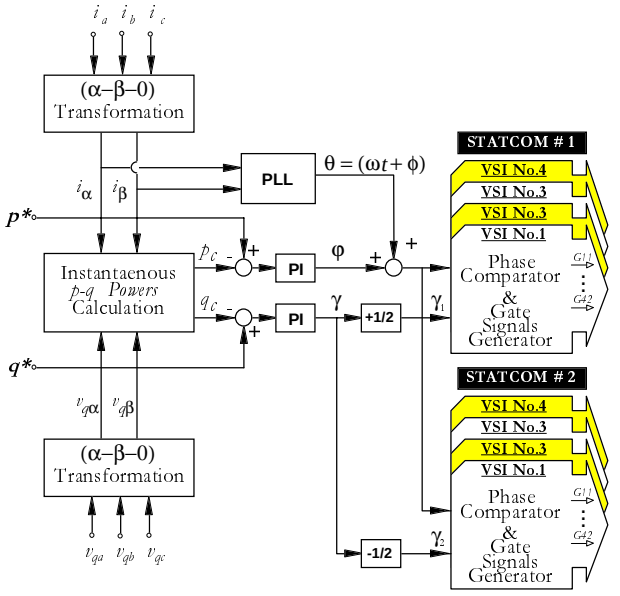

Fig. 11: Control block diagram of Dual Bridge SSSC based on quasi 48-pulse VSI.

The instantaneous real reference power p^* is used to keep the Dual-Bridge DC capacitor voltage at a given value through the control of the sector angle (φ) as shown in Fig. 9. Thus, the input of the phase comparator are γ and θ, and its output is the turn on and turn off signals for each semiconductor switch of the proposed Dual-Bridge SSSC.

VI. Simulation Results

A 100 MVA / 230 kV Dual-Bridge SSSC based on quasi 48-pulse inverter, with 2000 μF / 12.5 kV DC capacitor, was modeled using the ATP/EMTP [14] package as shown in Fig. 12. The SSSC was connected at the sending-end of a double circuit transmission system with 230 *kV* and 200 *km*, whose parameters are given in Table I. The source and the load are modeled as two ideal three-phase voltage source behind a reactance and phase-shifted by π/6 *rad*.

Table I: Transmission line parameters.

#	R (Ω/km)	L (mH/km)	C (μF/km)
Zero seq.	0.03167	3.2220	0.00787
Pos. seq.	0.02430	0.9238	0.01260

Figure 13 shows the three-phase transmission line currents. Initially the Dual-Bridge SSSC operates with a null compensation characteristic, then in t = 100 *ms* the instantaneous reference reactive power is step changed to -50 *Mvar* and the compensator output series voltage lags by π/2 *rad* the line current (capacitive characteristic). The time to respond to this step change is less than 20 ms, showing that this system can be very fast. In t = 200 *ms* the instantaneous reference reactive power is switched from -50 *Mvar* to +50 *Mvar* and the compensator operates with an inductive compensation characteristic (series voltage leads by π/2 *rad* the line current). As it can be seen, the transmission line currents decrease when the compensation becomes inductive. Then, after t = 300 *ms* the instantaneous reference reactive power is made zero and the compensator output voltages become null. Note that the compensation characteristics are obtained without any charge/discharge of DC capacitor voltage. Fig. 14 shows series output compensation voltages while Fig. 15 shows the phase *a* STATCOMs output voltage. Fig. 16 shows in detail the behavior of line current and series compensation voltage, respectively. All the curves are normalized considering 100 *MVA* and 1 *kA* as base values.

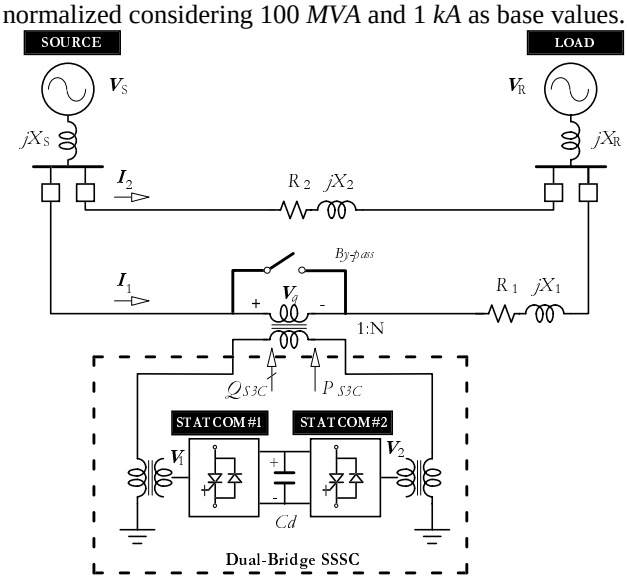

Fig. 12: Single line diagram of Dual-Bridge SSSC.

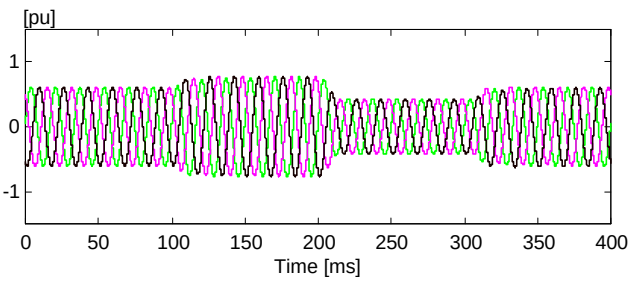

Fig. 13: Three-phase line currents.

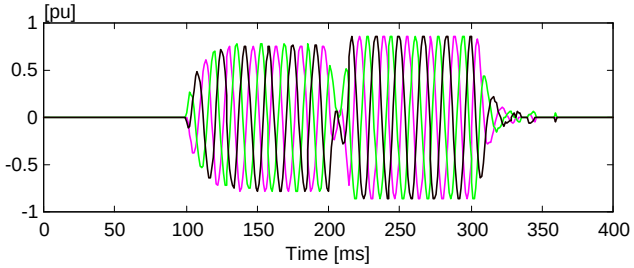

Fig. 14: Three-phase dual-bridge SSSC voltages.

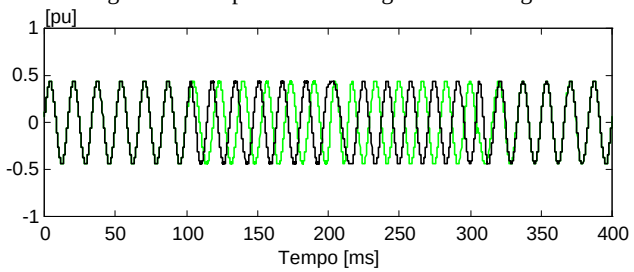

Fig. 15: Phase "*a*" quasi 48-pulse STATCOMs output voltages.

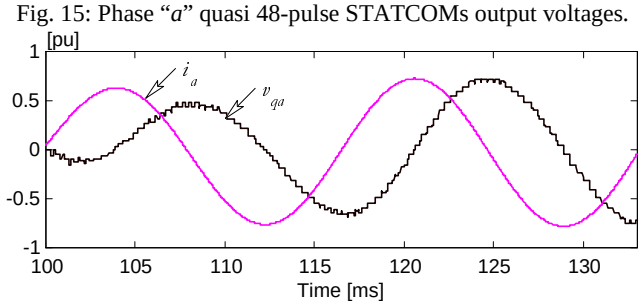

Fig. 16: Phase "*a*" SSSC multipulse output voltage and line current.

VII. Conclusion

This paper presented some basic concepts and principles of operation of a Dual-Bridge series FACTS devices. The EMTP was used to model and illustrate the operation of the proposed new compensator.

Some advantages of Dual-Bridge SSSC such as: controllability, energy storage components, higher performance, lowers harmonics generation were presented and discussed.

It was shown that the instantaneous power theory could be used to design the control the Dual-Bridge SSSC. The authors are convinced that this theory and the use of high power self-commutated semiconductor switches will be responsible for the faster dynamic behavior of future power transmission systems.

Appendix

The α-β-0 transformation and its inverse transformation for the three-phase voltages are given by:

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \qquad \text{(A.1)}$$

and,

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix}. \qquad \text{(A.2)}$$

Similar equations are also valid for the instantaneous three-phase currents.

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