Optimizing the Voltage Mode Control Loop of a Buck Converter for Point-of-Load Microprocessor Applications

Ognjen Djekić* and Slobodan Ćuk
Power Electronics Group
Caltech, EE136-93, Pasadena, CA 91125, USA
Phone: (626) 395-4711, Fax: (626) 792-1784
Email: auggie@its.caltech.edu

***Abstract* – A correlation is made between the shape of the closed loop output impedance of a buck converter and its load transient response. This correlation is used to design the voltage mode feedback loop that achieves an optimum load transient response for VRM applications. Additionally, a formula that predicts the peak output voltage deviation as a function of the loop gain crossover frequency is derived. The design approach was validated on a prototype that meets Intel Pentium III transient response specs.**

I. Introduction

The demand for faster, more powerful computers keeps pushing microprocessor manufacturers to pack more computational power and more features into each new generation of microprocessors. As a result, the power requirements of a microprocessor, as well as the on-chip power dissipation, have steadily been increasing. As this trend continued, adequate cooling of the processor, and the entire system, became an issue. In order to deal with the on-chip power dissipation, the processor core logic supply voltage had to be lowered. A lower core logic operating voltage reduces the processor power requirements providing the clock frequency remains unchanged. In other words, for a given power dissipation, a processor with a lower core logic operating voltage can run at a higher clock frequency. Hence, it is quite clear that future high performance microprocessors will continue to migrate to lower core supply voltages and higher operating currents making power distribution and delivery increasingly difficult.

As the processor core logic supply voltage is reduced, more precise signal voltage levels are required to insure error-free operation. Under the circumstances, microprocessor manufacturers have had to impose very stringent requirements on both the static and the transient output voltage regulation of the point-of-load modules powering the CPU. A portion of the latest Pentium III VRM electrical specifications is given in Table I [1]. Meeting these specs requires careful optimization of both the power stage and the control loop. This paper will focus on the design and optimization of the voltage mode control loop. An optimized control loop can save microfarads of output capacitance, thus reducing the size and the cost of the point-of-load module.

One way to approach the loop design of a point-of-load module is to use SPICE to simulate the entire circuit. However, this process is time consuming, and yields little insight into which circuit parameters need to be changed to improve the transient response of the converter. An alternative to "brute force" simulation, as it was pointed out in [2], [3] and [4], is the design oriented approach that uses the output impedance of the converter to predict its transient response. This approach was used in [4] to optimize the load transient response of a synchronous buck converter designed to meet the Pentium II VRM specifications.

TABLE I
VOLTAGE AND CURRENT SPECIFICATIONS FOR 2.0V PENTIUM III (K) PROCESSORS

Symbol	Parameter	µP frequency (MHz)	Min	Typ	Max	Unit
Vcc_{core}	Vcc for µP core			2.0		V
	Static tolerance at VRM pins on system board	(K) 450-500	-0.060		0.070	V
	Transient tolerance at VRM pins on system board		-0.130		0.130	V
Icc_{core}	Current for Vcc_{core}	(K) 450 (K) 500			14.5 16.1	A
Icc_{sgnt}	Icc for Stop-Grant Vcc_{core}				0.8	A
$\frac{dIcc_{core}}{dt}$	Icc slew rate				20	A/µs

In [4] the authors propose the use of constant off-time current mode control. This control method inherently offers attractive features like the relative ease of closing the loop and the information about the load current that can be used to achieve the ideal load transient response by offsetting the nominal output voltage depending on the load current. Another control method suitable for microprocessor power applications is summing mode control proposed in [5]. Summing mode control is similar to typical current mode control methods, but is claimed to have a much higher bandwidth, and thus a better transient response. While current mode control schemes advocated in [2], [4] and [5] demonstrate good transient response, it comes at the expense of reduced efficiency. A 7mΩ current sensing resistor will reduce the efficiency of the module by 2-3% depending on the output voltage.

In this paper, we will demonstrate how to use the closed loop output impedance of a buck converter to design and optimize a voltage mode control loop that will achieve a transient response similar to the ones reported in [4] and [5] without sacrificing efficiency. This loop design method eliminates the need for time-consuming simulation of the entire circuit and offers direct insight into where the compensation poles and zeros need to be placed to achieve the desired transient response. In addition, we will be able to derive a simple formula that accurately predicts the peak output voltage deviation due to a load current transient as a function of the output capacitance and the loop gain crossover frequency.

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The voltage mode control loop will be optimized for a 12V to 2.0V synchronous buck converter intended to meet the specifications set forth in [1]. An overview of the buck converter transient response is given in Section II. Section III examines the conventional voltage mode loop design. Section IV introduces the concept of optimum transient response, and Section V explains how to achieve it with voltage mode control. Sections VI and VII are devoted to transient response simulation and peak output voltage determination, respectively. Experimental results are presented in Section VIII, and conclusions in Section IX.

II. Overview of the Buck Converter Load Transient Response

A closed loop buck regulator with voltage mode control is shown in Fig. 1. The output of the regulator is connected to a dynamic (microprocessor) load. The load's current requirements can change from almost zero to 12.5A in a fraction of the regulator's switching period. A typical regulator response to a load current change with a slew rate of 20A/µs (Fig. 2a) occurring at $t=t_0$ is sketched in Fig. 2b. Fig. 2b shows that after a load current transient, the output voltage begins to droop because of the power supply's inherent inability to instantly change its operating point. The controller senses the output voltage error and attempts to correct it. Eventually, integral action of the control loop eliminates any steady state error in the output voltage and returns it to its nominal value, as shown in Fig. 2b. Between the time when the load current transient occurs and when the regulator output voltage returns to its nominal value, four distinct response intervals, I_1 through I_4, can be identified.

The first interval, I_1, coincides with the rise-time of the load current; I_2 represents the time needed by the control loop to react to the disturbance; I_3 is the time it takes the average inductor current to become equal to the load current, and I_4 is the interval during which the output voltage recovers to its nominal value after reaching its minimum value at $t=t_3$.

A. Interval I_1

Since $\Delta t_1=t_1-t_0$ is much shorter than the switching period, the control loop cannot immediately react to this disturbance. Thus, the converter initially responds to the

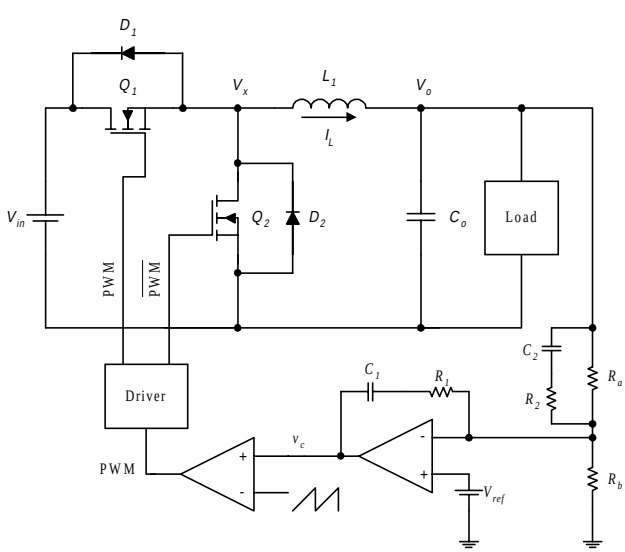

Fig. 1. Closed loop buck regulator with voltage mode control

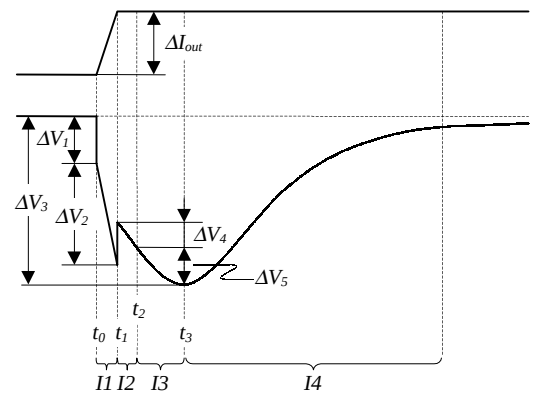

Fig. 2. Typical transient response of a synchronous buck converter to a load current step occurring at $t=t_0$

sudden change in the load current in an open loop fashion. As a result, during I_1, the control loop can simply be omitted, and the circuit of Fig. 1 can be modeled as shown in Fig. 3. In Fig. 3, the buck inductor is modeled by a constant current source; the equivalent series resistance and the equivalent series inductance of the output capacitors (*ESR* and *ESL*, respectively) have also been included, as they contribute to the output voltage deviation.

The output voltage deviation during Δt_1, ΔV_{o1}, can be calculated using the following expression:

$$\Delta V_{o1} = Z_o \cdot I_o, \tag{1}$$

where Z_o is the open loop output impedance of the converter, and I_o is the ramping load current.

From Fig. 3, it can, by inspection, be determined that Z_o is the impedance of the output capacitors. At the frequency of the load current slew rate, Z_o is dominated by the *ESR* and *ESL* of the output capacitors, but the discharge of the output capacitor has been included for completeness. Consequently, the resulting peak output voltage drop during I_1 can be calculated using (2).

$$\Delta V_{o1} = \Delta V_1 + \Delta V_2 = ESL\frac{dI_o}{dt} + ESR \cdot \Delta I_o + \frac{1}{2}\frac{\Delta I_o^{\,2}}{C_o \frac{dI_o}{dt}} \tag{2}$$

From (2), it is clear that ΔV_{01} depends on the number and the quality of output capacitors, and the magnitude and the slew rate of the load current step; ΔV_{01} *does not* depend on any feedback loop parameters.

B. Interval I_2

At $t=t_1$ the load current had ramped up to its final value, and the controller still had not had time to respond. Since we are primarily interested in the maximum output voltage deviation, let us assume that the controller turns the main switch (Q_1) on at $t=t_2$, after the worst case delay, t_d, given

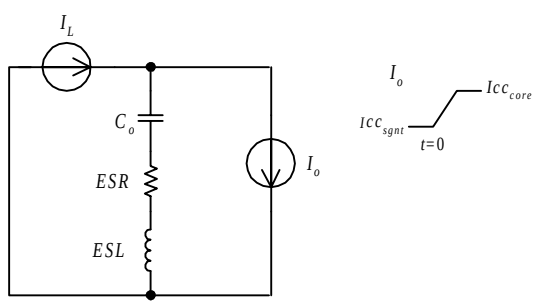

Fig. 3. Equivalent model of the buck regulator output during I_1

by:

$$t_d = D'T_s + t_p = t_2 - t_1 = \Delta t_2 \,, \tag{3}$$

where D' is the duty ratio of the synchronous rectifier, T_s is the switching period, and t_p is the propagation delay through the PWM comparator and the MOSFET driver. During Δt_2, the full load current discharges the output capacitors causing the worst case output voltage drop to be:

$$\Delta V_4 = \frac{\Delta I_o}{C_o} \Delta t_2 \,, \tag{4}$$

where C_o is the total output capacitance. Equation (4) shows that ΔV_4 is determined by the value of the output capacitor, the magnitude of the load current step, and the worst case delay, t_d, which, in turn, depends on the switching frequency, and the duty cycle, D; again, like ΔV_{01}, ΔV_4 *does not* depend on any feedback loop parameters since the loop has not had enough time to respond to the disturbance.

C. Interval I_3

At $t=t_2$, the controller finally turns Q_1 on, and the feedback loop attempts to correct the output voltage to its nominal value. During the ensuing time interval, $\Delta t_3 = t_3 - t_2$, the inductor current starts to ramp up, but the output voltage continues to decrease until the average inductor current becomes equal to the load current at $t=t_3$.

During I_3, the duty cycle (D) may or may not saturate (keep Q_1 on for more than one whole switching period). If D saturates, the formula given in [6] can be used to calculate ΔV_5. This formula can be used in cases when the buck inductor is too large to change its state within one switching cycle and the feedback has enough gain to command a unity duty cycle based on the disturbance until the inductor current becomes equal to the load current. If, on the other hand, the duty cycle does not saturate either because the inductor can change its state quickly or because the loop doesn't have enough gain to command a unity duty cycle, the formula given in [6] will not apply. Instead, a formula that takes into account the dynamics of the control loop should be used to calculate ΔV_5. Such a formula will be derived in Section VII.

If the duty cycle does not saturate during I_3, the converter of Fig. 1 can be modeled by its Thevenin equivalent circuit shown in Fig. 4. The Thevenin equivalent model takes into account the action of the control loop which results in the regulation of the output voltage and a modification of the open loop output impedance of the converter. Thus, the Thevenin voltage source, V_{TH}, is the regulated output voltage; the Thevenin impedance, Z_{TH}, is equal to the closed loop output impedance of the converter, Z_{of}. The closed loop output impedance can be expressed as:

$$Z_{TH} = Z_{of} = \frac{Z_o}{1+T} \,, \tag{5}$$

where Z_o is the open loop output impedance of the converter, and T is the loop gain, both of which can easily be calculated using standard small signal modeling methods.

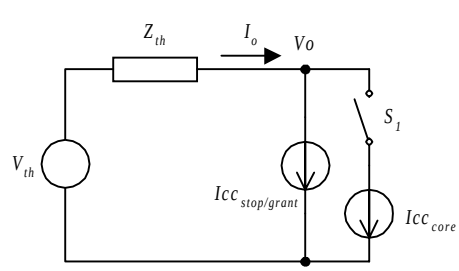

Fig. 4. The Thevenin equivalent model of a buck regulator output during I_3 and I_4

D. Interval I_4

At $t=t_3$, the average inductor current becomes equal to the load current. Consequently, after $t=t_3$ the output capacitors will start to recharge to their nominal voltage.

During I_4 the converter remains in the normal mode of operation dictated by the control loop. Therefore, the Thevenin equivalent model used to model the converter during I_3 remains valid during I_4.

III. Conventional Loop Compensation

In the previous section it was pointed out that the designer's ability to influence the shape of the load transient response using the control loop is limited to intervals I_3 and I_4. Thus, these two intervals will be the focus of the remainder of this work.

In a typical power supply application, the primary goal of a design is to tightly regulate the output voltage. In addition, the regulator will most likely be required to respond to relatively infrequent changes in the load current that certainly do not have the dynamics or the magnitude required by Pentium microprocessors [1]. Consequently, transient response is frequently a secondary concern. Under the circumstances, the voltage feedback loop is usually compensated in such a way to achieve a dominant low-frequency pole, single slope, loop gain characteristic. Closing the loop in this manner insures a tight output voltage regulation due to a high DC gain, and a reasonably good transient response depending on the achieved bandwidth.

The load transient response of a buck converter with a conventional voltage loop can be examined with the help of the Thevenin equivalent model of Fig. 4. When the switch S_1 is closed, it produces a step change in the load current. From Fig. 4 we can by inspection write an expression for the output voltage, V_o:

$$V_o(s) = \frac{V_{th}}{s} - Z_{th}(s) \cdot \frac{I_o}{s} \,. \tag{6}$$

It should, however, be pointed out that (6) is valid only if the duty cycle does not saturate after the step change in the load current. In this case, even though $I_o(t)$ is not a small signal perturbation, the mode of operation of the converter does not change. As a result, small signal models used to derive (6) are still valid, despite the temporary increase of the duty cycle.

In order to calculate the transient response using (6), $Z_{TH}(s)$ needs to be calculated. As it turns out, $Z_{TH}(s)$ can easily be determined graphically. First, $|Z_o|$ is sketched, as shown in Fig. 5a. Since the common single slope loop gain characteristic is assumed, $|T|$ and $|1+T|$ can easily be plotted as shown in Fig. 5b; $|Z_{TH}|$, given in Fig. 5c, is obtained by simply "doing the algebra on the graph", i.e. graphically adding $|Z_o(s)|$ and $|1+T|$. From Fig. 5c, an

expression for $Z_{TH}(s)$ can be written by inspection. Substituting this expression back into (6) results in a frequency-domain expression for the output voltage.

Fig. 5c shows that with single slope loop gain, the output impedance starts to quickly decrease below ω_0, and becomes vanishingly small at low frequencies. When this result is substituted in (6), it becomes clear why the output voltage quickly returns to its nominal value after any kind of disturbance. Consequently, the peak to peak voltage deviation due to a loading transient followed by an unloading transient is approximately equal to twice the peak output voltage deviation due to a loading transient alone. If, on the other hand, the output voltage were to stay at, or close to, the lowest level it had reached after the loading transient, extra headroom would be available for the unloading transient; the peak to peak output voltage deviation could approximately be reduced in half.

IV. Optimum Load Transient Response

It is by now apparent that the single slope loop gain is not the best way to close the loop in Pentium power supply applications. Instead, the system behavior during intervals I_3 an I_4 needs to be influenced by the control loop to minimize ΔV_5 (see Fig. 2) and control the output voltage recovery during I_4. Therefore, once the power stage components and the switching frequency have been chosen based on (1)-(4), optimum control loop design can be undertaken. If ΔV_3 (see Fig. 2) can be brought within static tolerances, the loop should be designed to minimize ΔV_5 and realize the response shown with a dashed line in Fig. 6. Otherwise, as will most likely be the case, the loop should still minimize ΔV_5, but will, in this case, have to achieve the response shown with a solid line in Fig. 6, and allow the output voltage to return to within the static tolerance limit.

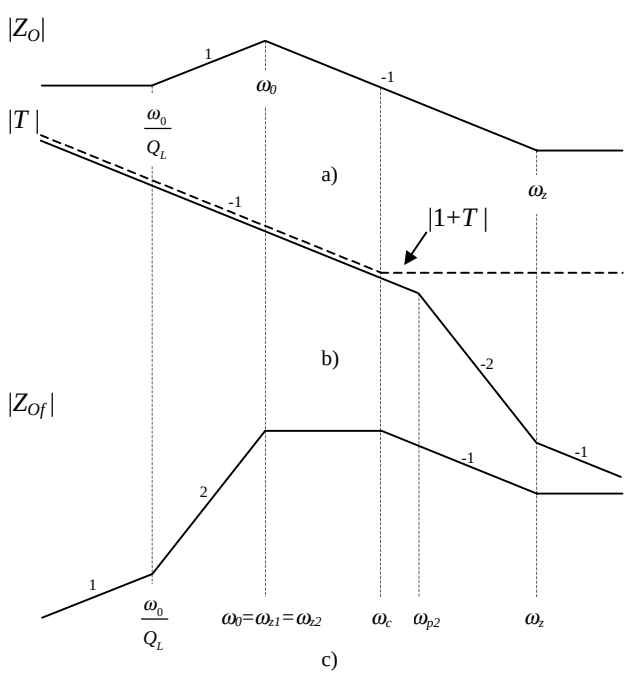

Fig. 5. a) Typical open loop output impedance of a buck converter, b) Single slope loop gain, c) Closed loop output impedance

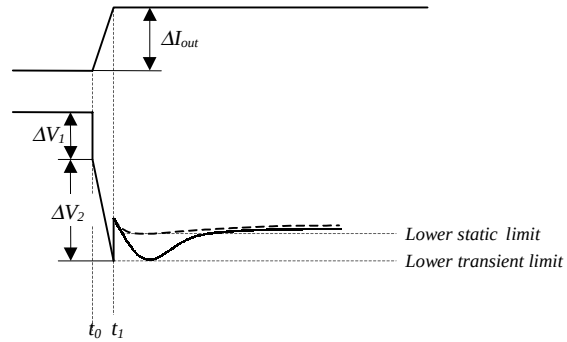

Fig. 6. Typical transient response of a synchronous buck converter to a load current step occurring at $t=t_0$

V. Achieving Optimum Transient Response with Voltage Mode Control

With voltage mode control the information about the value of the average inductor current is not available. Hence, it is not possible to offset the output voltage based on the value of the inductor current. Instead, the desired transient response shown in Fig. 6 needs to be achieved by clever loop design.

The problem with conventional single slope loop gain in the context of the optimum transient response in microprocessor applications was clearly outlined by (6) and Fig. 5c. The rapid decrease of $|Z_{of}|$ below ω_0 is undesirable, and should be eliminated through more suitable loop compensation.

An examination of Fig. 4 in conjunction with (6) leads to a conclusion that the dashed-line response in Fig. 6 requires:

$$Z_{TH}=R_{TH}=const. \tag{7}$$

Similarly, the solid line response shown in Fig. 4 could be realized with:

$$Z_{TH}=\begin{cases} R_1=const., f \geq f_m \\ R_2 < R_1 = const., f \leq f_m \end{cases} \tag{8}$$

where $1/f_m$ must be less than or equal to the time during which the output voltage can be outside the static limits [1]. Since the general shape of Z_o of a buck converter is predetermined, equations (7) and (8) define the shape of the loop gain that needs to be achieved.

A typical open loop output impedance of a synchronous buck converter is shown in Fig. 7a. In Fig. 7 $\omega_0 = 1/\sqrt{LC_o}$ is the filter corner frequency, $Q_L = R_0/R_l$ is the Q factor associated with the series resistance of the inductor, R_l, $R_0 = \sqrt{L/C_o}$ is the characteristic impedance, and $\omega_z = 1/(ESR \cdot C_o)$ is a zero due to the ESR of the output capacitors. The loop gain required to achieve Z_{TH} described by equations (7) and (8) is given in Fig. 7b by the dashed and the solid line, respectively. In Fig. 7b ω_{z1}, ω_{z2}, and ω_{p1}, ω_{p2} are the two compensation zeros and the two compensation poles, respectively, and ω_c is the loop gain crossover frequency.

Shaping the loop as shown in Fig. 7b results in a closed loop output impedance presented in Fig. 7c. Figures 7b

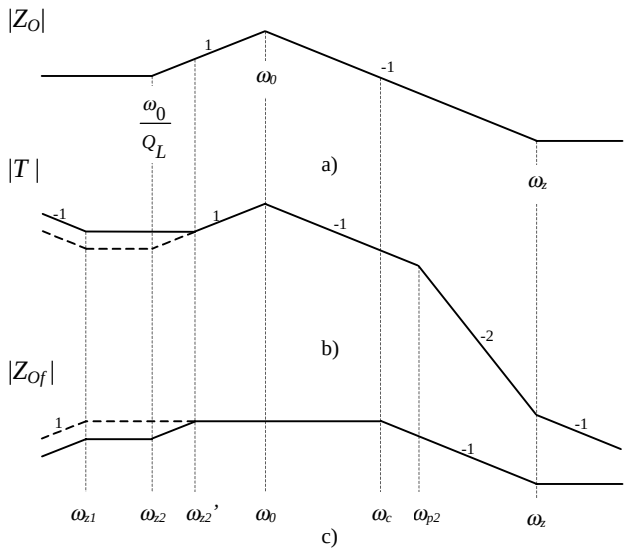

Fig. 7. a) A typical open loop output impedance of a buck converter, b) Targeted loop gain, c) Optimum closed loop output impedance

and 7c demonstrate that only the location of the compensation zero ω_{z2} determines whether Z_{of} approximates equation (7) or (8). If ω_{z2} is placed at $\frac{\omega_0}{Q_L}$, Z_{of} approximates (7) (see the dashed line in Figs.7b and 7c) and results in the dashed transient response in Fig. 6. On the other hand, if ω_{z2} is placed between $\frac{\omega_0}{Q_L}$ and ω_0, Z_{of} approximates (8) (see the solid line in Figs. 7b and 7c) and yields a transient response shown with a solid line in Fig. 6.

Further examination of Fig. 7 reveals that the compensation zero ω_{z1} and its associated pole (assumed to be at zero frequency and not shown), ω_{p1}, actually hurt the transient response by reducing Z_{of} at low frequencies. In fact, without this pole-zero pair, Z_{of} would have the exact shape needed to achieve the ideal transient responses shown in Fig. 6. Unfortunately, if this pole-zero pair were omitted from the compensation, the integral action of the control would be eliminated, and the required tight static voltage regulation could not be achieved. Therefore, some transient performance has to be traded for static voltage regulation.

Since ω_{z1} and ω_{p1} cannot be omitted from the compensation, their location has to be chosen carefully to minimize their effect on the transient performance. Namely, in Z_{of} ω_{z1} becomes a dominant low frequency pole. The location of this pole determines the rate of the output voltage recovery after a load transient. As it turns out, [1] specifies a load toggle rate of 100Hz to 100kHz. Therefore, placing the dominant low frequency pole (compensation zero ω_{z1}) in Z_{of} far below 100Hz insures that the output voltage will not significantly recover before the worst case unloading transient (100Hz) happens, thus providing the needed additional headroom for the transient response. The pole ω_{p1} can be placed anywhere from a decade below ω_{z1} all the way to zero frequency, depending on the static voltage regulation requirements. Placing ω_{p1} above zero frequency results in a finite closed loop output impedance at DC, and thus, in a finite output voltage offset (steady state error).

VI. Analysis and Simulation

Once the shape of the closed loop output impedance has been determined by "doing the algebra on the graph", we can by inspection write the expression for Z_{of}. If $\frac{\omega_0}{Q_L} < \omega_{z2} < \omega_0 = 1/\sqrt{LC_o}$, Z_{of} is drawn with a solid line in Fig. 7c, and can be expressed as:

$$Z_{of}(s) = ESR\frac{\left(1+\frac{\omega_z}{s}\right)\left(1+\frac{\omega_0/Q_L}{s}\right)}{\left(1+\frac{\omega_c}{s}\right)\left(1+\frac{\omega_{z1}}{s}\right)\left(1+\frac{\omega_{z2}}{s}\right)}. \tag{9}$$

In a special case, when $\omega_{z2} = \omega_0 = 1/\sqrt{LC_o}$, Z_{of} takes the shape shown with the dashed line in Fig. 7c, and (9) reduces to:

$$Z_{of}(s) = ESR\frac{\left(1+\frac{\omega_z}{s}\right)}{\left(1+\frac{\omega_c}{s}\right)\left(1+\frac{\omega_{z1}}{s}\right)}. \tag{10}$$

Substituting (9) and (10) into (6), respectively, and rearranging, we get:

$$V_o(s) = \frac{V_{th}}{s} - \Delta I_o \cdot ESR\frac{(s+\omega_z)(s+\omega_0/Q_L)}{(s+\omega_c)(s+\omega_{z1})(s+\omega_{z2})} \tag{11}$$

$$V_o(s) = \frac{V_{th}}{s} - \Delta I_o \cdot ESR\frac{(s+\omega_z)}{(s+\omega_c)(s+\omega_{z1})} \tag{12}$$

Equations (11) and (12) are frequency domain expressions for the converter output voltage during I_3 and I_4. The Mathematica™ software package can be used to calculate the inverse Laplace transform of (11) and (12) and plot the resulting time-domain converter output voltage behavior during I_3 and I_4. Simulation results for two compensation networks designed to approximate (7) and (8) are given in Fig. 8 by the dashed and the solid line, respectively.

Using Mathematica's built-in inverse Laplace function, predicting and plotting the load transient response of the converter takes only a few seconds compared to several minutes required for a SPICE simulation on a Pentium II 450MHz workstation.

Mathematica is an efficient tool for calculation and plotting of the time-domain transient response. However, doing the task analytically yields significant additional

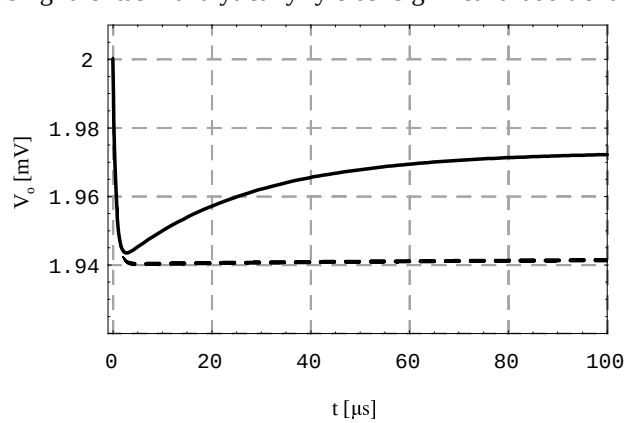

Fig. 8. Simulated converter transient response during I_3 and I_4

design insight.

Taking the inverse Laplace transform of (11) and (12) yields time-domain equations for the converter output voltage given by (13) and (14), respectively.

$$V_o(t) = V_{TH} - \Delta I_o \cdot ESR \cdot (A_1 e^{-\omega_c t} + A_2 e^{-\omega_{z1} t} + A_3 e^{-\omega_{z2} t}) \quad (13)$$

$$V_o(t) = V_{TH} - \Delta I_o \cdot ESR \cdot (A_1 e^{-\omega_c t} + A_2 e^{-\omega_{z1} t}) \quad (14)$$

where A_1, A_2, and A_3, are constants. Equations (13) and (14) show that the converter response during I_3 is a function of the loop gain crossover frequency, ω_c, and the compensation zeros, ω_{z1} and ω_{z2}. Furthermore, since $\Delta V_o(t)$ in both (13) and (14) is a sum of decaying exponential terms, the shape of the transient response can be controlled by appropriately adjusting the time constant of each of the exponential terms. In other words, if ω_c, ω_{z1} and ω_{z2} are properly chosen, the transient response can be made to resemble the waveforms in Fig. 6. This is actually a mathematical restatement of Fig. 7; choosing appropriate time constants is equivalent to shaping the closed output impedance according to (7) and (8). The added value of (13) and (14) lies in the opportunity to examine the contribution of each exponential term to the overall transient response and derive closed form expressions for peak voltage deviation.

VII. Calculating the Peak Voltage Deviation

Equation (14) is particularly suitable for obtaining a closed form expression for the peak output voltage deviation during I_3. Finding the peak voltage deviation in this case is equivalent to finding the maximum of the expression to the right of the minus sign in (14). Taking the first derivative of this expression, setting it equal to zero, and solving for t yields the time t_{min} at which the output voltage reaches its lowest level:

$$t_{\min} = \frac{1}{\omega_c - \omega_{z1}} \ln\left(-\frac{A_1 \cdot \omega_c}{A_2 \cdot \omega_{z1}} \right). \quad (15)$$

Substituting t_{min} back into (14), and making the appropriate approximations, we get an expression for the peak output voltage deviation during I_3:

$$\Delta V_5 \approx \frac{\Delta I_o}{\omega_c C_o} \left(\frac{\omega_{z1}}{\omega_c} \right)^{\frac{\omega_{z1}}{\omega_c}} \quad (16)$$

VIII. Experimental Verification

Theoretical results were verified on a prototype synchronous buck converter. The input voltage was chosen to be 12V, and the nominal output voltage was 2.0V. A voltage mode feedback loop was designed based on (7), (8) and Fig. 7, and implemented as shown in Fig. 1. The loop was designed for f_{z1}=20Hz, $f_{z2}=\frac{f_0}{Q_L}$=2.7kHz, and f_c=250kHz. The transient response was measured for a load current step from 0.1 to 15A with a slew rate of 60A/µs and a frequency of 100Hz. A plot of the converter output voltage is shown in Fig. 9 on a 50mV/division scale.

Fig. 9 shows the worst case peak to peak output voltage deviation due to a 15A load transient to be only 160mV.

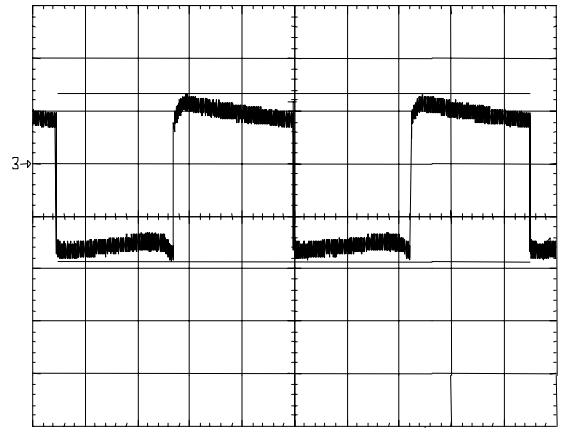

Fig. 9. The output voltage of the point-of-load module under the worst case transient conditions (load frequency = 100Hz)

This deviation is in fact within the static voltage tolerance specified in [1] with only 160µF of output capacitance. The experimental results also verified the validity of (16): peak measured deviation during I_3 was 56mv versus 60mV predicted by (16) and demonstrated in Fig. 8.

IX. Conclusion

In this paper we have shown how to correlate the desired time domain converter response to a step load current change with the shape of its closed loop output impedance. The closed loop output impedance is then used to determine the optimum shape of the loop gain and thus, the optimum location of the compensation poles and zeros. Since all relevant equations can be written by inspection, this design-oriented approach doesn't require any lengthy derivations, and offers immediate insight into how each compensation pole and zero affects the transient response of the converter. Thus, the proposed method insures that the desired load transient response can be achieved without time-consuming trial and error loop design using a circuit simulation tool.

The validity of the voltage mode loop design based on the closed loop output impedance was experimentally verified on a prototype buck converter built using exclusively surface mount parts. Tight static voltage regulation and the desired shape of the converter transient response were achieved by proper feedback loop design. A transient response typically available with current mode control schemes was realized with pure voltage mode control. Hence, by eliminating the current sensing resistor the overall efficiency of the module was improved by 2-3% without degrading the transient response.

X. References

[1] Intel document, "VRM 8.2 DC-DC Converter Design Guidelines", Order Number: 243773-002, March 1999.

[2] Z. Zhang, S. Ćuk, "Improving Transient Response of Switching Converters," IEEE IPEMC Record, November 1997.

[3] K. Schenk, S. Ćuk "Small Signal Analysis of Converters with Multiple Discontinuous Conduction Modes," IEEE PESC Record, pp. 623-629, 1998.

[4] R. Redl, Z. Zansky, "Optimizing the Load Transient Response of the Buck Converter", IEEE APEC Record, pp. 170-176, 1998.

[5] R. Lenk, "Summing Mode Control," PCIM Magazine, pp. 24-35, May 1999.

[6] J. O'Connor, "Converter Optimization for Powering Low Voltage, High Performance Microprocessors," IEEE APEC Record, pp. 984-989, 1996.