High Power Converters with Active Snubbers for Variable Speed Drive Applications

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Abstract— **This paper addresses the use of lossless active snubbers - resonant snubbers - in high power topologies suitable for electric drive applications. This study is primarily focused on Current Stiff Converter (CSC) topologies although the concepts are also extensive to Matrix Converter (MC) topologies. A commutation cell capable of representing all the commutation modes in these converter topologies is identified and analyzed. The discussion presented in this paper is supported by experimental data obtained from a high power CSC/MC commutation cell. Issues involved in the implementation of the commutation cell itself and MTO-thyristor characteristics relevant for their operation in CSC and MC topologies with resonant snubbers are addressed in this paper.**

I. Introduction

Lossless active snubbers, or simply resonant snubbers, have been proposed and investigated for improvement of the performance of high power PWM voltage stiff converters for variable speed drive applications [1], [2], [3]. This snubber struture has attracted a lot of attention in high power voltage stiff converter topologies (VSC), as an additional alternative among other high performance passive and active snubber structures [4], [5].

Three-phase current stiff converters (CSCs) are presently a leading structure in the medium voltages (2300 V to 6900 V)/high power (MW range) variable speed drives market. Among the CSC features, one can point out their sustained regeneration capability and improved overall reliability (overcurrent and short circuit protection, unidirectional current switches and absence of electrolytic capacitors). CSCs also present inherently low input and output dv/dt, an important characteristic considering EMC issues. The main drawbacks of classical PWM CSCs are associated to their low switching frequency, typically a few hundred Hz in GTO-based topologies, largely due to switching losses. Large AC side filter capacitors and DC bus inductor are required, increasing converter cost and size.

An important constraint on GTO-based CSCs switching frequency capability is the present snubber technology: the LRCD snubber [6], [7]. This snubber structure implies poor efficiency and device utilization. The absence of a stiff dc bus for energy recovery makes the regenerative process difficult, imposing an enormous constraint on the development of high performance snubber alternatives for CSCs. A recently introduced regenerative snubber for CSCs [8] returns the trapped energy directly to the AC mains through a baby dc bus (large electrolytic capacitors set), a line commutated inverter and a transformer. This bulky and expensive structure has to be repeated for each individual switch in the converter while maintaining all the LRCD snubber drawbacks regarding device utilization [9].

In this scenario, the active snubbers are seen as an interesting alternative, leading simultaneously to improvement in overall converter efficiency (higher switching frequency capability) and also improving device utilization. A drawback is the need of control for proper operation. Several implementations of the active snubbers have already been proposed for CSCs [2], [10], [11]. The concept has also been extended to MCs [2], [12].

This paper addresses modeling, control and modulation issues that arise in CSCs with resonant snubbers and extended to the MC case. These aspects are shown to be quite relevant considering the relatively strong connection between snubber and main converter operation. Alternatives of implementation of current stiff converters with resonant snubbers are presented, yielding prompt derivation of matrix converter topologies based on the same principles. Analysis and topological features are presented for the current stiff converters case considering the economical importance of these converters in medium voltage drives applications. The analysis presented in this paper are supported by experimental data obtained from a high power (pulsed) commutation cell based on the MTO (MOS Turn-Off thyristor) XSDM170HK (4500 V/500 A) from SPCO [13]. Issues involved in the implementation of the commutation cell itself as well as some characteristics of the MTO-thyristor relevant for the operation with resonant snubbers are addressed in this paper.

II. Characterization of resonant snubbers in Current Stiff Converters

The basic implementation of the resonant snubbers with auxiliary switches [2], [3] for voltage stiff converters (VSC) and CSCs is depicted in fig. 1. The CSC implementation of the resonant snubber is obtained basically by exchanging the dc voltage input (output) and ac current output (input) in the VSC implementation by an ac voltage input (output) and dc current output (input). Also, the forward voltage

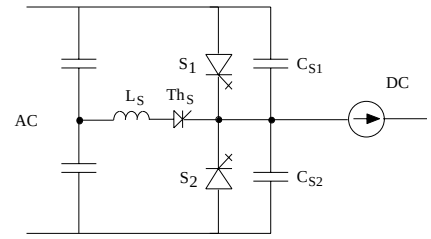
blocking, forward/reverse current conducting switches of the VSC are replaced by forward/reverse voltage blocking, forward current conducting switches in the CSC case. The same back-to-back arrangement of snubber devices shown in the VSC implementation can also be used in the CSC with advantages over the realization shown in fig. 1. The influence of the dc bus current amplitude on the commutation processes is minimized, but it implies an excessive number of additional devices (12 snubber devices) in comparison with the number of additional devices required by VSCs (6 snubber devices). The basic implementation of resonant snubbers in MCs is also given in fig. 1a, with i_{dc} replaced by ac line currents from the low frequency front end. A common-anode group of devices is added to the structure in fig. 1 to handle reverse currents. This similarity between CSCs and MCs is explored throughout this paper.

Fig. 2 shows the relevant waveforms associated with the resonant snubber implementation in CSCs and MCs. Two commutation sequences are identified in this figure. The *passive commutation sequence* takes place whenever the incoming device is reverse biased. Otherwise, external means have to be provided to create zero voltage conditions on the incoming device during its turn-on process, and the *active commutation sequence* takes place.

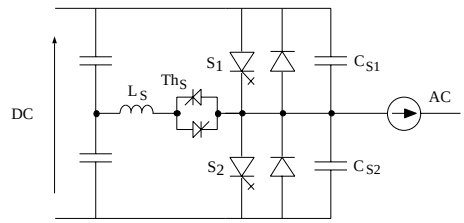
The passive commutation sequence starts when the conducting device is turned off. The dc bus current commutates to the snubber capacitors and the voltage across the devices ramps up. The incoming device starts conducting at the zero crossing instant of the voltage across its terminals. The active commutation sequence implies the introduction of a resonant mode to drive the voltage across the incoming device down to zero. This sequence starts by turning on the snubber device. The current through the snubber inductor ramps up, reaching the dc bus current amplitude. At this instant, the outgoing device is turned off under zero current conditions. Since no device is conducting, a resonant mode between the snubber inductor and capacitors takes place. The charge in the snubber capacitor across the incoming device is transferred to the one across the outgoing device (reverse biased) and the incoming device turns on under zero voltage conditions.

The resonant snubber implementation in CSC/MC topologies in fig. 1 can be generalized in the form shown in fig. 3. The common-cathode group of the main devices is shown in this figure, as well as one branch formed by the series connection of the snubber device, Th_s and snubber inductor, L_s. This generalization is based on the fact that the snubber driving voltage, v_{Sb}, is in fact a control parameter. It is shown later that the three phase implementation from the single phase CSC cell in fig. 1 is but one of several realization possibilities.

The identification of v_{Sb} in fig. 3 as a control parameter moves the focus this discussion to the active commutation sequence. Without loss of generality, it is assumed that $v_{an} > v_{bn} > v_{cn}$, with $|v_{an}| < |v_{cn}|$ and the ac current modulation commands a commutation from S_5 to S_1. All the circuit components are assumed to be lossless. The



(a) CSC realization.



(b) VSC realization.

Fig. 1. Resonant snubbers with auxiliary switches.

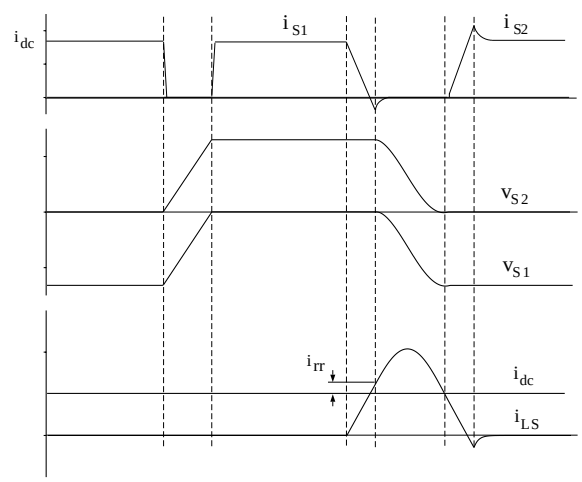


Fig. 2. Resonant snubber waveforms.

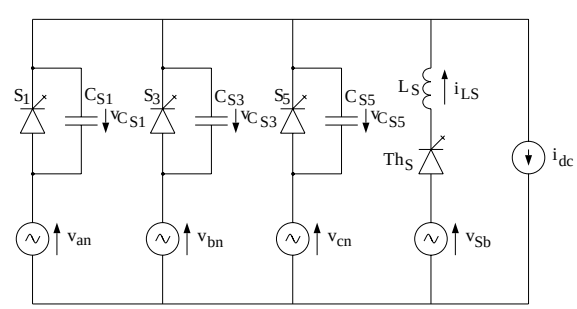


Fig. 3. Generalized CSC with resonant snubbers.

terminal ac voltages are assumed to remain constant during the commutation intervals.

Mode 1 ($t < t_0$): initial condition with switch S_5 conducting.

Mode 2 ($t_0 \leq t < t_1$): at $t = t_0$, the snubber switch Th_s is turned on. The current through the snubber inductance, i_{L_S} ramps up driven by the voltage $v_{L_S} = v_{Sb} - v_{cn}$ and $i_{L_S}(t_0) = 0$. During this mode, the snubber inductor current is given by:

$$i_{L_S}(t) = \frac{v_{L_S}(t_0)}{L_S}(t - t_0) \tag{1}$$

Mode 3 ($t_1 < t < t_2$): at $t = t_1$, the main conducting devices turn-off under either zero current or zero voltage condition with $i_{L_S}(t_1) \geq i_{dc}$ or $i_{L_S}(t_1) < i_{dc}$, respectively. With all the main devices off, a resonant mode takes place and a null current vector is applied to the ac terminals. During this mode, the voltage across the incoming device is driven down towards zero. The relevant snubber quantities are given by:

$$\begin{aligned} v_{C_S}(t) &= Z_o\left[i_{dc} - i_{L_S}(t_1)\right] sin\omega_o(t - t_1) + \\ &+ v_{L_S}(t_1)\, cos\omega_o(t - t_1) - \\ &- v_{L_S}(t_1) + v_{C_S}(t_1) \end{aligned} \tag{2}$$

$$\begin{aligned} iL_S(t) &= \frac{1}{Z_o} v_{L_S}(t_1)\, sin\omega_o(t - t_1) - \\ &- \left[i_{dc} - i_{L_S}(t_1)\right] cos\omega_o(t - t_1) + \\ &+ i_{dc} \end{aligned} \tag{3}$$

where $\omega_o, = l/\sqrt{L_s\, C_{eq}}$, $Z_o = \sqrt{L_s/C_{eq}}$ and $C_{eq} = 3C_s$.

The relative amplitude of i_{L_S} with respect to i_{dc} defines two snubber energy boost modes. The condition $i_{L_S}(t_1) \geq i_{dc}$ defines the *pseudo-active boost mode*, in contrast with the *active boost mode* defined by the condition $i_{L_S}(t_1) < i_{dc}$. These two boost modes are strongly dependent on the main devices turn-off characteristics, with the pseudo-active boost mode being completely defined by their reverse recovery process.

Mode 4 ($t_2 \leq t < t_3$): at t_2 the voltage across the incoming device, S_1, is minimum and turn on takes place under nearly or at zero voltage conditions. The current i_{L_S} ramps down. This mode is analogous to *Mode 2*.

Mode 5 ($t \geq t_3$): at $t = t_3$, i_{L_S} reaches zero and Th_s, turns off under zero current condition.

Eq. (2) above can be used to obtain the voltage across any of the main devices by plugging in the respective initial snubber capacitor voltage, $v_{C_S}(t_1)$. From (1) and (2), a *necessary and sufficient condition* for zero voltage switching of the incoming device is given by:

$$[v_{Sb} - v_{cn}]^2 + Z_o^2\left[i_{L_S}(t_1) - i_{dc}\right]^2 \geq [v_{Sb} - v_{an}]^2 \tag{4}$$

where $v_{Sb} = v_{L_S}(t_1) + v_{cn}$.

It can be also shown that zero voltage switching of the incoming device in the common-cathode group is obtained if:

$$v_{Sb} \geq \frac{v_{an} + v_{cn}}{2} \tag{5}$$

The conditions expressed in (4) and (5) can be promptly generalized by recognizing v_{an}, and v_{cn}, as the phase voltages associated with the incoming and outgoing devices $v_{fn,in}$ and $v_{fn,out}$, respectively. Similar analysis can be performed for the common-anode group of devices. In the latter case, the inequality sign in (5) must be reversed. Equation (5) defines a *sufficient condition* for the turn-on of the incoming device under zero voltage, regardless of the amplitude of $i_{L_S}(t_1)$ with respect to i_{dc}.

Fig. 4 shows phase plane plots of the snubber quantities during the resonant mode for several values of $i_{L_S}(t_1)$. Notice that $i_{L_S}(t_1) - i_{dc} = i_{rr}$ is the reverse recovery current through the main devices. In all plots, $v_{Sb} = (v_{fn,in} + v_{fn,out})/2$. It is seen that minimum ratings for the snubber components are obtained for $i_{L_S}(t_1) = i_{dc}$. This condition also implies to minimum voltage stress on the main converter devices. From the perspective of minimum ratings of the snubber components and zero voltage stress on the main devices, the situation where $v_{Sb} = (v_{fn,in} + v_{fn,out})/2$ and $i_{L_S}(t_1) = i_{dc}$, corresponds to an *optimal commutation condition*.

From (1) and (5), the time interval required to drive i_{L_S} from zero to i_{dc}, (*Mode 2*) is given by:

$$t_1 - t_0 = \frac{2\, L_s\, i_{dc}}{v_{fn,in} - v_{fn,out}} \tag{6}$$

From (6), it is seen that the condition $i_{L_S}(t_1) = i_{dc}$ introduces a dwell time that is an inverse function of the difference between the phase voltages associated with the devices undergoing commutation. This dwell time becomes excessive long as this voltage difference diminishes due to commutation occurring close to the zero crossing of the line voltage involved in the process. If the interval $t_1 - t_0$ is limited such that $t_1 - t_0 \leq \Delta t_{dw}$, then the current through the snubber inductor at the end of *Mode 2* is such that $i_{L_S}(t_1) \leq i_{dc}$, when the line voltage goes below a certain limit. As discussed in the previous paragraphs, this condition does not affect the operation of the snubber, as long as condition (5) is satisfied. In fact, the limitation of the duration of *Mode 2* is a simple way to overcome the dwell time problems introduced by operation at low ac voltage levels in variable voltage applications without exceeding the voltage rating of the converter devices.

For rated operating conditions, on the other hand, it is desirable to eliminate any additional voltage stress on the devices, implying that optimal or near optimal active commutation conditions should be introduced. From (6) it is seen that in order to constrain the dwell time or maximize i_{L_S} within a certain time interval, the amplitude of the line voltage involved in the active commutation process has to be maximized. This condition can be obtained by restricting the active commutation process to commutation be-

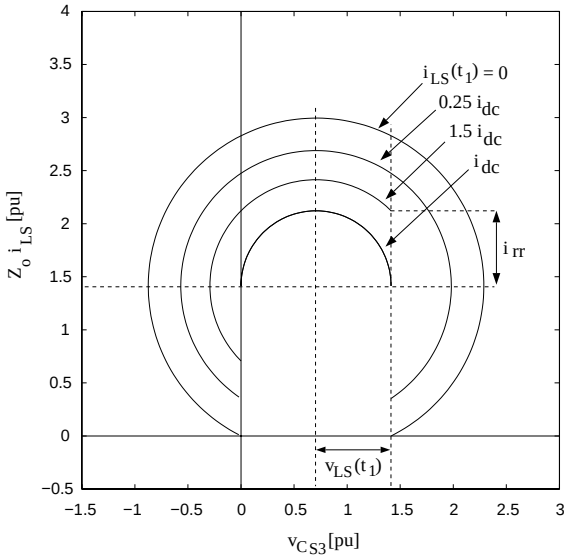


Fig. 4. Active commutation - *Mode 3*.

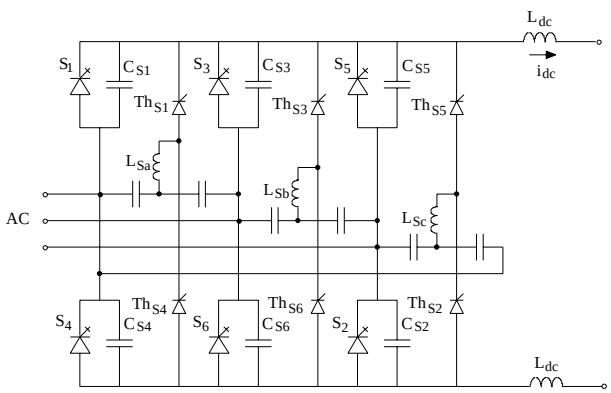


Fig. 5. AVD realization.

tween devices associated with the maximum instantaneous line to line voltage. Although effective, this scheme introduces further constraints on the converter compatibility with pulse width modulation (PWM).

III. Three-phase realizations

A. Average Voltage Driven (AVD) realization

In practical implementations, the sufficient condition in 4 can be very closely approximated with the topology depicted in fig. 5 [2], [3]. In this topology, the basic snubber structure in fig. 1 is reproduced for each pair of devices potentially undergoing commutation. The total number of snubber inductors is reduced by recognizing that the common-cathode and common-cathode devices groups do not undergo commutation simultaneously. The snubber driving voltage condition expressed by (5) is met by means of a series connection of the ac filter capacitors and employing the center tap voltage to drive the snubber inductor/device branch.

Although suitable commutation conditions exist for any pair of devices in both positive and negative groups, significant dwell time intervals can result if optimal commutation conditions are to be obtained, as pointed out previously. This situation is somewhat similar to the one encountered in VSC topologies with resonant snubbers at the zero crossings of the ac currents. As it was proposed in the previous section, this problem is minimized if the converter operation is constrained to a set of feasible switching patterns that maximize the snubber inductor voltages during *Mode 2* of the active commutation process. This condition is met if active commutation occur between devices associated to the maximum line to line voltage amplitude at any instant, implying that the snubber inductor voltage is not only maximized but it is also constrained to a fairly narrow range $(\sqrt{3}/2)V_{LL,peak} \leq v_{L_S}(t_1) \leq V_{LL,peak}$. Significant simplification of the design of the snubber inductor is also obtained from the minimization of the inductor voltage fluctuations.

Fig. 7 shows a space vector diagram where a lagging displacement power factor condition is illustrated. A suitable switching sequences for this operating conditions is:

$$\vec{i}_1 \xrightarrow{p} \vec{i}_6 \xrightarrow{p} \vec{i}_0 \xrightarrow{a} \vec{i}_1 \cdots \tag{7}$$

where $\xrightarrow{p}$ and $\xrightarrow{a}$ indicate passive and active commutation sequences, respectively. The vector sequence leading to only one active commutation per switching period can be obtained for any vectors $\vec{v}_s$ and $\vec{i}^*$ from the three converter current vectors $\vec{i}_{xyz}$ (including a null vector) adjacent to $\vec{i}^*$, according to the pattern:

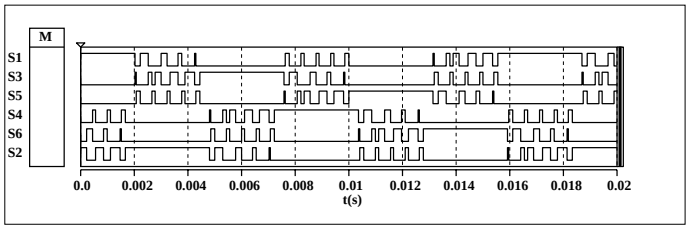
$$\begin{aligned} max(|\vec{v}_s \cdot \vec{i}_x|) &\xrightarrow{p} \quad |\vec{v}_s \cdot \vec{i}_y| \quad \xrightarrow{p} \\ &\xrightarrow{p} \quad min(|\vec{v}_s \cdot \vec{i}_z|) \quad \xrightarrow{a} \\ &\xrightarrow{a} \quad max(|\vec{v}_s \cdot \vec{i}_x|) \ldots \end{aligned} \tag{8}$$

Notice that the resultant switching function implies an inversion in the relative position of the vectors within a switching period six times for each complete cycle of the fundamental ac current, as shown in fig. 6. This characteristic leads to low frequency harmonic distortion of the output current (more significant at low switching frequencies).

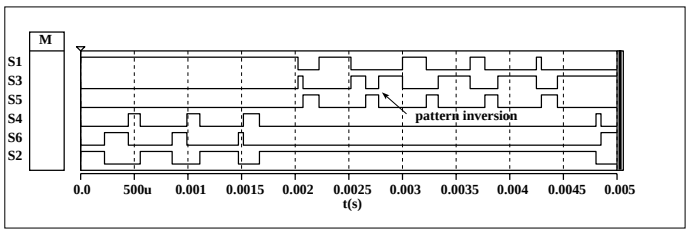
Modulation intervals can be computed from direct application of the space vector modulation equations to current stiff converters:

$$\begin{aligned} t_m &= \frac{T}{i_{dc}} (-i^*_{qs}\, sin\, \theta_n - i^*_{ds}\, cos\, \theta_n) \\ t_n &= \frac{T}{i_{dc}} (i^*_{qs}\, sin\, \theta_m + i^*_{ds}\, cos\, \theta_m) \end{aligned} \tag{9}$$

where t_m and t_n are the injection intervals of the non-null current vectors $\vec{i}_m$ and $\vec{i}_n$, respectively, and $\vec{i}_m$ leads $\vec{i}_n$ by $\pi/3$; i^*_{qs} and i^*_{ds} are the components of $\vec{i}^*_s$; in the stationary reference frame in fig. 7. Notice that in the switching patterns (7) one device remains on for the entire switching interval. In fact, these patterns can be identified with discontinuous PWM schemes. In this case, each device is kept on for an interval of $\pi/3\ rad$, corresponding to the interval



(a)



(b)

Fig. 6. Switching function with change in vector position.

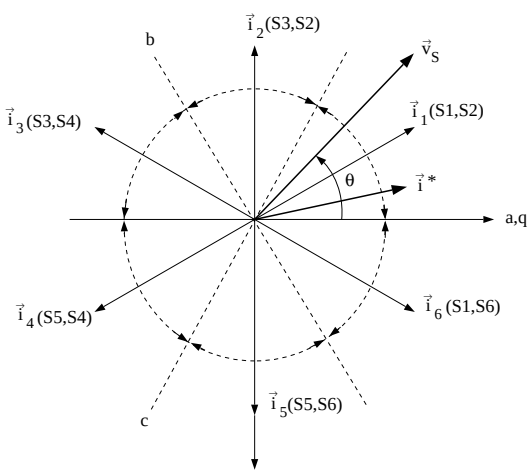


Fig. 7. Space vector diagram.

when the associated phase current has the highest amplitude. An advantage of discontinuous PWM algorithms is a significant reduction of the total number of commutations per period. The realization shown in fig. 5 is fully compatible with these algorithms, with minor modifications introduced to constrain the snubber inductor voltage in the active commutation sequence, as discussed above. Other switching patterns are also possible, but optimal commutation conditions are not guaranteed. Among the drawbacks of the *AVD* realization depicted in fig. 5, it can be pointed out the relatively large number of extra parts associated with the resonant snubber, the need to balance the voltages across the input filter capacitors and the high dv/dt rating required for the snubber devices.

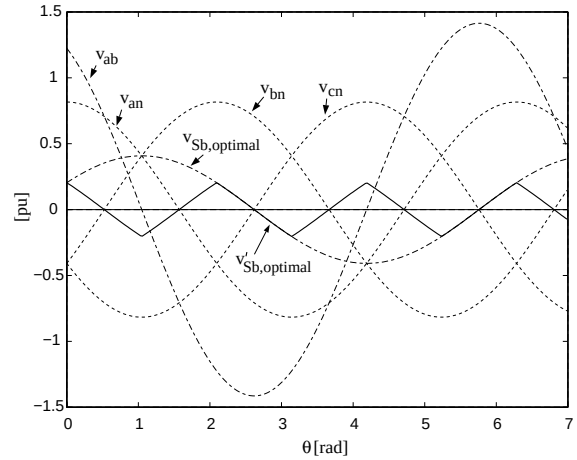


Fig. 8. Optimal snubber driving voltage

B. Neutral Voltage Driven (NVD) realization

The conditions set for the operation of the *AVD* realization discussed above imply $v_{Sb} = v_{Sb,optimal}$. The minimum dwell time condition is met for $v_{Sb} = v'_{Sb,optimal}$ as shown in fig. 8, where v_{Sb} is seem to be a low amplitude zero sequence component. Notice that $v_{Sb} < 0$ when active commutation takes place between devices in the positive group and $v_{Sb}(t) > 0$ when it happens between devices in the negative group. Moreover, the amplitude of $v_{Sb}(t)$ is significantly lower than the line to line peak voltages:

$$|v_{Sb}(t)| \leq \frac{V_{LL,peak}}{4\sqrt{3}} \tag{10}$$

From the conditions above, one can conclude that *near optimal commutation conditions* are established if v_{Sb} is set equal to the neutral potential of the ac voltages, or $v_{Sb} = 0$ (for balanced voltages). This approximation leads to a significant simplification of the topology in fig. 5: only one snubber device and inductor are required for each of the main devices groups. Also, since the tap on the ac voltages is no longer required, the total size and parts count of the ac filter capacitor is significantly reduced and voltage balancing is no longer an issue. An artificial neutral can be created from a Y-connection of a balanced set of ac capacitors, as shown in fig. 9. If an input transformer is employed, the neutral point of the secondary side can also be used, if available. It is also possible to eliminate one of the snubber inductors, following the same reasoning for the *AVD* realization, but there is a penalty: higher voltage rating for the snubber devices (up by a factor of $\sqrt{3}$).

Besides the advantages in terms of cost and size reduction, the CSC topologies in figs. 5 and 9 are quite similar from the perspective of PWM compatibility, requiring basically the same switching patterns. For instance, the switching sequences in (7) can also be used here for the situations illustrated in fig. 9. However, since the snubber driving voltage v_{Sb} is not always equal to the average of the voltage amplitude of the phases undergoing commutation, the voltage stress on the main devices increases.

The extra voltage stress on the main devices associated

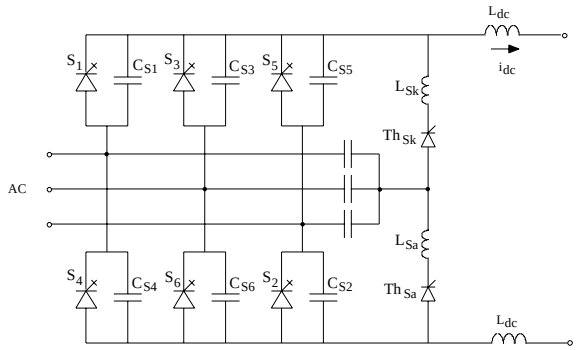


Fig. 9. Neutral Voltage Driven (NVD) realization.

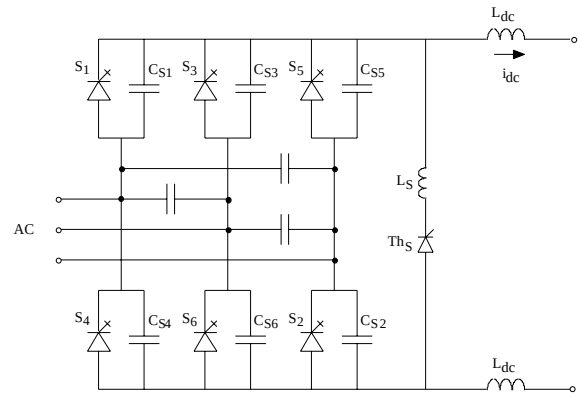


Fig. 10. Line Voltage Driven (LVD) realization.

with the NVD realization can be estimated from the expression of the voltage across the snubber capacitors during the resonant mode in the active commutation sequence. Assuming $v_{Sb} = v_{L_S}(t_1) + v_{fn,out}(t_1) \equiv 0$ and $i_{L_S}(t_1) \approx i_{dc}$ in (2), an estimate of the peak voltage stress across the outgoing device can be obtained as:

$$\begin{aligned} v_{stress,peak} &\approx (cos\omega(t-t_1)-1)\, v_{L_S}(t_1) \\ &\approx 2\, v_{fn,peak} = 1.63\, pu \end{aligned} \tag{11}$$

where $v_{fn,peak}$ is the peak phase voltage. Notice that (11) indicates an extra voltage stress of about 15.5%, compared to the standard voltage stress of $\sqrt{2}$ pu. It is important to point out that this is a theoretical value. Somewhat larger peak voltage stresses should be expected considering the reverse recovery characteristic of the power devices in the main switches and overcompensation of the snubber losses. Although undesirable, this extra voltage stress is not severe and it is largely compensated by the significant reduction in the total parts count required for the implementation of the resonant snubber. It can also be shown that this extra voltage stress is reduced in the presence of third harmonic distortion in the input voltages (p.e., in the variation employing an input transformer with neutral connection).

C. Line Voltage Driven (LVD) realization

Further simplification can be obtained by removing the neutral point connection to the snubber inductor/device branch in fig. 9. After elimination of the redundancies, the *Line Voltage driven* (*LVD*) realization depicted in fig. 10 is obtained. At the time of its first appearance in the literature [14], the optimal conditions for the active commutation process were not recognized and voltage stresses on the main devices in excess of two times the line to line peak voltage were present. A zero voltage stress control strategy was later on introduced [15], [16], employing the commutation and modulation principles discussed in this paper. A comparison between the generalized topology in fig. 3 with the *LVD* topology in fig. 10 reveals some particular aspects of this topology. The snubber driving voltage, v_{Sb} , associated with active commutations in the positive device group is defined from the state of the negative device group and vice-versa. This fact means that v_{Sb} is restricted to the amplitudes of the ac line voltages. Another important characteristic is that if optimal (or near optimal) commutation conditions are desired, the conducting devices in both positive and negative groups are turned off under zero current conditions at the end of *Mode 2* of the active commutation process. As a consequence, the resonant mode involves all the snubber capacitors in the process of circulating the energy trapped in the snubber components. The equivalent capacitance seen from the dc bus in this case is given by $C_{eq} = (3/2)\, C_s$. These singularities of the *LVD* realization lead to slightly modified equations describing the snubber state during *Mode 3*:

$$\begin{aligned} v_{C_S}(t-t_1) &= \frac{1}{2}\left[Z_o\left[i_{dc} - i_{L_S}(t_1)\right] sin\omega_o(t-t_1) - \right. \\ &\quad + v_{L_S}(t_1)\, cos\omega_o(t-t_1) + \\ &\quad \left. - v_{L_S}(t_1)\right] + v_{C_S}(t_1) \end{aligned} \tag{12}$$

$$\begin{aligned} iL_S(t-t_1) &= \frac{1}{Z_o}\, v_{L_S}(t_1)\, sin\omega_o(t-t_1) - \\ &\quad - \left[i_{dc} - i_{L_S}(t_1)\right] cos\omega_o(t-t_1) + \\ &\quad + i_{dc} \end{aligned} \tag{13}$$

where: $\omega_o, = l/\sqrt{L_s\, C_{eq}}$, $Z_o = \sqrt{L_s/C_{eq}}$, $C_{eq} = (3/2)C_s$ and v_{C_S} is the voltage across a snubber capacitor.

From (12), a sufficient condition for zero voltage switching of the incoming devices can be derived:

$$v_{Sb} \geq v_{fn_in} \tag{14}$$

Eq. (14) establishes that zero or minimum extra voltage stress is applied to the main devices in the *LVD* realization if v_{S_b} is equal to the line voltage associated with the incoming device (the snubber branch is in "parallel" with the incoming device). For instance, the active commutation process from S_5 to S_1 with $v_{an} > v_{bn} > v_{cn}$, and $|v_{an}| < |v_{cn}|$ require S_4 to be turned on. With S_4 conducting, the optimal commutation condition is obtained for the commutation from S_5 to S_1 as well as from S_4 to S_2. Notice that under this ac voltage condition and from the discontinuous PWM scheme for CSCs, it is assumed that S_2 is

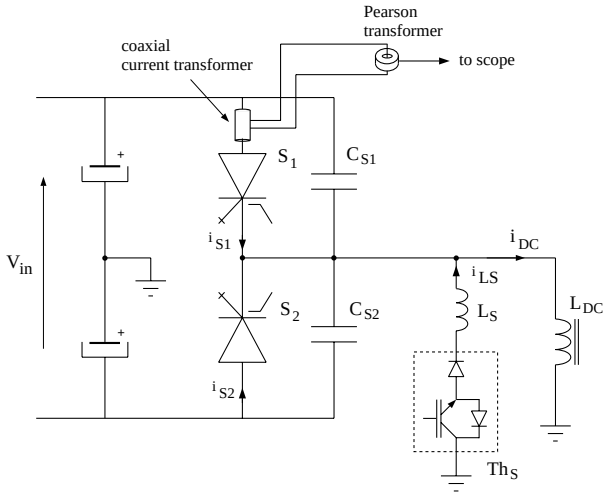


Fig. 11. High power (pulsed) test setup employing MTOs.

on during the entire switching interval. Hence the commutation sequence $S_2 \rightarrow S_4 \rightarrow S_2$ is introduced as part of the active commutation process in the example above, where all these extra transitions can be shown to occur under soft switching conditions. Also, the current vector $\vec{i}_1$ associated with the converter state (S_1, S_2) is exactly in opposition to the vector $\vec{i}_4$ associated with the converter state (S_5, S_4), meaning that the effects of the latter one on the modulation process can be compensated in a quite simple manner. The same modulation scheme and switching pattern discussed for the previous topologies can also be applied in this case, with the addition of the extra commutations required by the active commutation process.

IV. Experimental Results

A. Resonant Snubber Test Setup

The high power (pulsed) test setup implemented for the evaluation of the resonant snubbers in CSC topologies is depicted in fig. 11, with MTO devices employed in the main switches (S_1 and S_2). A series connected IGBT and fast recovery diode set is employed as the snubber switch (Th_S).

The test circuit in fig. 11 is capable of reproducing both passive and active commutation sequences with minimum hardware and control complexity. In this circuit, the snubber driving voltage is set for *optimal* commutation conditions [10] with the snubber driving voltage derived from the center tap of the input supply V_{in}. *Near optimal* commutation conditions [11] can be set by introducing an independent supply to set the snubber driving voltage or by splitting the input voltage in multiple levels.

A cascade connection of two current transformers has been used to minimize the total insertion impedance associated with the measurement of the current through the devices. A co-axial current transformer was inserted directly in the power setup. The secondary winding consists of 10 turns of copper tape wound around the toroidal wound tape core. The primary side of the transformer was built by machining a toroidal shape with the proper dimensions to accommodate the transformer core and secondary winding

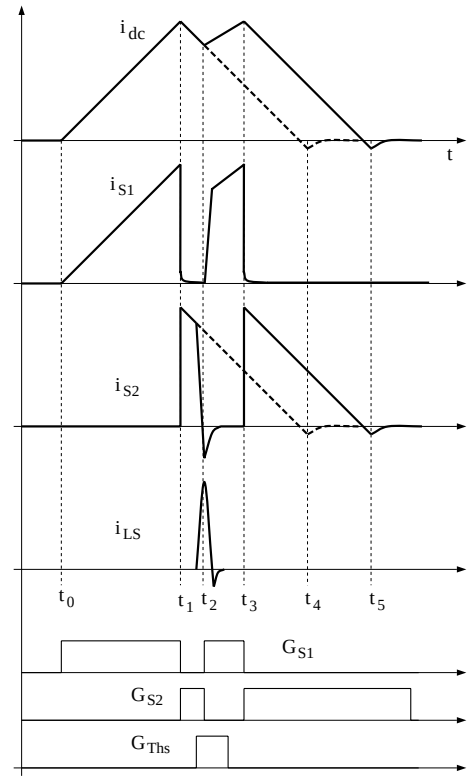


Fig. 12. High power (pulsed) test setup main waveforms.

in a copper bar. This arrangement allows the measurement of the current through the power device only and does not include the snubber capacitor current. The current through the shorted secondary winding of the co-axial transformer is then measured using a commercial current transformer. The total gain of the cascade connection is 0.01 V/A (1 MΩ input impedance).

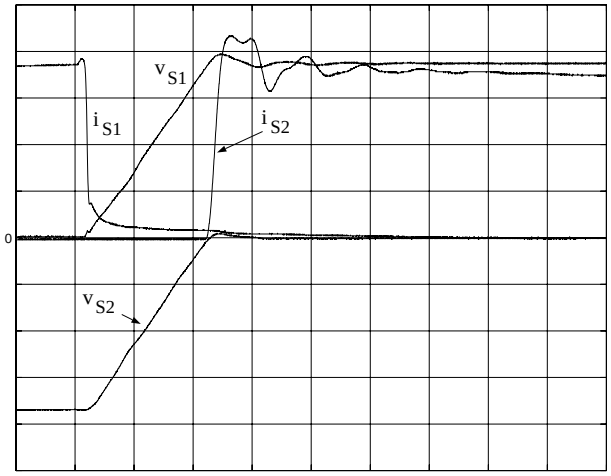
The operation of the test setup is illustrated by the idealized waveforms depicted in fig. 12. Passive commutation processes take place at instants t_1 and t_3. Active commutation process is observed at instant t_2. Fig. 12 also shows the commands for all the switches in the circuit.

The commutation cell described here was tested for several values of dc bus current, input voltage and snubber capacitor values in order to identify trade-offs in CSC operation involving these quantities. The following paragraphs present the procedures and summarize the results obtained in this investigation.

B. Passive Commutation

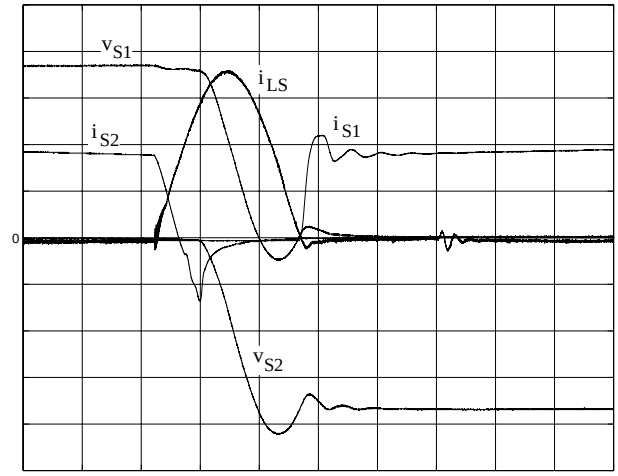
Typical passive commutation waveforms illustrating the entire switching transient are shown in fig. 13, where commutation takes place from switch S_1 to switch S_2. These plots were obtained with $i_{dc} = 150$ A, $V_{in} = 750$ V and $C_S = 1.0$ μF. While the turn-off process is similar to that observed in VSC topologies, the turn-on process implies reverse bias on the incoming switch and it is proper of CSC and MC topologies employing self-commutated devices.

It has been pointed out in the literature that the lack of a series inductor to limit the $\mathrm{d}i_A/\mathrm{dt}$ during the pas-



Voltage scale: 200 V/div.
Current scale: 40 A/div.
Time base: 5μs/div.

Fig. 13. Passive commutation sequence.



Voltage scale: 200 V/div.
Current scale: 75 /div.
Time base: 10 μs/div.

Fig. 14. Active commutation sequence: pseudo-active boost mode.

sive commutation sequence would limit the applicability of this snubber structure in converter circuits based on thyristor-type devices [8]. However, di_A/dt measurements performed in the test setup in do not support the position above. In fact, the tests confirm the self limited di_A/dt characteristic of the MTO and, by extension, of GTO devices at turn-on, as pointed out by Wood [17]($di_A/dt = 168\,A/\mu s \mid i_A = 150\,A$ and $di_A/dt = 188\,A/\mu s \mid i_A = 200\,A$, both with $v_in = 750\,V; C_s = 1\,\mu F$). The conclusion in this matter is that the lack of a series inductor does not constrain the application of the resonant snubbers with MTOs and possibly other thyristor-type devices with highly interdigitated gate-cathode structure. Low dI/dt rates result from the ZVS conditions implying a reduction of the α of the transistors in the MTO structure (wide neutral region in the *N-base* at low voltages), resulting in a less intense regenerative action and slower turn-on process.

C. Active Commutation

The active commutation sequence preserves the turn-on characteristics observed in the analysis of the passive commutation sequence. The main difference between the turn-on processes in these two commutation sequences is the magnitude of the reverse voltage across the incoming switch, significantly lower in the active commutation case. The turn-off process, on the other hand, is unique due to its zero current switching nature and the effects of the charge stored in the outgoing switch over the commutation process.

The active commutation sequence starts as the snubber switch is turned on. Fig. 14 shows typical active commutation waveforms with the outgoing switch being turned-off under ZCS conditions. The switching conditions are such that $i_A \approx 150$ A, v_{AK}=750 V, $C_S = 1.0\,\mu F$.

The peak reverse recovery current I_{rr} and charge Q_{rr} under the conditions in fig. 14 are given by $-102\,A$ and $356\,\mu C$ ($di_A/dt = -36\,A/\mu s$). Large reverse recovery charge is observed in large devices such as the MTOs employed in this test setup. The reverse recovery charge of the outgoing switch is used to boost i_{L_S} to the magnitude required to compensated for losses during the resonant mode and guarantee ZVS conditions for the incoming switch (snubber energy boost). The portion of the reverse recovery current with positive derivative is associated with the turn-off losses in the outgoing switch, contributing to increase the losses during the resonant mode in the active commutation sequence.

V. Conclusions

The paper addresses modeling, control and modulation issues that arise from the utilization of resonant snubbers in current stiff converters. Theoretical analysis is supported by results from a prototype commutation cell capable of reproducing all the commutation modes present in CSC toplogies with resonant snubbers. These analysis and test results are also extensive to the matrix converters case.

The commutation processes of CSCs with resonant snubbers were reviewed. The passive commutation process is always guaranteed and only requires a minimum amplitude of the dc bus current to guarantee bounded commutation intervals. The active commutation process, on the other hand is more involved. A generalized representation of CSC and MC topologies with resonant snubbers was introduced, leading to the derivation of necessary, sufficient and optimal conditions for the occurrence of the active commutation.

Three realizations were presented and analyzed for CSCs. The *AVD* realization offers flexibility and minimum stress on the main devices at the expense of a relatively large number of extra components. The *NVD* realization provides independent commutation of the common-anode and common-cathode devices groups. The *LVD* realization requires only one snubber device implying active use of the main converter devices to assist the active commutation process. The ripple in the input currents and total number of switchings of the main devices per switching period in-

creases in this topology. It is important to observe that all these realizations achieve the benefits sought in the introductory section, offering significant advantages over classical RCD snubbers. These realizations can be promptly applied to the matrix converter case.

The MTO (MOS Turn-Off) thyristor was selected for this study primarily because of its reverse voltage blocking capability and improved gate turn-off characteristics. These characteristics suggest this device as a superior choice for both CSC and MC topologies than classical GTO devices. An important observation regarding the passive commutation turn-on process is the self-limited di/dt exhibited by the MTO, a characteristic pointed out in the literature for regular GTOs. In addition to intrinsic switching characteristics, the ZVS conditions also contribute to slow down the turn-on process, reducing the current transfer ratio α of the transistors in the device structure ($di_A/dt < 200\,\mathrm{A}/\mu\mathrm{s}$ for dc bus currents up to 200 A).

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