A Scalable Compact Model for Depletion MOSFETs in Smart Power Applications Allowing Efficient Parameter Determination

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Abstract–This paper presents a scalable quasi-static depletion MOSFET model applicable in circuit design. Both subthreshold and on-state behaviour are reproduced for low and high voltage devices. During transient simulations a dynamic model with current dependent channel charge partition provides the source and drain displacement currents. To ensure practical application a parameter extraction scheme is given. Finally, the comparison between measured and simulated characteristics for various devices proves a good model accuracy.

I. Introduction

In the beginning of circuit integration depletion MOSFETs (DMOSFETs) were widely used as load elements in inverters.

Although CMOS technology replaced NMOS solutions in many applications there are still designs preferring such traditional topologies. This is mainly due to a high cost pressure on products, the power consumption of which plays a rather non-critical role. Smart power circuits for the automobile industry are typical examples for such integrated devices.

In the past a few models of DMOSFETs have been published. Unfortunately, they do not cover all operation modes [1], [2] and sometimes suggest an implicit equation system [4], which very often causes problems in numerical simulations. Until today, no hint for a complete parameter extraction routine can be found in literature.

For instance, [1] derives a model for the on-state, but does not analyse subthreshold mode. Furthermore, the dynamic behaviour follows from a capacitance network. In contrast to this, [4] suggests an implicit equation system, which is valid in subthreshold region, too. The charge model only considers the channel, bulk and gate charge. Finally, [2] presents an approximate closed-form solution for the substhreshold current, which neglects inversion completely.

In the following a circuit model working in all operation modes is discussed. Its simple parameter determination procedure assures practical usage.

II. Depletion MOSFET

Depletion MOSFETs of n-type are n-channel enhancement MOSFETs with an additional n-implantation as drawn in Fig. 1. To avoid oxide breakdown, high voltage devices show zones of increased insulator thickness near the drain and source terminal. In good approximation there is no gate influence on these resistances. Low voltage devices do not need such regions, hence the gate overlaps both the darin and source n^+-area at the same oxide thickness as in the middle of the device.

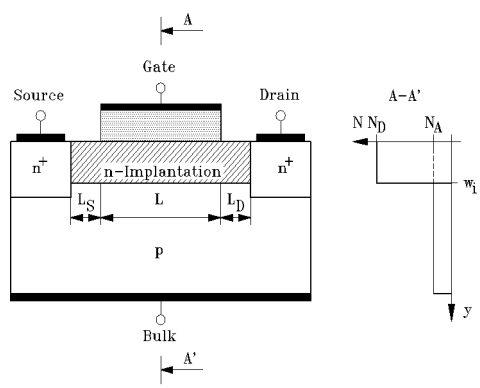

Fig. 1. Structure of a depletion MOSFET with source and drain resistance.

As known from the enhancement MOSFET there are three possible states at the semiconductor surface: accumulation, depletion and inversion. These local modes combine to six different operating conditions in the inner depletion MOSFET (Fig. 2-7). For a sweep of the gate-source voltage V_{GS} at fixed drain-source and source-bulk voltage (V_{DS}, V_{SB}) the device goes through all states in the given sequence (Fig. 4 excepted).

If there is no accumulation at the drain (Fig. 2) saturation may occur for high drain-source voltages at the drain end of the channel. Fig. 8 illustrates this assuming a combination of accumulation and depletion under the gate oxide.

The appearance of local modes can be seen as the main difference to enhancement MOSFETs, where there is only inversion in on-state possibly turning into saturation.

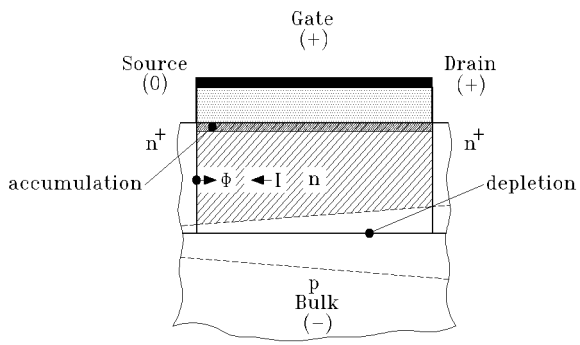

Fig. 2. Accumulation at the semiconductor surface.

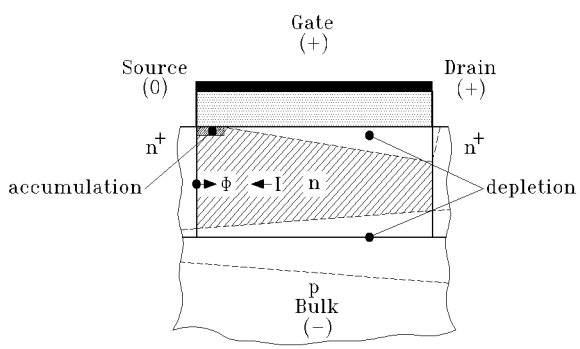

Fig. 3. Accumulation and depletion at the semiconductor surface.

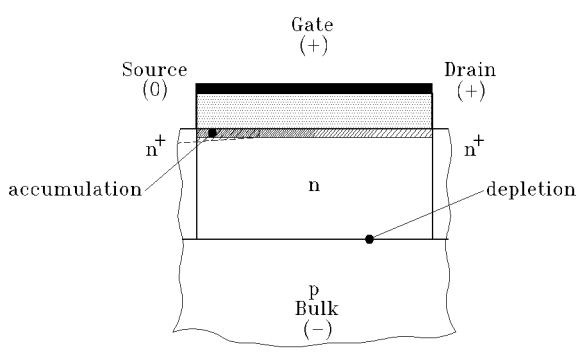

Fig. 4. Accumulation at the semiconductor surface and punch-through of body space-charge region.

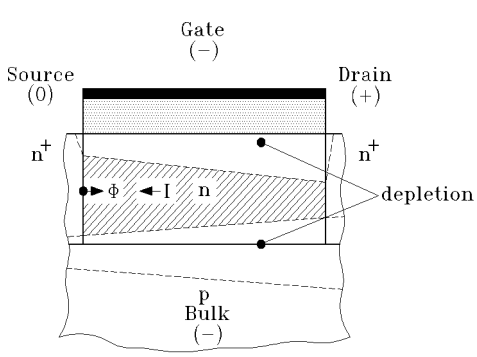

Fig. 5. Depletion at the semiconductor surface.

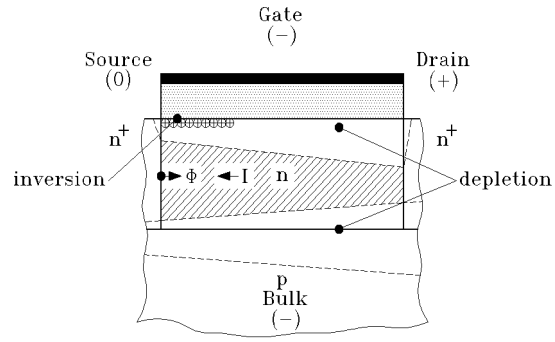

Fig. 6. Inversion and depletion at the semiconductor surface.

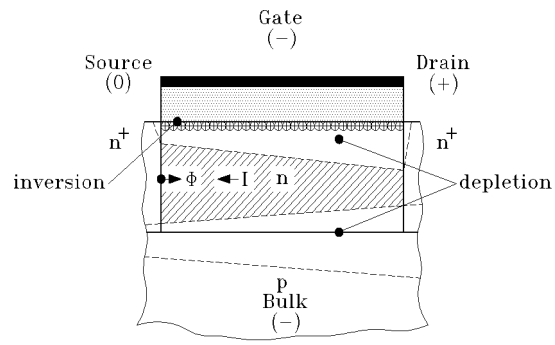

Fig. 7. Inversion at the semiconductor surface.

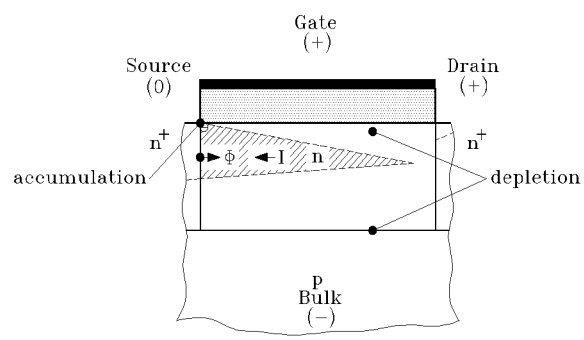

Fig. 8. Saturation for accumulation and depletion at the semiconductor surface.

Concerning the source and drain resistance depletion by the bulk space charge region predominates. The drain resistance has an additional saturation region near the terminal, when the depleted zone reaches the semiconductor surface.

Each terminal of the device can get a charge assigned. The gate charge is simply the sum over all charges on the gate metallization, whereas bulk doping ions (N_A^-) form the bulk charge. All electrons in the inner transistor and both resistances can be divided into a source and drain component (Fig. 9).

In subthreshold mode the electrostatic potential in the inner transistor remains approximately constant along the channel, thus the current flows mainly by diffusion of very few electrons.

Based on these considerations a model description will be derived in the next section.

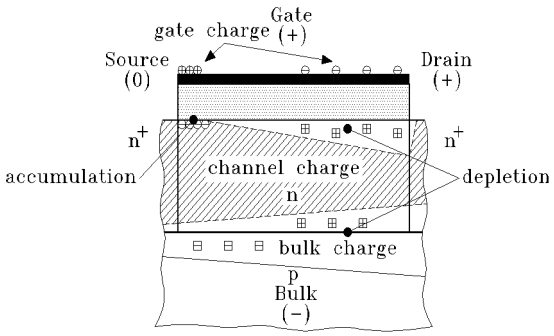

Fig. 9. Charges in a depletion MOSFET.

III. Model Description

The key to a compact circuit model is the introduction of an electrostatic potential Φ (Fig. 2-8) and the definition of individual charges per area for each possible state at the semiconductor surface:

- accumulation (Q'_{na})
- accumulation punch-through (Q'_{nap})
- depletion (Q_{nd})
- inversion (Q_{ni}).

This leads to a single equation for the drain-source current I_{DS} in on-state due to drift

$$\begin{aligned} I_{DS} &= \frac{w\mu_{ns}}{L}\left(\int_{acc.} Q'_{na}\,\mathrm{d}\Phi + \int_{acc.\,pt.} Q'_{nap}\,\mathrm{d}\Phi\right) \\ &\quad + \frac{w\mu_n}{L}\left(\int_{dep.} Q'_{nd}\,\mathrm{d}\Phi + \int_{inv.} Q'_{ni}\,\mathrm{d}\Phi\right), \quad (1) \end{aligned}$$

where w and L is the width and length of the inner transistor, respectively. With μ_n and μ_{ns} the different mobilities in the channel and at the semiconductor surface are taken into account. Both borders of each section, i.e. the limits of each integral, can be calculated in terms of Φ. A set of switching conditions assigns the proper values at each operating point. The intention is, that only those integrals applicable to a particular terminal voltage are evaluated, whereas the other terms of (1) vanish.

Source and drain resistance are only subject to partial depletion by the bulk space charge region. Hence, their current-voltage relation is

$$\begin{aligned} I_{DS} &= \frac{w\mu_n}{L_{S,D}}\int_{R_S,R_D} Q'_{nRS,D}\,\mathrm{d}\Phi \\ &= \frac{w\mu_n}{L_{S,D}}\Big(qN_D w_i\left(\Phi_{eS,D}-\Phi_{bS,D}\right) \\ &\quad - \frac{2}{3}\sqrt{\frac{2q\varepsilon_0\varepsilon_{Si}N_A N_D}{N_A+N_D}} \\ &\quad \times\Big(\left(V^*_{SB}+V_D+\Phi_{eS,D}\right)^{\frac{3}{2}} \\ &\quad - \left(V^*_{SB}+V_D+\Phi_{bS,D}\right)^{\frac{3}{2}}\Big)\Big), \quad (2) \end{aligned}$$

using $\Phi_{bS,D}$ as the potential Φ at the beginning and $\Phi_{eS,D}$ as the value of Φ at the end of the particular resistance. L_S and L_D is the length of the source and drain resistance, respectively (Fig. 1). Saturation in the drain resistance occurs for:

$$\begin{aligned} \Phi &= \Phi_{sat} \\ &= \frac{qw_i^2 N_D\left(N_A+N_D\right)}{2\varepsilon_0\varepsilon_{Si}N_A} - V^*_{SB} - V_D - V^*_{DS}. \quad (3) \end{aligned}$$

V^*_{SB} and V^*_{DS} denote terminal voltages of the inner transistor.

Charge calculation in on-state requires an integration over the length of each particular local mode. With the known current I_{DS} the length dependence can be transformed into a potential (Φ) dependence. For the channel and bulk charge results:

$$Q_n = -\frac{w^2\mu_n}{I_{DS}}\int_0^{V_{DS}} Q'_n\,Q'^*_n\,\mathrm{d}\Phi, \quad (4)$$

$$Q_B = -\frac{w^2\mu_n}{I_{DS}}\int_0^{V_{DS}} Q'_B\,Q'^*_n\,\mathrm{d}\Phi. \quad (5)$$

Note that Q'^*_n was used instead of Q'_n to distinguish between μ_n and μ_{ns}. From a modification of [3] the source charge follows as (see also Fig. 1):

$$\begin{aligned} Q_S &= -\frac{w^3\mu_n^2}{I_{DS}^2\left(L_S+L+L_D\right)} \\ &\quad \times\int_0^{V_{DS}} Q'^*_n\int_0^{\Phi} Q'_n\,Q'^*_n\,\mathrm{d}\Phi^*\,\mathrm{d}\Phi. \quad (6) \end{aligned}$$

When defining Q_{niT} and Q_{SiT} as the channel and source charge of the inner transistor and $Q'_{nS,D}$ as the channel charge per area in the resistances (6) changes to:

$$\begin{aligned} Q_S &= -\frac{w^3\mu_n^2}{I_{DS}^2\left(L_S+L+L_D\right)} \\ &\quad \times\Bigg(\int_{\Phi_{bS}}^{\Phi_{eS}} Q'_{nS}\int_{\Phi_{bS}}^{\Phi} Q'^2_{nS}\,\mathrm{d}\Phi^*\mathrm{d}\Phi \\ &\quad + \int_{V^*_{DS}}^{V^*_{DS}+\Phi_{eD}} Q'_{nD}\int_{V^*_{DS}}^{\Phi} Q'^2_{nD}\,\mathrm{d}\Phi^*\mathrm{d}\Phi\Bigg) \\ &\quad + \frac{L+L_D}{L_S+L+L_D}Q_{nS} + \frac{L}{L_S+L+L_D}Q_{SiT} \\ &\quad + \frac{L_D}{L_S+L+L_D}Q_{niT}. \quad (7) \end{aligned}$$

All charges sum up to zero:

$$0 = Q_G + Q_B + Q_n - Q_i \quad (8)$$

with

$$Q_i = -qww_iLN_D. \quad (9)$$

Approximating all square roots by a terminated Taylor series drastically simplifies the equations for the charge model with only a slight loss of accuracy.

In subthreshold operation the channel is cut off over its whole length. The remaining electrons transport the current by diffusion. Boltzmann's statistics predict an exponential behaviour of I_{DS} for constant $\Phi = \Phi_s$ but varying electrochemical potential:

$$I_{DS} = \frac{w}{L} I_s \exp\left(\frac{\Phi_s}{V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}^*}{V_T}\right)\right). \quad (10)$$

In contrast to [2] we need only one additional parameter instead of three. Since diffusion predominates grad(n) is constant, which makes the charge calculation for the inner transistor easier:

$$Q_{niT} = Q_s \exp\left(\frac{\Phi_s}{V_T}\right)\left(1 + \exp\left(-\frac{V_{DS}^*}{V_T}\right)\right), \quad (11)$$

$$Q_s = -\frac{1}{2}\frac{wL}{\mu_n V_T} I_s,$$

$$Q_{BiT} \approx Q_{Bs}\sqrt{\Phi_s + V_D + V_{SB}^*}, \quad (12)$$

$$Q_{Bs} = -wL\sqrt{\frac{2q\varepsilon_0\varepsilon_{Si}N_A N_D}{N_A + N_D}},$$

$$Q_{SiT} = \frac{Q_s}{3}\exp\left(\frac{\Phi_s}{V_T}\right)\left(2 + \exp\left(-\frac{V_{DS}^*}{V_T}\right)\right). \quad (13)$$

Beside the basic current and charge description our model includes:

- channel length modulation [5]
- avalanche breakdown
- parasitic diodes (source/drain-bulk junction)
- temperature dependence of all currents and charges.

IV. Paramter Determination

The 25 paramters can be determined automatically using the commercial programs *IC-CAP* (extraction) and *SABER* (simulation). But not all parameters need to be known for each device. As an example, the parasitic diodes of the source and drain region exhibit a small influence on the terminal characteristics of a long channel DMOSFET only.

The extraction procedure consists of 14 steps, which are summarized in the following.

- *1) Determination of oxide thickness.* ($C - V$ - measurement to obtain C_{GG} for a wide/long transistor.)
- *2) Determination of geometry reduction.* (Plot/extrapolation of $g_m = f(width)$ and $1/g_m = f(length)$ to obtain the width for $g_m = 0$ and the length for $1/g_m = 0$.)
- *3) Determination of doping parameters.* (Optimization of transfer characteristic for a wide/long transistor, V_{DS}: small, I_D: between subthreshold and on region, V_{SB}: 5 or 6 different values.)
- *4) Determination of subthreshold transport current.* (Optimization of transfer characteristic in subthreshold region.)
- *5) Determination of mobility parameters.* (Optimization of transfer characteristic of a wide/long transistor in on-state and not too high V_{GS}.)
- *6) Check length reduction.* (Simulation of transfer charcteristic for a wide/short transistor.)
- *7) Check width reduction.* (Simulation of transfer characteristic for a narrow/long transistor.)
- *8) Determination of the possible parasitic drain resistance.* (Optimization of transfer characteristic for a short/wide transistor and large values of V_{GS}.)
- *9) Determination of channel length modulation.* (Optimization of output characteristic in saturation for a short/wide transistor.)
- *10) Determination of the temperature exponent for mobility and subthreshold current.* (Optimization of transfer characteristic for several temperatures and a wide/long transistor.)
- *11) Check parameters.* (Simulation of a narrow/short transistor.)
- *12) Determination of DC parameters for the diodes.* (Measurement of diode $I - V$ - characteristic to obtain *SPICE* parameters.)
- *13) Determination of junction capacitances for the diodes.* ($C - V$ - measurement to obtain *SPICE* parameters.)
- *14) Determination of drain/source resistance region lengths.* (Optimization of transfer characteristic for a wide/short transistor.)

V. Results

The model was implemented in a *SABER* simulator. For verification at first simulated output and transfer characteristic of a device with source and drain resistance are compared with measurements (Fig. 10, 11). Both figures proof a good model quality. Deviations are mainly due to the assumption of an abrupt junction between channel and bulk (as in [1], [4]).

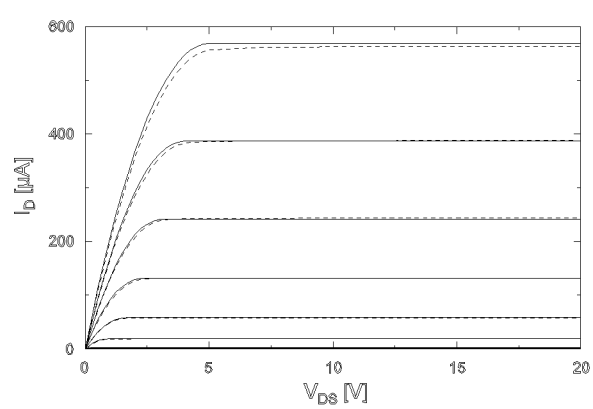

Fig. 10. Output characteristic of a DMOSFET *with* source and drain resistance (- - measured, — simulated; $V_{GS} = (-3 \ldots 5)$V, $V_{SB} = 0$V).

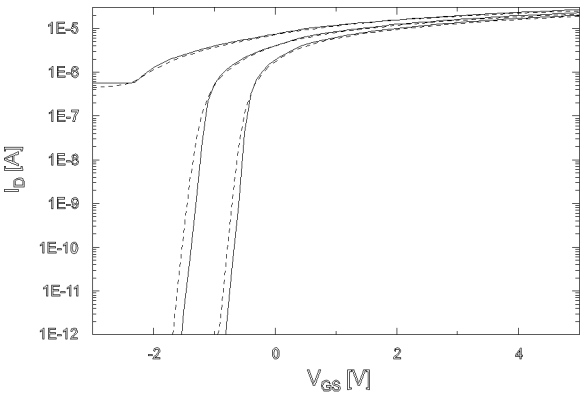

Fig. 11. Transfer characteristic of a DMOSFET *with* source and drain resistance (- - measured, — simulated; $V_{DS} = 0.1$V, $V_{SB} = (0 \ldots 5)$V).

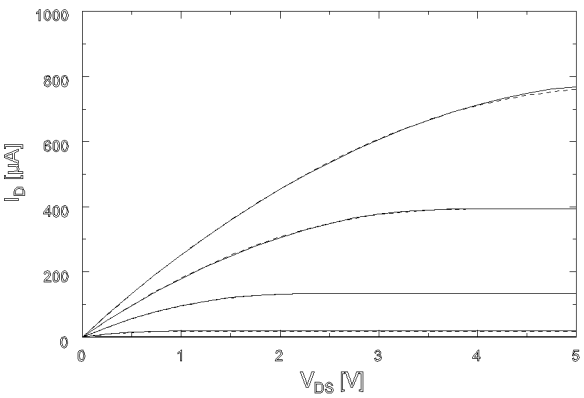

Fig. 12. Output characteristic of a DMOSFET *without* source and drain resistance (- - measured, — simulated; $\frac{w}{L} = \frac{w_0}{L_0} = 1$; $V_{GS} = (-3 \ldots 5)$V, $V_{SB} = 0$V).

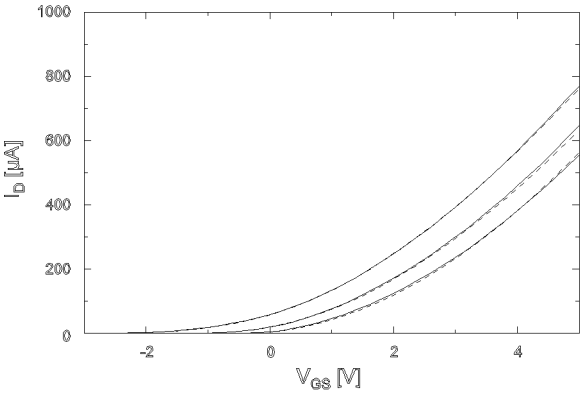

Fig. 13. Transfer characteristic of a DMOSFET *without* source and drain resistance (- - measured, — simulated; $\frac{w}{L} = \frac{w_0}{L_0} = 1$; $V_{SB} = (0 \ldots 5)$V, $V_{DS} = 5$V).

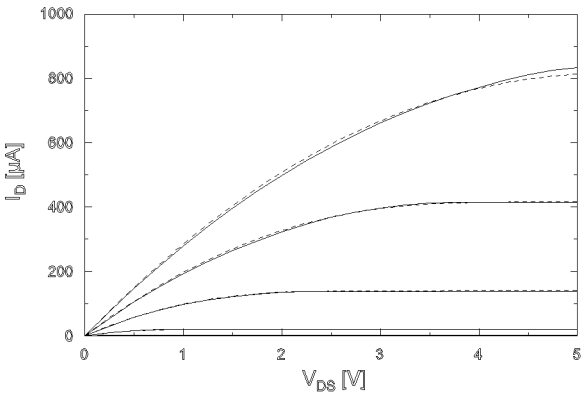

Fig. 14. Output characteristic of a DMOSFET *without* source and drain resistance (- - measured, — simulated; $\frac{w}{L} = \frac{0.15w_0}{0.15L_0}$; $V_{GS} = (-3 \ldots 5)$V, $V_{SB} = 0$V)

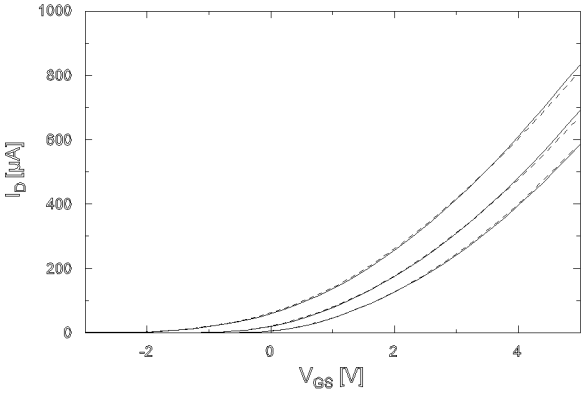

Fig. 15. Transfer characteristic of a DMOSFET *without* source and drain resistance (- - measured, — simulated; $\frac{w}{L} = \frac{0.15w_0}{0.15L_0}$; $V_{SB} = (0 \ldots 5)$V, $V_{DS} = 5$V).

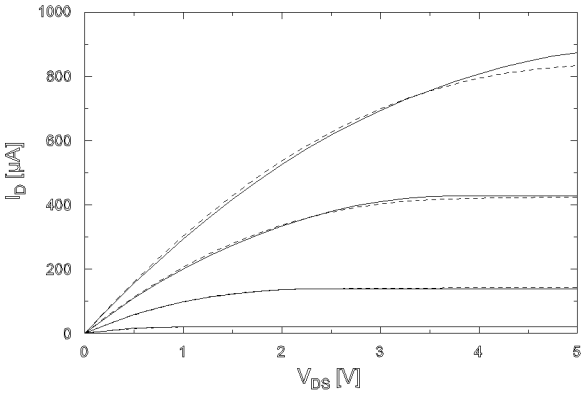

Fig. 16. Output characteristic of a DMOSFET *without* source and drain resistance (- - measured, — simulated; $\frac{w}{L} = \frac{w_0}{L_0} = \frac{0.1w_0}{0.1L_0}$; $V_{GS} = (-3 \ldots 5)$V, $V_{SB} = 0$V).

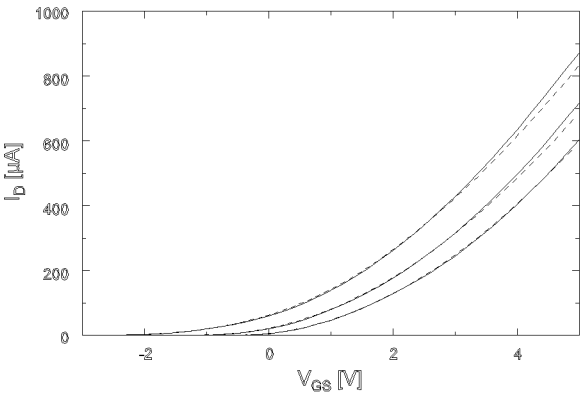

Fig. 17. Transfer characteristic of a DMOSFET *without* source and drain resistance (- - measured, — simulated; $\frac{w_0}{L_0} = \frac{0.1 w_0}{0.1 L_0}$; $V_{SB} = (0 \ldots 5)$V, $V_{DS} = 5$V).

A next step is the prove of scalabilty. The six figures above (Fig. 12-Fig. 17) show again the comparison of measured and simulated output and transfer characteristics. In contrast to the prevoius there are no additional resistances and the geometry varies from $\frac{w}{L} = \frac{w_0}{L_0}$ to $\frac{w}{L} = \frac{0.1 w_0}{0.1 L_0}$. Only small deviations can be observed.

Capacitance measurements provide a suitable benchmark for the charge model. We measured and simulated the gate-gate capacitance G_{GG}, which is defined to be

$$C_{GG} = \left.\frac{\mathrm{d}Q_G}{\mathrm{d}V_{GS}}\right|_{V_{SB}, V_{DB} = \mathrm{const.}} \tag{14}$$

at $V_{SB} = V_{DB} = 0$V for a device without additional resistances. Both curves show some differences caused by the already mentioned doping profile approximation and a sharp transition between various semiconductor surface states. The last simplification is absolutely necessary to obtain integrable electron charges per area in (1) and hence an explicit equation system of the inner device.

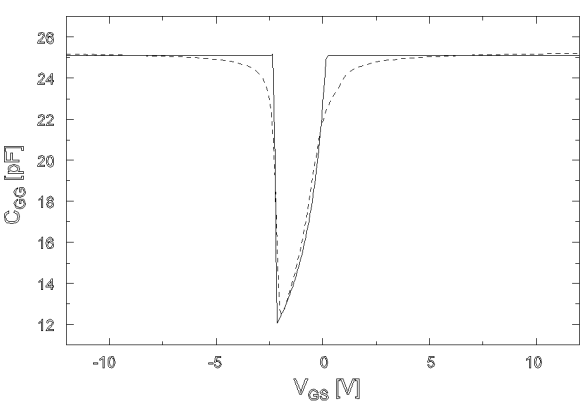

Fig. 18. Gate-gate capacitance of a DMOSFET *without* source and drain resistance (- - measured,— simulated; $V_{SB} = V_{DS} = 0$V).

Finally, Fig. 19 displays the drain current and the ratio between source and channel charge again for a device without source and drain resistance. It can be seen, that source and drain charge are equal at $V_{DS} = 0$, since the surface state and the bulk depletion region width do not change along the channel. With rising V_{DS} there are fewer electrons at the drain than near the source, because the space charge region width increases. Eventually pinch-off occurs and the source and drain charge ratio assumes a value of $Q_S/Q_D \approx 1.5$.

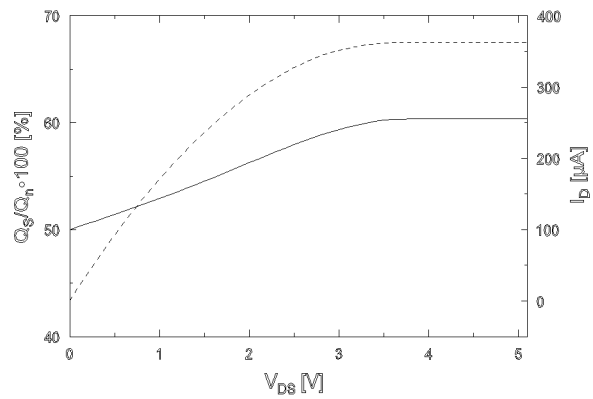

Fig. 19. Drain current (- -) and source charge in per cent of channel charge (—) of a DMOSFET *without* source and drain resistance ($V_{SB} = 0$V, $V_{GS} = 3$V).

VI. Conclusion

A depletion MOSFET model for smart power circuit simulations covering all operation modes was presented. It applys a charge description for all internal states in subthreshold mode and on-state.

Measurements of DC characteristics and the gate-gate capacitanc prove the validity of the description.

All 25 parameters can be determined automatically, which guarantees practical usefulness.

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