A Reversible Unity Power Factor Step-Up/Step-Down AC-DC Converter Controlled by Sliding Mode

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Abstract - The step-up inverter with controlled output current manages DC-to-AC power transfer, with any ratio between the DC and the AC levels. By reversing the energy flow, this circuit becomes a high power factor step-down (or step-up) rectifier. Sliding mode is applied to control the fifth-order system. Simulation results of a 1kW inverter/rectifier are included to confirm the analysis.

I - INTRODUCTION

The differential voltage-source inverter, as presented in [1]-[4], is a fourth-order circuit that generates an AC output voltage whose peak value is independent of the DC input level, using only one power processing stage. It is intended mainly for applications requiring peak output voltage higher than the DC input. As it can be seen in Fig. 1, the inverter consists of two independent step-up (or "boost") converters, each one of them generating a DC-biased sinusoidal voltage. The DC offset is necessary because individual voltages v_{C1} and v_{C2} must be kept higher than V_{in} all the time. Across the load is applied the differential voltage between the two converters. In this way, if a sinusoidal voltage is desired at the output, the DC levels must be identical, while the AC references for v_{C1} and v_{C2} are phase-shifted (by any angle, although 180 degrees provides the best use of the components).

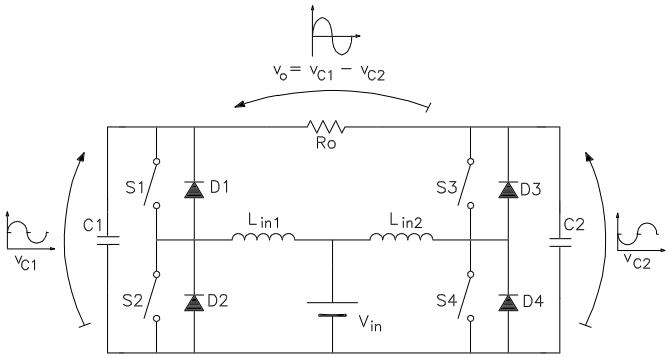


Fig. 1 - Diagram of the differential voltage-source inverter implemented with two step-up converters.

The goal of the present work is to study this topology acting as an inverter with imposed output current, which can be used for AC power (co)generation from photovoltaic cells, for instance. Moreover, by reversing the energy flow, the circuit becomes an AC-DC converter with high power factor input current. The AC current control is made possible by the inclusion of an inductor (L_{ac}) in the original inverter, as shown in Fig. 2, augmenting its total order to five. The current through L_{ac} becomes the variable of major interest, and the difference (v_{C1} - v_{C2}) must adapt itself as required by the shape and magnitude of $i_{L_{ac}}$. Here again, these voltages must never fall below V_{dc}. Due to the possibility of power flow reversion, the sources and inductors are identified as *AC* or *DC*, rather than *input* or *output*. The key advantage of the proposed converter is its ability to manage power transfer from a DC source to an AC one with reversibility, irrespective of the ratio between their voltages.

The system is controlled by sliding mode, or sliding regime [6]-[11]. As it is shown in the next sections, two subsystems are defined. They are analysed separately, governed by independent sliding surfaces, and driven by independent single-input control circuits.

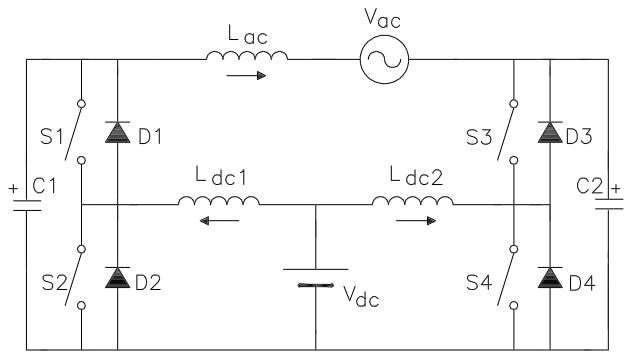


Fig. 2 - Circuit of the inverter after insertion of L_{ac}.

II - ANALYSIS

The complete system can be broken into two parts for control purposes, as shown in Fig. 3: the "right-side" converter, responsible for controlling $i_{L_{ac}}$, and the "left-side" one, responsible for v_{C_2}. These subsystems are coupled, so the output variable of one converter is perceived as a disturbance by the other: $i_{L_{ac}}$, in Fig. 3a, must be imposed through (v_{ac} + v_{C_2}), and similarly the right-side converter must keep v_{C_2} sufficiently close to v_{C_2}*, no matter what the instantaneous value of $i_{L_{ac}}$ is. (Asterisks indicate *reference values*.)

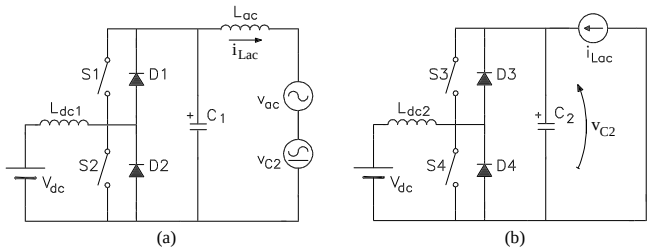


Fig. 3 - a) Left-side subsystem, responsible for imposing i_{Lac};
b) right-side subsystem, responsible for regulating v_{C2}.

A. Right-side converter

Since the right-side converter is a second-order circuit, it is preferable to start the analysis by it. Equation (1) defines the reference for v_{C_2} (ω represents the mains angular frequency).

$$v^*_{C2}(t) = V^*_{C2_{dc}} + V^*_{C2_{ac}} \cdot \sin(\omega t + \pi) \quad . \tag{1}$$

If the voltage v_{ac} is equally divided between capacitors C_1 and C_2, then each converter processes half of the total output power. So, $V^*_{C2ac_p} = \frac{1}{2} \cdot V_{ac_p}$, where p stands for *peak value*, and the following condition must be satisfied in excess:

$$V^*_{C2_{dc}} > V_{dc} + \tfrac{1}{2} \cdot V_{ac_p} \quad . \tag{2}$$

The step-up configuration requires a duty cycle on S_4 according to (3), here referred to as *right converter duty cycle* (d_R). S_3, by its turn, receives complementary pulses.

$$d_R(t) = 1 - \frac{V_{dc}}{v_{C_2}(t)} \approx 1 - \frac{V_{dc}}{V^*_{C_{2dc}} + \frac{1}{2} \cdot V_{ac_p} \cdot \sin(\omega t + \pi)} \quad . \tag{3}$$

Current i_{Ldc2} can be calculated from the instantaneous energy balance:

$$i_{L_{dc_2}}(t) = \left[v_{C_2}(t) / V_{dc} \right] \cdot \left[-i_{L_{ac}}(t) + i_{C_2}(t) \right] \quad . \tag{4}$$

Assuming that, in steady state, all the variables follow their references ($i_{L_{ac}}$* is defined in section II-*B*), one obtains:

$$i_{L_{dc_2}}(t) = \frac{1}{V_{dc}} \left[\frac{1}{4} \cdot V_{ac_p} I^*_{L_{ac_p}} \left(1 - \cos 2\omega t\right) - V^*_{C2_{dc}} I^*_{L_{ac_p}} \sin \omega t - \right.$$

$$\left. -\omega C_2 \left(\frac{1}{2} \cdot V^*_{C2_{dc}} V_{ac_p} \cos \omega t - \frac{1}{8} \cdot V^2_{ac_p} \sin 2\omega t \right) \right] \quad . \tag{5}$$

The above equation describes the low-frequency current through L_{dc2}; there are still high-frequency excursions due to the commutations between S_3 and S_4. One observes that there is a continuous term in this current, responsible for the power transfer, added to alternate components of first and second orders. The presence of such components is inherent to the operation of this circuit. If the current through C_2 is negligible, the term $-\omega C_2 \cdot (\ldots)$ disappears from (5). In general, i_{C_2} and the switching ripple do not greatly increase the efficient value of the current, which can be calculated through (6). Positive peak current occurs when $\omega t = 3\pi/2$, being given by (7) (plus the high-frequency ripple, $\frac{1}{2} \cdot \Delta I_{Ldc2max}$).

$$I_{Ldc_{2ef}} = \left(I^*_{L_{ac_p}} / V_{dc} \right) \cdot \sqrt{\frac{3}{8} \cdot V^{*2}_{C2_{ac_p}} + \frac{1}{2} \cdot V^{*2}_{C2_{dc}}} \quad . \tag{6}$$

$$I_{Ldc_{2_p}} = I^*_{L_{ac_p}} \cdot \left(V^*_{C2_{dc}} + V^*_{C2_{ac_p}} \right) / V_{dc} \quad . \tag{7}$$

In rectifying operation, all the terms involving $i_{L_{ac}}$ (or I_{Lac_p}*) in (4), (5), and (7) are inverted. Duty cycle remains unchanged because the reference for v_{C_2} is the same.

Since the gate pulses to the switches are complementary, the discontinuous conduction on L_{dc2} is avoided, and only two subtopologies or structures are possible. They are shown in Fig. 4. S_3, D_3 and S_4, D_4 are presented as single ideal switches, whose state is described by variable γ (8). $i_{L_{ac}}$ is assumed to be at its reference value.

$$\begin{cases} \gamma = 1 \Rightarrow S_4, D_4 \text{ ON}; \; S_3, D_3 \text{ OFF} \\ \gamma = 0 \Rightarrow S_4, D_4 \text{ OFF}; \; S_3, D_3 \text{ ON} \end{cases} \; ; \; \bar{\gamma} = (1 - \gamma) \quad . \tag{8}$$

The situation $\gamma = 1$ is associated to an increase of energy in the circuit. L_{dc2} and C_2 are completely decoupled. The inductor current rises linearly, while $i_{L_{ac}}$* flows through C_2. Condition $\gamma = 0$ establishes the coupling between the elements L_{dc2} and C_2. One must observe that i_{Ldc1} and $i_{L_{ac}}$* can be either positive or negative, depending upon the angle $\varphi = \omega t$.

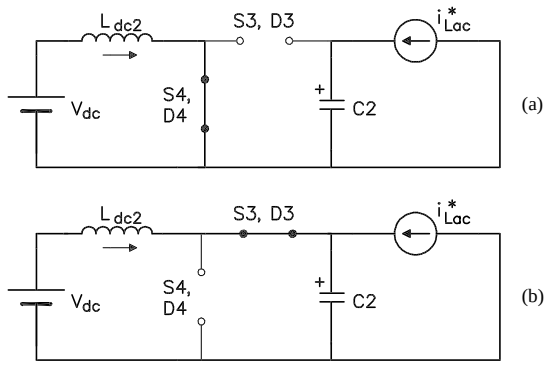


Fig. 4 - The two structures of the right-side converter:
a) S_4, D_4 on; b) S_4, D_4 off.

After defining the error variables ε_{vC2} and ε_{iLdc2} (9), the state error equation (10) can be written. Actually, the low-frequency reference functions, when compared to the switching frequency, can be considered as *quasi-static*, in such a way that the term $\mathrm{d}/\mathrm{d}t\,[v_{C2}^*\,;\, i_{Ldc_2}^*]^{\mathrm{T}}$ is, in general, neglected ("T" means *transposition*).

$$\varepsilon_{v_{C_2}} = v_{C_2} - v^*_{C_2} \quad ; \quad \varepsilon_{i_{Ldc_2}} = i_{L_{dc_2}} - i^*_{L_{dc_2}} \quad . \tag{9}$$

$$\begin{bmatrix} \varepsilon'_{v_{C_2}} \\ \varepsilon'_{i_{Ldc_2}} \end{bmatrix} = \begin{bmatrix} i_{L_{dc_2}} / C_2 \\ -v_{C_2} / L_{dc_2} \end{bmatrix} \cdot \bar{\gamma} + \begin{bmatrix} i^*_{L_{ac}} / C_2 \\ V_{dc} / L_{dc_2} \end{bmatrix} - \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} v^*_{C_2} \\ i^*_{Ldc_2} \end{bmatrix} \quad . \tag{10}$$

B. Left-side converter

The left-side subsystem is, in fact, a step-up converter with a resonant circuit plus a voltage source at the output. Its main objective (and the objective of the system as a whole) is to control $i_{L_{ac}}$. Any necessary adjustment of the voltage across L_{ac} is done on v_{C_1}, even due to small tracking errors from the right-side converter. The reference for $i_{L_{ac}}{}^*$ is declared in (11). For rectifying operation, π rad are added to the argument of the sine function.

$$i^*_{L_{ac}}(t) = I^*_{L_{ac_p}} \cdot \sin \omega t \quad . \tag{11}$$

The DC offset on the right-side capacitor is naturally established also on C_1. If this offset is properly chosen, according to (2), both v_{C_1} and v_{C_2} never fall below V_{dc}, ensuring the operation of the system. Moreover, since L_{ac} is designed to filter the high-frequency switching ripple, its steady-state low-frequency voltage is small, and also the AC component of v_{C_1} oscillates close to ($v_{ac} + v_{C_2}$):

$$v_{C_1}(t) \approx V^*_{C2_{dc}} + \tfrac{1}{2} \cdot V_{ac_p} \cdot \sin \omega t \quad , \tag{12}$$

thus the equations of duty cycle and i_{Ldc1} become similar to (3) and (5), respectively, with π rad added to the arguments of each sine or cosine function, giving (13) and (14). Here again, when the system acts as an AC-DC converter, all the terms with $I_{Lac_p}{}^*$ are inverted.

$$d_L(t) \approx \; 1 \; - \left\{ V_{dc} \Big/ \left[V^*_{C2_{dc}} + \tfrac{1}{2} \cdot V_{ac_p} \cdot \sin(\omega t) \right] \right\} \quad ; \tag{13}$$

$$i_{L_{dc_1}}(t) \approx \frac{1}{V_{dc}} \Big[\tfrac{1}{4} \cdot V_{ac_p} I^*_{L_{ac_p}} \left(1 - \cos 2\omega t\right) + V^*_{C2_{dc}} I^*_{L_{ac_p}} \sin \omega t +$$

$$+ \omega C_1 \left(\tfrac{1}{2} \cdot V^*_{C2_{dc}} V_{ac_p} \cos \omega t + \tfrac{1}{8} \cdot V^2_{ac_p} \sin 2\omega t \right) \Big] \quad . \tag{14}$$

The two possible subtopologies for the left-side converter are shown in Fig. 5; it is assumed that v_{C_2} follows exactly its reference. The state of the switches, γ, is defined in (15).

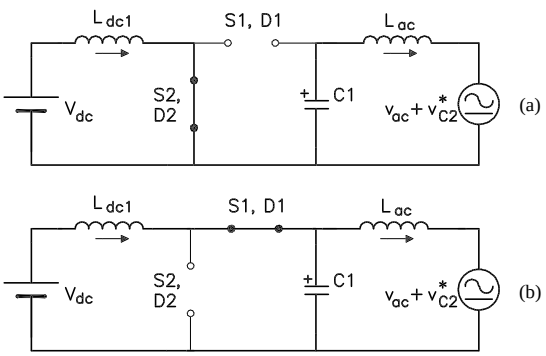


Fig. 5 - The two structures assumed by the left-side converter: a) S_2, D_2 on; b) S_2, D_2 off.

$$\begin{cases} \gamma = 1 \Rightarrow S_2, D_2 \text{ ON}; \quad S_1, D_1 \text{ OFF} \\ \gamma = 0 \Rightarrow S_2, D_2 \text{ OFF}; \quad S_1, D_1 \text{ ON} \end{cases} \; ; \; \bar{\gamma} = (1 - \gamma) \quad . \tag{15}$$

Using similar definitions for the error variables as in the previous section, state error equation (16) can be written. Here again, the term d/dt $[\ldots]^{\mathrm{T}}$ vanishes.

$$\begin{bmatrix} \varepsilon'_{i_{L_{ac}}} \\ \varepsilon'_{v_{C_1}} \\ \varepsilon'_{i_{L_{dc_1}}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L_{ac}} & 0 \\ \frac{-1}{C_1} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{L_{ac}} \\ v_{C_1} \\ i_{L_{dc_1}} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{i_{L_{dc_1}}}{C_1} \\ \frac{-v_{C_1}}{L_{dc_1}} \end{bmatrix} \cdot \bar{\gamma} + \begin{bmatrix} \frac{-v_{ac} - v^*_{C_2}}{L_{ac}} \\ 0 \\ \frac{V_{dc}}{L_{dc}} \end{bmatrix} -$$

$$- \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i^*_{L_{ac}} & v^*_{C_1} & i^*_{L_{dc_1}} \end{bmatrix}^{\mathrm{T}} \tag{16}$$

III - Control Strategy

The system is controlled by sliding mode or sliding regime. A sliding-mode controller changes its structure in order to bring and keep the output close to the desired condition [6]-[11]. It is well suited to power electronics circuits, because they present a particular structure for each state of the switches, naturally changing their structures according to switching actions. The sliding mode takes place in the error state space, in which a trajectory crossing the origin is designed. When the representative point of the system reaches the trajectory, it is confined close to it, and then directed toward the origin of the space. (The origin represents the desired condition: null error.) This trajectory is called *sliding surface* (σ), and the motion, *sliding mode* or *sliding regime*. The designed sliding surface divides the space into two subspaces, each one associated to a structure. One must ensure that the motion in the neighbourhood of σ be directed toward the surface, so that the representative point does not deviate from the specified trajectory. This is known as the *existence condition*, mathematically expressed by (17) (σ′ = dσ/dt).

$$\lim_{\sigma \to 0^-} \sigma' > 0 \quad \text{and} \quad \lim_{\sigma \to 0^+} \sigma' < 0 \quad . \tag{17}$$

The practical sliding mode does not occur exactly on the sliding surface all the time, since this would require an infinite switching frequency. In fact, it happens very close to it, giving rise to what is called a *quasi-sliding mode* [8]. Alternatively, *sliding mode* can be used in generic sense, reserving the expression *limit sliding-mode* for the theoretical case [11]. A simple way to implement the quasi-sliding mode is by hysteretic comparison between the actual state and the desired trajectory.

Equation (18) defines the right-side sliding surface σ_R. It is a weighted sum of the error variables. Taking s_1 and s_2 constant, the "surface" becomes, in fact, a straight line in the plane $\varepsilon_{vC2} \times \varepsilon_{iLdc1}$, completely determined by its slope, $\alpha = s_1 / s_2$. Units: s_2 in ohms, α in siemens; s_1 is dimensionless.

$$\sigma_R = s_1 \cdot \varepsilon_{v_{C_2}} + s_2 \cdot \varepsilon_{i_{Ldc_2}} \quad . \tag{18}$$

Due to the definition adopted for the error variables (9), whenever the representative point lies below the switching line σ_R, there is few energy in the storing elements C_2 and

L_{dc2}, and thus γ is set to 1. Conversely, the subspace above σ_R is associated to surplus energy and to $\gamma = 0$.

From condition (17), it is found that:

$$0 < \alpha < \left[V_{dc} \cdot C_2 \Big/ \left(L_{dc_2} \cdot I^*_{L_{ac_p}} \right) \right] \ , \tag{19}$$

and also the minimum v_{C2} for the sliding regime to take place:

$$v_{C_2}(t) > V_{dc} + \max\left\{ \alpha \cdot Z^2_{n_R} \cdot \left[i^*_{L_{ac}}(t) + i_{L_{dc_2}}(t) \right] \ , \ 0 \right\} \ , \tag{20}$$

where $Z_{n_R} = \sqrt{L_{dc_2} / C_2}$.

Using a fixed hysteresis width $\Delta\sigma_R$, steady-state switching frequency becomes dependent on the point of operation (duty cycle and current through L_{ac}):

$$f_{s_R}(t) = \left[d_R(t) / \Delta\sigma_R \right] \cdot \left[s_2 \cdot V_{dc} / L_{dc_2} + s_1 \cdot i^*_{L_{ac}}(t) / C_2 \right] \ . \tag{21}$$

When $i_{L_{ac}}$ reaches its negative peak value, the variations of i_{Ldc2} and v_{C2} become maximum. In AC-DC operation, this happens at $\varphi = \omega t = \pi/2$ rad, and both duty cycle and switching frequency are at their minimum. So, L_{dc2} and C_2 can be chosen according to (22), and also the hysteresis width must be elected accordingly. Another aspect to be considered when determining C_2 is its low-frequency current, which should not exceed 5% or 10% of rated $i_{L_{ac}}$*.

$$L_{dc_2} \geq \frac{V_{dc} \cdot d_{R_{min}}}{\Delta I_{L_{dc2_{max}}} \cdot f_{s_{R_{min}}}} \quad \text{and} \quad C_2 \geq \frac{I^*_{L_{ac_p}} \cdot d_{R_{min}}}{\Delta V_{C_{2_{max}}} \cdot f_{s_{R_{min}}}} \ . \tag{22}$$

The left-side third-order converter requires a bidimensional sliding surface σ_L, defined in (23). The election of s_4 and s_5 follows the same procedure adopted for the right-side sliding-mode controller. The parameter s_3 is chosen at last, after considering the maximum value of $|v_{L_{ac}}|$. The evolution of $i_{L_{ac}}(t)$ does not remarkably affect the switching frequency and the duty cycle, so basically the equations for the left side are close to those established for the right side, with a π rad phase-shift. Also equation (22) is used for sizing L_{dc1} and C_1, and L_{ac} is elected to give an appropriate resonant frequency with the paralleled C_1 and C_2.

$$\sigma_L = s_3 \cdot \varepsilon_{i_{L_{ac}}} + s_4 \cdot \varepsilon_{v_{C_1}} + s_5 \cdot \varepsilon_{i_{Ldc_1}} \ . \tag{23}$$

This way of considering the whole system as the interconnection of two or more subsystems, each one driven by an independent single-input control circuit, is known as *decentralised switching scheme* [8].

As a matter of fact, on the right side, only the reference for the output variable v_{C2} is explicitly declared, and ε_{vC2} is denominated the *ruling parameter*; i_{Ldc2}, here called *secondary variable*, depends upon instantaneous operational conditions and energy demand of the circuit, so its reference is difficult to determine. It is important to observe that, while v_{C2} governs the converter's macroscopical behaviour, the short on and off intervals are mainly dictated by the excursions of i_{Ldc2}, so that only its sharp, high-frequency trips are necessary to the controller. In this way, signal $\varepsilon^e_{i_{Ldc2}}$ is actually obtained after a high-pass filtering on the sensed variable (carrying the superscript "*e*", which means "estimated"). The low-frequency i_{Ldc2} is assumed to naturally adapt itself to circuit demands.

Similarly, on the left side, $\varepsilon_{i_{Lac}}$ is the ruling parameter, reference $i_{L_{ac}}$* is well defined, while secondary variables v_{C1} and i_{Ldc1} are high-pass filtered.

This use of high-pass filters is well suited to DC-DC converters [12]-[15]. In the present application, the low-frequency AC evolutions (up to doubled mains frequency) can be considered as quasi-static, therefore allowing the use of the same technique, similarly as it has been shown in [2]-[4], [16]. Of course the inclusion of each filter contributes to increase the order of the system. It is desirable to have fast filters, with high cutoff frequency, in order not to alter greatly the dynamics of the circuit, but on the other hand they must present some sensitivity to the resonant frequency of L_{dc1} and C_1 (or L_{dc2} and C_2), remembering that the resonant frequency in a switched circuit depends also on the duty cycle [17].

A general portrait of the converter and its sliding-mode controllers is depicted in Fig. 6. One can see the power circuit, the signals to be measured, the high-pass filters, the definitions of the surfaces σ_L and σ_R, the hysteretic comparators, and also a sketch of the reference signals to be followed.

During start-up, first the DC value of v_{C2} is established, then S_A is turned on; at last, the AC values are slowly increased.

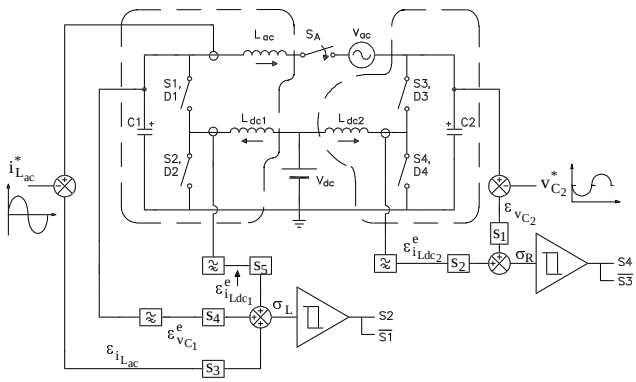


Fig. 6 - General portrait of the system. With the decentralised scheme, two sliding surfaces are defined, each one applied to a switching cell.

IV - Design Example and Simulation Results

A system was designed to perform 1kW DC-AC and AC-DC power transfer between the sources specified below:

- V_{dc} = 100V;
- $v_{ac}(t)$ = 311 sinωt;
- f_{ac} = 60Hz.

The reference functions are defined in (24) and (25). (The latter must be shifted by π rad when considering AC-DC operation.) With $V_{C2_{dc}}$* = 305V, it is assured at least a

50V difference between v_{C_2} and V_{dc} (and also between v_{C_1} and V_{dc}).

$$v^*_{C_2}(t) = 305 - 155.5\sin\omega t \quad \text{(V)} \;; \tag{24}$$

$$i^*_{L_{ac}}(t) = 6.43\sin\omega t \quad \text{(A)} \;. \tag{25}$$

In order to highlight the independence of the subsystems, the switching frequencies are selected to lie in a different range for each converter: from 13kHz to 65kHz on the right side and from 26kHz to 120kHz on the left side.

The right-side parameters are: $L_{dc2} = 471\mu$H and $C_2 = 16.8\mu$F; α must be lower than 0.55S, thus $s_1 = 0.02$ and $s_2 = 0.1\Omega$ are chosen. Moreover, the total hysteresis width is selected as $\Delta\sigma_R = 0.35$V. A first-order high-pass filter tuned to 1.2kHz is used for obtaining $\varepsilon^e_{i_{Ldc2}}$.

On the left side: $L_{dc1} = 130\mu$H, $C_1 = 5.3\mu$F, and $L_{ac} = 300\mu$H ; $s_3 = 0.2\Omega$, $s_4 = 0.021$, and $s_5 = 0.11\Omega$. Total hysteresis width is $\Delta\sigma_L = 0.66$V. High-pass filters: both (for i_{Ldc_1} and for v_{C_2}) are Butterworth second-order filters tuned to 1kHz.

Due to the combination of parameters in (21), the widest variation of the switching frequency occurs under full-load AC-DC operation, becoming minimum under full-load inverter operation, as illustrated in Fig. 7a for the right side.

Fig. 7b shows the theoretical curves of duty cycles on both sides as functions of $\varphi = \omega t$. They range from 0.33 to 0.78. Theoretical i_{Ldc_2} for full-load inverter operation can be seen in Fig. 7c (excluding high-frequency trips).

The system was simulated through the program *VisSim*™. The main results are shown in Figs. 8 and 9 for inverter mode and in Fig. 10 for AC-DC operation. Numerical values (analytical and obtained in simulations) are summarised in Table I.

TABLE I

COMPARISON BETWEEN VALUES OBTAINED THROUGH ANALYSES AND THROUGH NUMERICAL SIMULATIONS

Inverter Mode				
AC Current: 6.54 / -0.04° (A) (theoretical: 6.43 / 0°) THD ≅ 4.9%; transferred power: 1017W.				
	Left-side converter		Right-side converter	
Parameter	Theor.	Simul.	Theor.	Simul.
$i_{Ldc\,(avg)}$ (A)	5.00	5.17	5.00	5.01
$i_{Ldc\,(rms)}$ (A)	15.3	15.7	15.4	15.6
f_s (kHz), $\varphi = 0°$	78.3	82.3	40.8	42.0
$\varphi = 90°$	62.5	65.8	27.5	26.8
$\varphi = 180°$	78.3	80.6	40.8	36.4
$\varphi = 270°$	50.8	54.1	30.4	29.9
Rectifier Mode				
AC Current: 6.50 / 179.98° (A) (theoretical: 6.43 / 180°) THD < 1%; transferred power: -1010W.				
	Left-side converter		Right-side converter	
Parameter	Theor.	Simul.	Theor.	Simul.
$i_{Ldc\,(avg)}$ (A)	-5.00	-4.87	-5.00	-5.12
$i_{Ldc\,(rms)}$ (A)	15.3	15.4	15.4	15.8
f_s (kHz), $\varphi = 0°$	77.2	81.1	40.8	40.5
$\varphi = 90°$	120.0	121.3	12.9	12.6
$\varphi = 180°$	78.3	85.7	40.8	48.9
$\varphi = 270°$	26.4	28.4	65.0	61.3

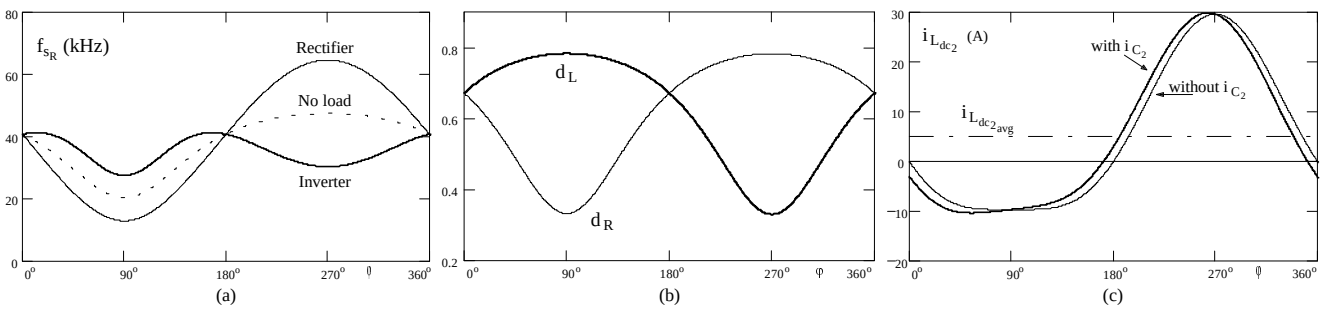


Fig. 7 - Theoretical curves: a) Right-side switching frequency regarding the following cases: full-load AC-DC, no-load, and full-load DC-AC operation; b) duty cycles on both sides (concerning either AC-DC or DC-AC power flow); c) current through L_{dc2} for inverter operation, considering and not considering the current required by C_2 (compare to Fig. 8e); the positive average current indicates power flowing *from* the DC source.

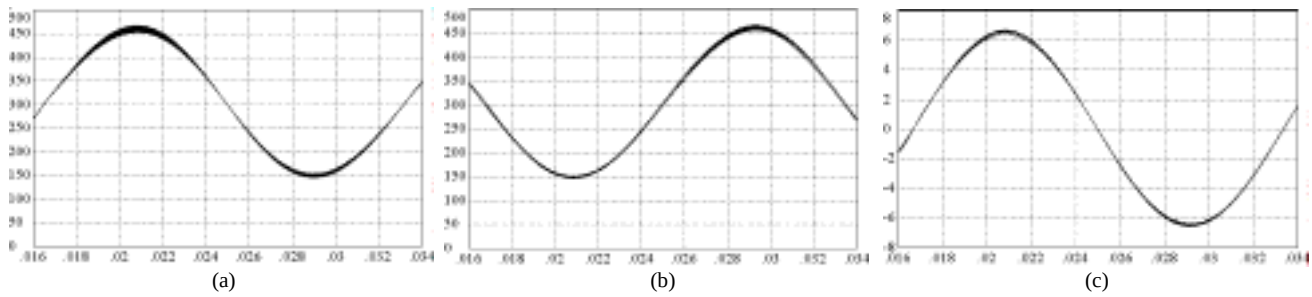
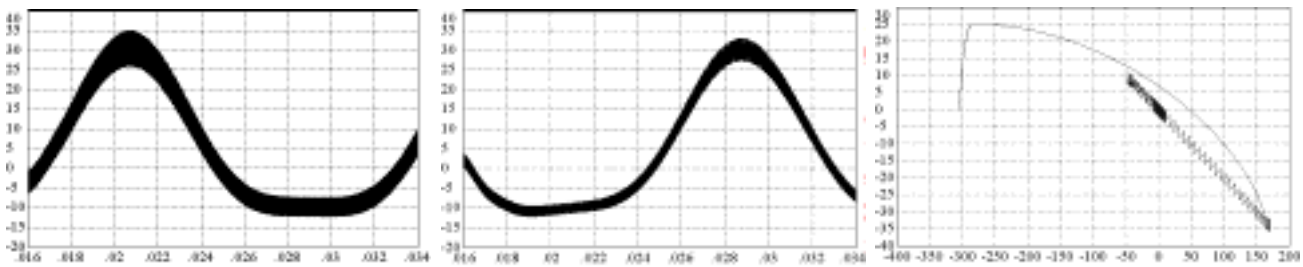
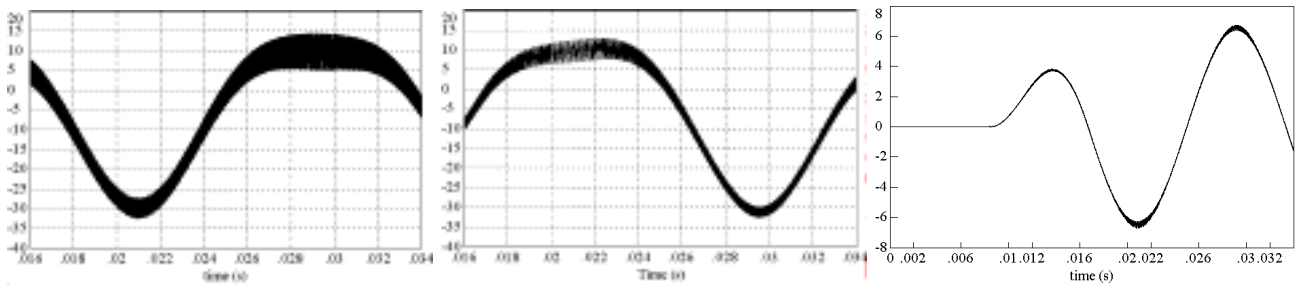


Fig. 8 - Simulation results of the converter acting as inverter: a) v_{C1}; b) v_{C2}; c) i_{Lac} (time in seconds).



(a) (b) (c)

Fig.9 - More simulation results concerning inverter-mode operation: a) i_{Ldc1}; b) i_{Ldc2} (time in seconds); c) right-side state error plane $\varepsilon_{vC2} \times \varepsilon^{e}_{iLdc2}$, showing start-up from rest, including limitation on the current through L_{dc2}.



(a) (b) (c)

Fig. 10 - Simulation results for AC-DC operation: a) i_{Ldc1}; b) i_{Ldc2}; a) i_{Lac}, shown from t = 0: during the first half period, S_A is kept off, and no current flows through L_{ac}; afterwards the current slowly increases, reaching rated condition at t = 16.7ms.

V - Conclusion

The step-up inverter showed to be an interesting way to perform AC-to-DC and/or DC-to-AC power transfer, with no concerns about the relative voltage levels at the DC and the AC sides. The sliding-mode controller with decentralised switching scheme fits very well for this circuit to find and track the time-varying reference functions. These functions are only defined for the two output variables; the other signals are high-pass filtered. The use of such filters does not remarkably degrade the overall performance of the system.

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