A NEW ZVS-PWM CLAMPING MODE ISOLATED NON PULSATING INPUT AND OUTPUT CURRENT DC-TO-DC CONVERTER.

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Abstract - In this paper a new converter capable of operating in high frequency, featuring high efficiency and improved circuit EMI characteristics is presented. The main characteristic of this converter is to work with non-pulsating input and output current. Besides, it presents zero-voltage switching (ZVS) in the main and auxiliary switches as well as minimum voltage stress. The principle of operation is explained and experimental results taken from a 600W, 25kHz-laboratory prototype is presented.

I. - INTRODUCTION

It is known that the current-fed flyback push-pull converter has several advantages with respect to the conventional voltage or current-fed ones. However, the largest advantage is that it has two forms of processing energy that allow a larger efficiency for a given power or a larger amount of processed energy for a given efficiency.

As it was already discussed in [1,4] the mentioned converters have two important disadvantages:

- The sensibility to the leakage inductance of its transformers.
- And the fact of having pulsed currents in the input or in the output depending on the operation mode. If it works in buck mode the input current is pulsed; whereas if it works in boost mode the output current is pulsed. This behavior increases the emission of electromagnetic interference irradiated.

This paper presents a solution for the problems above described.

II. THE PROPOSED CIRCUIT

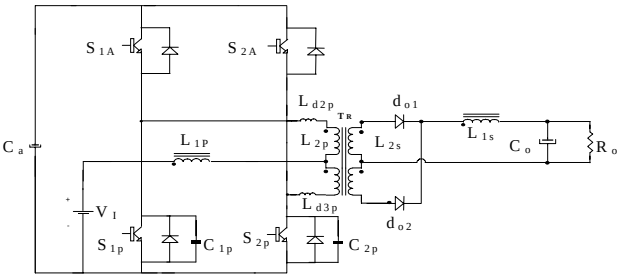
The circuit introduced in this paper was born from the application of the active Boost type clamping [2] to the new flyback-push-pull converter [1], generating a robust and efficient circuit.

The new circuit is robust due to its immunity against leakage inductance variations in the two transformers connected in series. These inductances are included, in the case of the push-pull transformer, to the commutation process and in the case of the flyback transformer, to the energy transfer process.

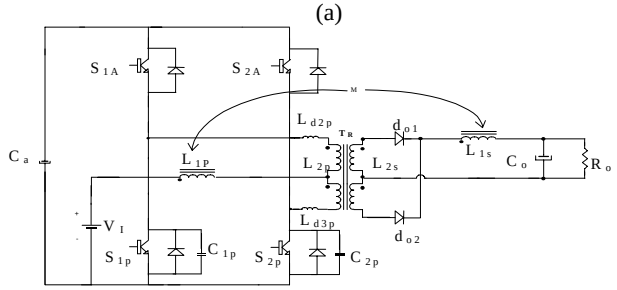
Also, the converter efficiency is closely associated with the fact that it has two forms energy processing: direct, through the push-pull transformer, and indirect, through capacitive accumulation.

The circuit can work without coupling of the input and output inductors in the same way as the Cuk converter [3], but in this configuration, the converters volume will increase.

The only disadvantage observed in the proposed converter is that it requires two auxiliary switches, but it is possible to only have it with one auxiliary switch [4]. The proposed converter is shown in Fig. 1.



(a)



(b)

Fig. 1 - New converter a) non-coupled version and b) version with coupled input and output inductors.

III. PRINCIPLE OF OPERATION

The main waveforms of the converter are shown in the Fig 2. In Fig. 2(a) and 2(b) the gating signals of the main and auxiliary switches are shown. Fig. 2(c) shows the current through the main switch (IS_{1p}), the output diodes (d_o) and the auxiliary switch of the same pole (dashed line). Fig. 2(d) shows the current through the accumulation capacitor and finally, Fig. 2(e) shows the input current (iL_{1P}). The converter has a total of ten stages for an operation cycle, however it is necessary to describe only five, i.e. for half period, since in the other portion of the period the operation is analogous.

1ª Stage (t_0,t_1) Clamping capacitor's linear charge.

At instant t=t_0, A gate-drive signal is applied to S_{1p} and S_{2a} while its body diodes are conducting, therefore they will commute without losses. In this stage the current in L_{1p} begins to increase and the source *Vi* supplies energy to the accumulative capacitor C_a and to the load.

A current flow in both transformers' primary windings yielding that d_{01} and d_{02} turns on and the output current starts to free wheel. At t=t_x the current in the winding L_{2p} reaches zero. The diode d_{1p} is reverse biased and the switch S_{1p} turns on, while the current through C_a decreases.

2ª Stage (t_1-t_2) Energy transfer.

At t=t_1 iL_{1p} it reaches its maximum value and the current through the capacitor C_a reaches zero and inverts its direction. In this stage, energy is transferred from the source and of the capacitor C_a for the load. The commutation inductance and leakage inductance of the push-pull transformer are negligible in this stage due to that its currents are almost constant and only the input inductance L_i (that is the flyback transformer leakage inductance) will have influence, due to its larger value.

3ª Stage (t_2-t_3) The first commutation.

At t=t_2 S_{1p} is turns off, triggering the first process of lineal commutation. The capacitor C_{1p} assumes the current allowing soft commutation in the switch. Note that the leakage inductance is used in the commutation. Due to the polarity of the current in L_{3p} and in L_{2p}, the diode d_{01} will be blocked and the conduction of the diode d_{02} will be reinforced in the output circuit.

4ª Stage (t_3-t_4) Clamping capacitor's linear discharge.

At t=t_3 the voltage across C_{1p} reaches $V_i/(1-D)$ causing d_{1a} to turn on, a portion of energy stored in the input inductance, as well as, of energy of the source are stored in it. The switch S_{1a} can be gating under zero voltage. The currents through the inductance Ld_{2p} and Ld_{3p} are constant, and therefore, they do not influence this stage.

5ª Stage (t_4 – T/2) The Second commutation.

At t=t_4, S_{2a} is turn off causing C_{2p} to assume the current and prepare S_{2p} to commute under zero voltage, at t=T/2. When S_{2p} turns on, the next semi-cycle of operation begins.

III. TRANSFER CHARACTERISTIC FOR D<0,5.

In order to obtain the output characteristic is known that average flux in the flyback inductor is zero, in a commutation period, then neglected the commutation intervals, the following equation is obtained:

$$V_{L1P_{\Delta t_1}} \cdot \Delta t_1 + V_{L1P_{\Delta t_5}} \cdot \Delta t_5 = V_{L1P_{\Delta t_2}} \cdot \Delta t_2 \qquad (1)$$

Substituting the expressions and with some algebraic work, the gain is obtained in function of the duty cycle and the input current ripple as a:

$$\frac{V_o}{V_i} = \frac{D}{N \cdot (1-D)} - \frac{\Delta I \cdot (2 \cdot L_i - L_d)}{V_i \cdot T \cdot N \cdot (1-D)} \qquad (2)$$

The input current ripple is normalized as shown:

$$\overline{\Delta I} = \frac{\Delta I \cdot L_d}{V_i \cdot T}, \quad \zeta = \frac{L_i}{L_d}, \quad \overline{V_o} = \frac{N \cdot V_o}{V_i} \text{ and } L_{d2P}=L_{d3P}=L_d$$

With equal flyback and push-pull transformers turns-ratio (*N*).

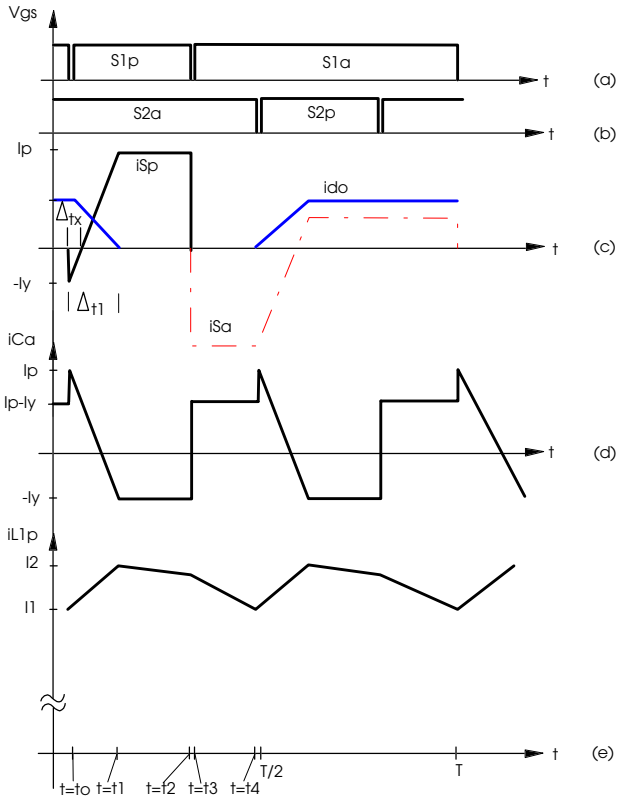


Fig. 2 – Relevant waveforms.

Hence:

$$\overline{V_o} = \frac{D}{(1-D)} - \frac{\overline{\Delta I} \cdot (2 \cdot \zeta - 1)}{(1-D)} \qquad (3)$$

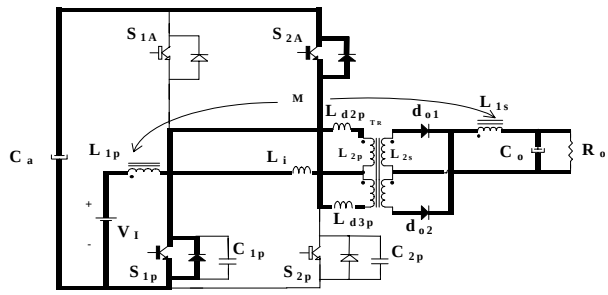


Fig. 3 – First stage.

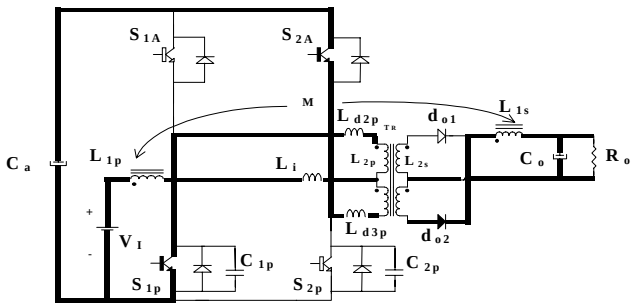


Fig. 4 – Second stage.

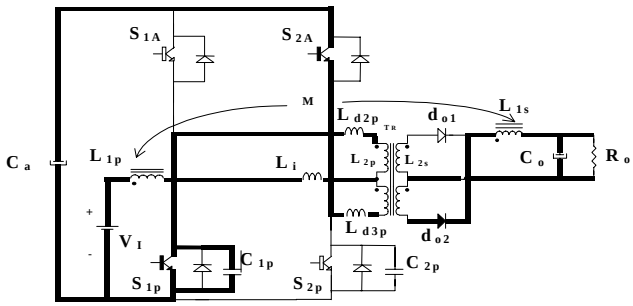


Fig. 5 – Third stage

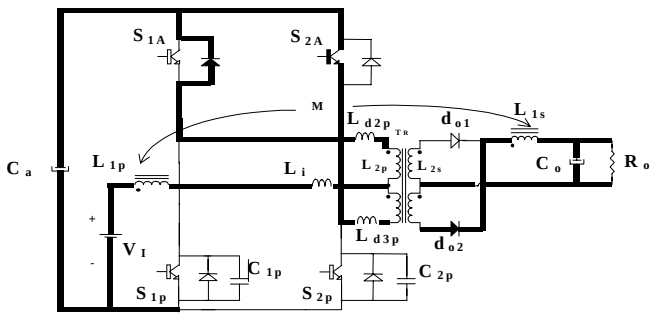


Fig. 6 – Fourth stage.

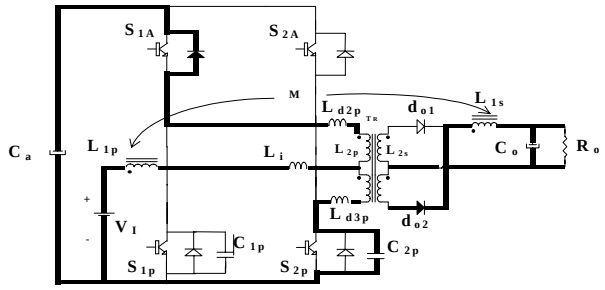


Fig. 7 – Fifth stage.

In the former expression, the gain of the converter is a function of the input current ripple, thus not being a good representation. Therefore, the connection is sought between this ripple and the output current.

The input current ripple is given by:

$$\Delta I = \frac{(V_i + N \cdot V_o) \cdot D \cdot T}{L_d \cdot (2 \cdot \zeta - 1)} - \frac{D \cdot T \cdot (V_i + N \cdot V_o)}{L_d \cdot (2 \cdot \zeta - 1)} \cdot \sqrt{1 - \frac{I_i \cdot L_d \cdot (2 \cdot \zeta - 1)}{(V_i + N \cdot V_o) \cdot D^2 \cdot T \cdot (\zeta + 1)}} \quad (4)$$

Knowing that:

$$I_i = \frac{V_o \cdot I_o}{\eta \cdot V_i} \;,\; \overline{I_o} = \frac{L_d \cdot I_o}{V_i \cdot T \cdot N} \quad \text{e} \quad \overline{V_o} = \frac{N \cdot V_o}{V_i} \quad (5)$$

The normalized input current ripple is obtained as a function of the gain, the duty cycle and the normalized output current, as shown in the following equation:

$$\overline{\Delta I} = \frac{(1+\overline{V_o}) \cdot D}{(2 \cdot \zeta - 1)} \cdot \left(1 - \sqrt{1 - \frac{\overline{V_o} \cdot \overline{I_o} \cdot (2 \cdot \zeta - 1`)}{(1+\overline{V_o}) \cdot \eta \cdot D^2 \cdot (\zeta + 1)}} \right) \quad (6)$$

Substituting the previous expression in the gain equation, given in (3), the normalized gain is obtained:

$$\overline{V_o} = \frac{\left(2 \cdot D^2 - \frac{\overline{I_o} \cdot (2 \cdot \zeta - 1)}{\eta \cdot (\zeta + 1)} \right) + \left(\sqrt{\left(\frac{\overline{I_o^2} \cdot (2 \cdot \zeta - 1)^2}{\eta^2 \cdot (\zeta + 1)^2} + 4 \cdot D^2 \right)} \right)}{2 \cdot \left(1 - D^2 + \frac{\overline{I_o} \cdot (2 \cdot \zeta - 1)}{\eta \cdot (\zeta + 1)} \right)} \quad (7)$$

IV. DESIGN METODOLOGY

Following a design procedure is proposed, for a switching supply based on the new converter.

a. - Specifications

These general specifications are:

- V_I input Voltage
- V_o output Voltage
- P_o output Power
- F_s commutation Frequency
- η Efficiency
- D Duty cycle
- ζ Ratio between Li and Ld.

The latter specification is very important because it furnishes a notion of the input current ripple. For continuous current, ζ >1 is necessary. However this value cannot be excessive (ζ >50) since if the use of the proper leakage of the transformer flyback is requested, large values will imply in the use of a very volumous core. Therefore, an acceptable value (for acceptable cores) it is 10 < ζ <20. For this project the used value was $\zeta = 10$.

b. – Calculation of N.

For the calculation of the transformer turns ratio the ideal gain is used, obtained from the real gain equation:

$$N \cdot \frac{V_o}{V_i} = \frac{D - \overline{\Delta I} \cdot (2 \cdot \zeta - 1)}{(1 - D)} \quad (8)$$

The ideal gain is that obtained when the input current ripple is zero, i.e. when the leakage inductance in the transformer flyback, as well as the push-pull are neglected. Hence the transformation ratio is given for:

$$N = \frac{V_i \cdot D}{V_o \cdot (1 - D)} \quad (9)$$

c. – Calculation of normalized gain $\overline{V_o}$.

The voltage gain can be calculated using the obtained transformer ratio, as shown bellow:

$$\overline{V_o} = N \cdot \frac{V_o}{V_i} \tag{10}$$

d. – Calculation of the commutation inductances (L_d).

With the specifications of D and ζ and with the obtained $\overline{V_o}$ it is possible to obtain $\overline{I_o}$ from the output characteristic, with this values, the commutation inductance can be calculated as:

$$L_d = \frac{\overline{I_o} \cdot V_i \cdot N}{F_S \cdot I_o} \tag{11}$$

With $\overline{I_o}$ is also possible to calculate the normalized input ripple $\overline{\Delta I}$.

e. – Calculation of the commutation capacitors.

The calculation of the commutation capacitors can be obtained directly from the equations of the time intervals in the stages [5]. The calculation is done for the worst case, being the second commutation the more critic, therefore:

$$C_p = \frac{I_y \cdot \Delta t_6}{V_{C_a}} \tag{12}$$

The commutation interval Δt_6 must be much smaller than the dead time between switches in the same leg.

V. EXPERIMENTAL PROTOTYPE: DESIGN AND BUILDING

a. – Design example.

The specifications used were the same as in [1], therefore:

$$P_o = 600W \quad \eta = 0.9 \quad V_i = 48 \quad F_S = 25kHz$$

$$V_o = 60V \quad I_o = 10A \quad N = 0.33 \quad D = 0.4$$

And

$$\zeta = 10 .$$

In this case a duty cycle D=0.4 was used, due the fact that for D=0.3 the obtained leakage inductance was too small, compromising the soft commutation.

Firstly the value of the normalized gain of the converter is calculated, hence:

$$\overline{V_o} = \frac{N \cdot V_o}{V_i} = 0.33 \cdot \frac{60}{48} = 0.4125 \tag{13}$$

Once obtained the values of M, N and D, the relative output current ($\overline{I_o}$) is obtained from the curve of the gain of the converter with active clamping, yielding $\overline{I_o} = 0.136$. The relative ripple therefore is $\overline{\Delta I} = 0.017$ or $\Delta I = 3.682A$.

The commutation inductance is calculated bellow:

$$L_d = \frac{\overline{I_o} \cdot V_i \cdot N}{F_S \cdot I_o} = 8{,}617\mu H \tag{14}$$

The L_i/L_d ratio is chosen as $\zeta = 10$, in an attempt of optimization of the ferrite core, in order to compatible inductance. Hence L_I =87μH.

The calculation of the commutation capacitors is done through equation 12. Knowing that the clamping voltage is given from:

$$V_{C_a} = \frac{V_i}{(1-D)} \tag{15}$$

Therefore for D=0.4, V_{ca} = 80V the negative peak is obtained [5] Iy=10,644A.

The commutation time interval is calculated as being 7 times smaller than the dead time Tm, given in the gating circuit. In this case for the circuit integrated (IRF2111) is Tm=700ns, hence is assumed Δt_6 = 100ns.

$$C_p = \frac{I_y \cdot \Delta t_6}{V_{C_a}} = 13.305nF \tag{16}$$

The commercial value used was 15nF.

b. - Experimental Results.

The power and control circuits of the experimental prototype are shown in Fig. 8a and Fig. 8b respectively. Four switches two transformers and two diodes constitute the power circuit. The isolated command of the switches of the same leg is obtained through the IRF2111 integrated circuit. The experimental results were obtained at rated load power, which is equal to 600W.

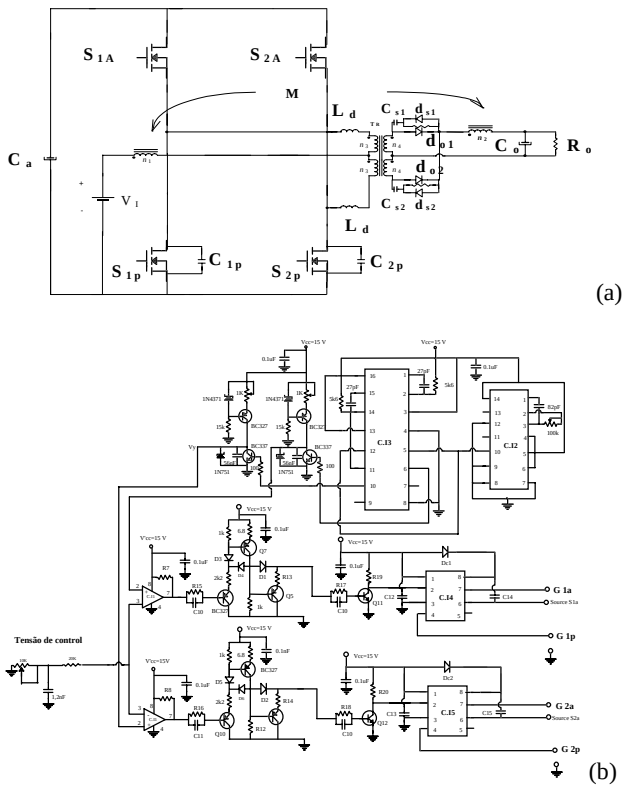


Fig. 8 - Power (a) and control (b) diagrams.

Fig. 9 shows the currents in the primary (upper curve, IL_{1p}) and in the secondary winding (lower curve, IL_{1s}) of the flyback transformer. Note that there is continuous current in the input and in the output, so the converter is working as a DC-DC transformer. This means that there is no regeneration of the commutation and leakage inductance energy to the source. Instead, the energy is redirected to the load through the accumulation capacitor.

This reduces the circulating reactive energy in the converter.

(a) Table N° 1: Power circuit.

S_{1P} , S_{2P}, S_{1A}, S_{2A}	IRFP150
do_1, do_2	MUR1530
Ds_1,ds_2 snubber output diodes	SKE 4f2/04
Cs_1,Cs_2 snubber output diodes	4700pf 1.6KV polypropylene
Rs_1,Rs_2 snubber output diodes	47KΩ 1/2W
Co Output capacitor	47uF 250V
Ca Accumulation capacitor	15uF 250V polypropylene
C_{1P}, C_{2P}	15nF 250V polypropylene
L_d Commutation Inductors core E-30/7 Gap approximately 4 mm.	n=12 turns AWG22
Flyback transformer core E-65/26 N=0.33 Gap approximately 2 mm.	n_1=9 turns AWG22 13 wires. n_2=27 turns. AWG22 8 wires.
T_R *Push-pull* Transformer core E-65/26 N=0.33	n_3=6 turns AWG22, 9 wires. n_4=18 turns AWG22, 5 wires.

(b) Table N° 2: Control circuit.

P1	Potentiometer de 56 KΩ
P2,P3,	Potentiometer de 1KΩ
P4	Potentiometer de 10 KΩ
R_1, R_2	5,6KΩ 1/8W
R_3, R_4	15 KΩ 1/8W
R_5, R_6	100Ω 1/8W
R_7, R_8	1KΩ 1/8W
R_9, R10	15KΩ 1/4W
R11, R12	1KΩ 1/4W
R13, R14	15KΩ 1/4W
R15, R16	1KΩ 1/4W
C_1	82pF
C_2	100nF
C_3,C_4,C_5	56nF
C_6,C_7	27pF
C_8,C_9	100nF
C_{10},C_{11}	1nF
D_1,D_2,D_3,D_4,D_5,D_6	1N4148
Dz_1,Dz_2	2.7V 1N4371
Dz_3,Dz_4	5.1V 1N751
Q_1,Q_2	BC558B PNP
Q_3,Q_4	BC537 NPN
Q_5,Q_6,Q_7,Q_8,Q_9,Q_{10}	BC327 PNP
C.I1	LM311
C.I2	CD4047BE
C.I3	CD4528BE
CI4,CI5	IRF2111
R17,R18,R19,R20	1KΩ 1/8W
C12,C13,C14,C15	0,1uF
Dc1,Dc2	1N4936
Q11,Q12	BC337 NPN

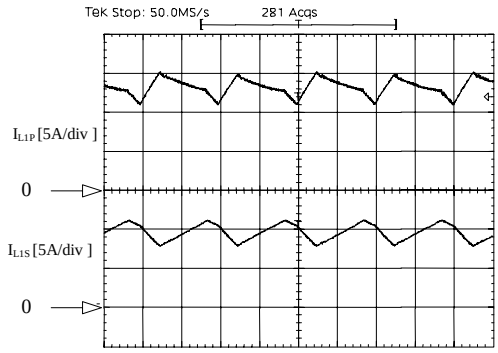
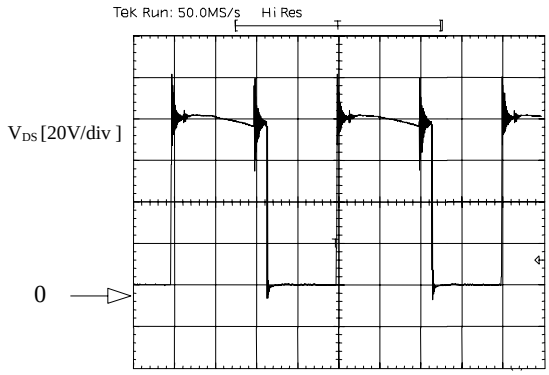


Fig. 9 - Flyback transformer currents (10 μ s/div).

Fig. 10 shows the voltages of the main and auxiliary MOSFET's; the effective clamping in the switches is clearly observed. The parasitic inductance of the circuit layout causes a voltage spike of approximately 22V. A possible solution for this situation is changing the position of the accumulation capacitor, placing it as near as possible of the switches.



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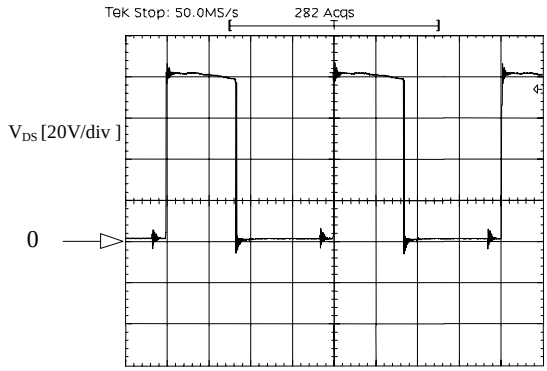


(b)

Fig. 10 – Switch voltages: a) Main b) Auxiliary (10 μs/div).

Fig. 11 shows the commutation process in the main switches at full load, 600W. The new circuit seems quite robust, since it maintained soft switching with less than 1/5 of the nominal power.

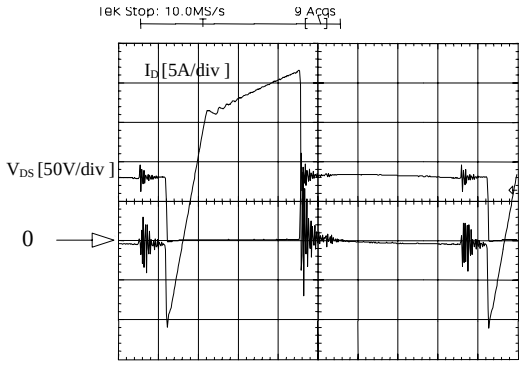
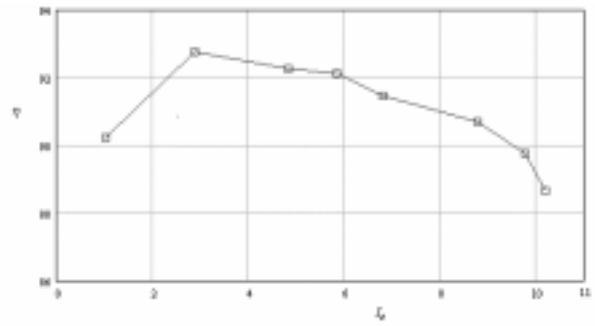


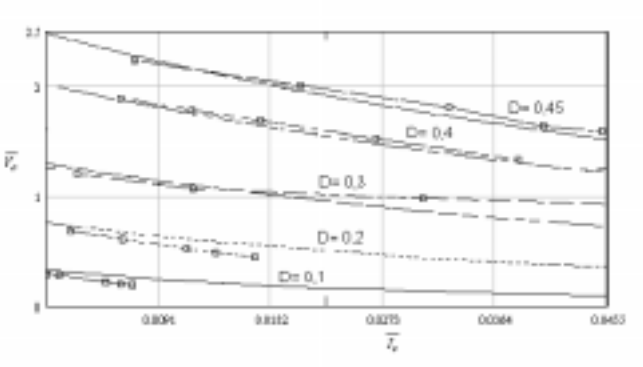
Fig. 11 - Commutation process in the main switches at full load (5 μ s/div).

Fig. 12(a) shows the experimentally obtained efficiency of the circuit. It is observed that in 400W the efficiency starts to decrease; at full load (600W) the efficiency is 89.4 percent.

Fig. 12(b) shows a comparison of the gain obtained experimentally (dot line) with that obtained theoretically.



(a)



(b)

Fig. 12 – (a) Experimental efficiency as a function of the output current. (b) Experimental gain.

IV. CONCLUSIONS

In this paper a new current-fed capacitive accumulation converter was presented. The new converter is capable of eliminating the problems of switch voltage overshoots due to the resonance between leakage inductance of the magnetic elements and the output capacitance of the MOSFETs.

The proposed converter provides soft commutation (ZVS) in the switches and non-pulsating input and output currents.

The inductance's energy is used for the commutation of the switches and later on is accumulated in the accumulation capacitor and regenerated to the load, guaranteeing low reactive energy in the circuit. As a consequence of the transfer of energy with continuous current in the input as well as in the output, the problems of the irradiated electromagnetic interference (EMI) are reduced.

V. REFERENCES

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