A Space Vector PWM Method for Three-Level Voltage Source Inverters

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Abstract— **In this paper, a space vector PWM method for three-level inverters is presented. In the proposed technique, boundary restrictions can be easily incorporated to minimize the harmonic distortion output voltages, to limit the minimum pulse width and to balance the voltages of the dc-link capacitor bank. The solutions obtained are simple algebraic equations relating directly the pulse widths of the gate signals to the phase reference voltages. Computer simulation results are used to demonstrate the main features of the proposed technique.**

I. Introduction

The recent developments of the power electronics industry resulted in a considerable increase of the power that can be manipulated by semiconductor devices. In spite of that, the maximum voltage supported by these devices remains the major obstacle in medium and high voltage applications. For such applications multilevel converters have been proposed [4], [5], [2]. Multilevel inverters present low harmonic distortion of the output voltages when compared to standard two-level inverters operating at the same switching frequency [4], [5], [2]. Several PWM methods have been proposed for multilevel inverters [1], [3].

In this paper, a space vector PWM method for three-level inverters is presented. In the proposed technique, boundary restrictions can be easily incorporated to minimize the harmonic distortion output voltages, to limit the minimum pulse width and to balance the voltages of the dc-link capacitor bank. The solutions obtained are simple algebraic equations relating directly the pulse widths of the gate signals to the phase reference voltages. Computer simulation results are used to demonstrate the main features of the proposed technique.

II. The three-level inverter

Fig. 1 shows the simplified circuit diagram of a three-level GTO inverter. Each phase has four GTO switches, four freewheeling diodes and two clamping diodes connected to the dc-link center tap.

Table I shows the possible switching states for a given inverter phase. The variable c_x, $(x \in \{a, b, c\})$, may be 1, 0 or -1 connecting the charge to points P, O or N, respectively.

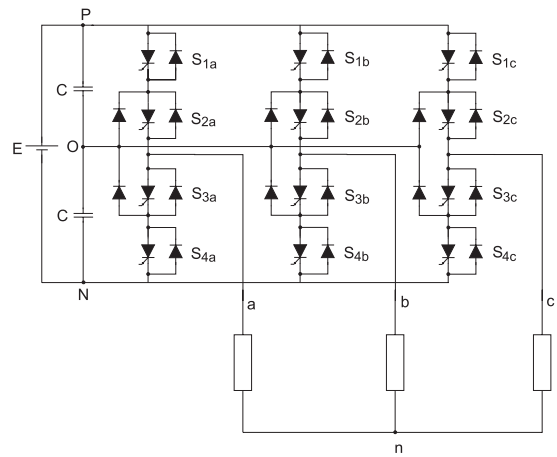

Fig. 1. Simplified circuit diagram of a three-level inverter

TABLE I
Switching states for a three level inverter

States	c_x	S_{1x}	S_{2x}	S_{3x}	S_{4x}
P	1	ON	ON	OFF	OFF
O	0	OFF	ON	ON	OFF
N	-1	OFF	OFF	ON	ON

Fig. 2 shows a typical control signal for a switching period. With three different switching states for each phase the three-level inverter of fig. 1 has 27 possible switching states.

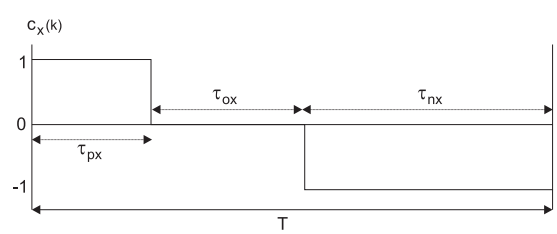

Fig. 2. Control signal c_x for a switching period

Fig. 3 shows all the voltage vectors generated by the inverter of Fig. 1. These voltages vectors can be grouped into four different classes: Z) zero vector V_0 having three

switching states; S) small amplitude vectors ($E/3$) having two different switching states each i.e., V_1, V_4, V_7, V_{10}, V_{13} and V_{16}; M) medium amplitude vectors ($\sqrt{3}E/3$) having only one switching state i.e., V_3, V_6, V_9, V_{12}, V_{15} and V_{18} and L) large amplitude vectors ($2E/3$) having only one switching state i.e., V_2, V_5, V_8, V_{11}, V_{14} and V_{17}.

In general, in standard space vector methods only three voltage vectors corresponding to the apexes of the triangle in which the reference voltage vector is inside are used and this reduces the harmonic content of the output voltages [1], [3].

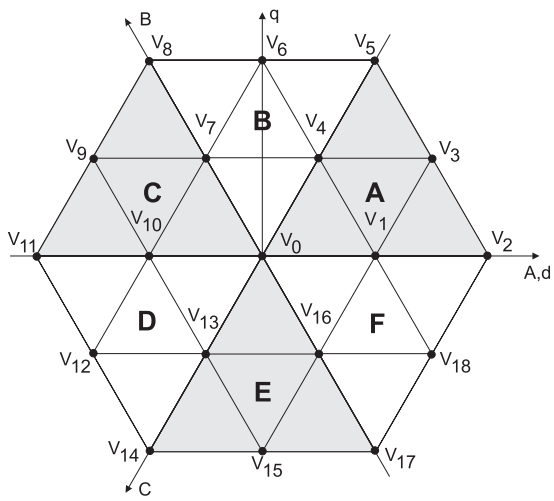

Fig. 3. Space voltage vectors of a three-level inverter

III. Basic equations

The output voltage $v_{xn}(t)$, can be expressed in terms of the control variable $c_x(t)$, as follows:

$$\begin{bmatrix} v_{an}(t) \\ v_{bn}(t) \\ v_{cn}(t) \end{bmatrix} = \frac{E}{6} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} c_a(t) \\ c_b(t) \\ c_c(t) \end{bmatrix} \tag{1}$$

The average value of the output voltages in the k-th switching period, $\bar{v}_{xn}(k)$, is calculated by:

$$\begin{bmatrix} \bar{v}_{an}(k) \\ \bar{v}_{bn}(k) \\ \bar{v}_{cn}(k) \end{bmatrix} = \frac{E}{6} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} \bar{c}_a(k) \\ \bar{c}_b(k) \\ \bar{c}_c(k) \end{bmatrix} \tag{2}$$

where, $\bar{c}_x(k)$ is the average value of the control signal of phase x in the k-th period. From figure 2 it easy to see that:

$$\bar{c}_x(k) = \frac{\tau_{px}(k) - \tau_{nx}(k)}{T} \tag{3}$$

Defining the average voltage vector in the k-th period, $\bar{V}_{dq}(k)$ by:

$$\bar{V}_{dq}(k) = \frac{2}{3}\left(\bar{v}_{an}(k) + a\bar{v}_{bn}(k) + a^2\bar{v}_{cn}(k)\right) \tag{4}$$

with a= $e^{j2\pi/3}$. Using the above equation and (2) it can be found that:

$$\bar{V}_{dq}(k) = \frac{E}{2}\frac{2}{3}\left(\bar{c}_a(k) + a\bar{c}_b(k) + a^2\bar{c}_c(k)\right) = \frac{E}{2}\bar{C}_{dq}(k) \tag{5}$$

where $\bar{C}_{dq}(k)$ is defined as the control vector of the three-level inverter in the k-th period. Then, for a given reference voltage vector $\bar{V}^*_{dq}(k)$ the control vector can be determined by:

$$\bar{C}_{dq}(k) = \frac{2}{E}\bar{V}^*_{dq}(k) \tag{6}$$

The zero sequence component for the control vector is defined by:

$$\bar{C}_0(k) = \frac{1}{3}(\bar{c}_a(k) + \bar{c}_b(k) + \bar{c}_c(k)) \tag{7}$$

It can be shown that the pulse widths τ_{px} and τ_{nx} can be determined by using equations (6) and (7) and the inverse dq transformation. The pulse widths are calculated by:

$$\tau_{px}(k) - \tau_{nx}(k) = \frac{2T}{E}\bar{v}^*_{xn}(k) + \bar{C}_0(k) \tag{8}$$

In order to determine the pulse widths for a given phase the zero sequence component $\bar{C}_0(k)$ must be selected. By a suitable choice of this component it is possible to balance the DC-link capacitors voltages and to reduce the load current ripple.

IV. Determining pulse widths in sector A

In order to simplify the study, the hexagon in Fig. 3 is divided into six sectors (A to F). In this section, the switching patterns for sector A will be defined. These results can be extended for the others sectors. Fig. 4 shows a expanded view of sector A with its subregions numbered from 1 to 4.

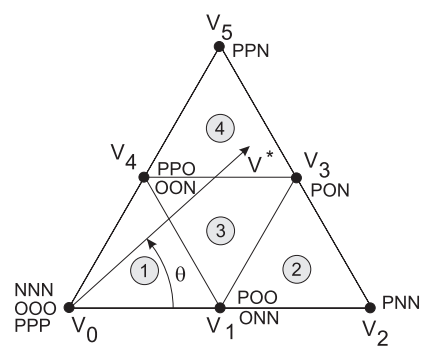

Fig. 4. Space voltage vectors in sector A

A. Balancing the DC-link capacitor voltages

Some of the vector groups defined previously (Z,S,M,L) affect the balancing of the DC-link capacitor voltages [3], [1]. The Z and L vectors do not affect the neutral-point voltage at all. The S vectors have two different switching states. One of these states connects the load to the upper

capacitor terminal and the other connects the load to the lower capacitor terminal. If the load is inductive these two switching states are almost symmetrical during the switching period and then the DC-link capacitor voltages can be balanced. The M vectors also affect the neutral voltage but have only one switching state and thus the balancing cannot be provided.

B. Switching patterns for subregion A1

The switching patterns consists in a ordered sequence of switching states corresponding to the voltage vectors of the inverter in a given region. The ordering of the vectors can minimize the number of commutations of the inverter switches. The subregion A1 contains three vectors (V_0, V_1 and V_4) corresponding to seven different switching states. If all switching states vectors are employed in this subregion to form the switching pattern the harmonic content of the output voltages is reduced. Such a pattern is named *complete pattern*. The complete switching pattern for subregion A1 is given by /PPP/PPO/POO/OOO/OON/ONN/NNN/. Fig. 5 shows the control signals of the the three phases of the inverter for this switching pattern during two switching periods. Notice that in consecutive switching states only one switch commutation occurs. A switching pattern that does not uses all the possible switching states is called *reduced pattern*. The use of reduced patterns will be treated in the next section.

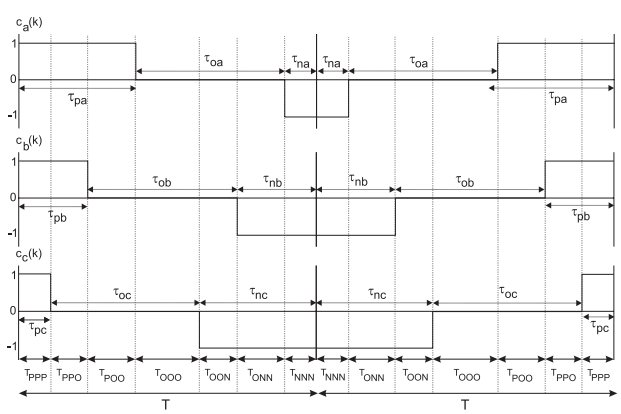

Fig. 5. Switching patterns for the subregion A1

In the first switching period the complete switching pattern is employed. In the second period the switching pattern is reversed minimizing the number of switch commutations. To reduce the load current ripple it is necessary to split uniformly the utilization of the zero voltage vector over the switching period. With respect to Fig. 5 this is obtained if $2T_{NNN} = T_{OOO}$ and $2T_{PPP} = T_{OOO}$.

As explained before, the balancing of the DC-link capacitor voltages is achieved if the switching states corresponding to the S vectors are equally used. With respect to Fig. 5 this is obtained if $T_{PPO} = T_{OON}$ and $T_{POO} = T_{ONN}$.

Using these restrictions and equation (8), a linear system is obtained:

$$\begin{cases} \tau_{pa}(k) - \tau_{na}(k) - \bar{C}_0(k) = \frac{2T}{E} v^*_{an}(k) \\ \tau_{pb}(k) - \tau_{nb}(k) - \bar{C}_0(k) = \frac{2T}{E} v^*_{bn}(k) \\ \tau_{pc}(k) - \tau_{nc}(k) - \bar{C}_0(k) = \frac{2T}{E} v^*_{cn}(k) \\ \tau_{pa}(k) - \tau_{pb}(k) - \tau_{nb}(k) + \tau_{na}(k) = 0 \\ \tau_{pb}(k) - \tau_{pc}(k) - \tau_{nc}(k) + \tau_{nb}(k) = 0 \\ 2\tau_{pc}(k) + \tau_{pa}(k) + \tau_{nc}(k) = T \\ 2\tau_{na}(k) + \tau_{pa}(k) + \tau_{nc}(k) = T \end{cases} \tag{9}$$

Solving this system gives the pulse widths that define the control signals in Fig. 5 provided that the reference voltage vectors remain inside the subregion A1. The solution is given by:

$$\begin{cases} \tau_{pa}(k) = \frac{T}{4} + \frac{T}{2E}(v^*_{an}(k) - v^*_{cn}(k)) \\ \tau_{na}(k) = \frac{T}{4} - \frac{T}{2E}(v^*_{an}(k) - v^*_{cn}(k)) \\ \tau_{pb}(k) = \frac{T}{4} + \frac{3T}{2E} v^*_{bn}(k) \\ \tau_{nb}(k) = \frac{T}{4} - \frac{3T}{2E} v^*_{bn}(k) \\ \tau_{pc}(k) = \tau_{na}(k) \\ \tau_{nc}(k) = \tau_{pa}(k) \end{cases} \tag{10}$$

and $\tau_{ox}(k)$ is calculated by:

$$\tau_{ox}(k) = T - \tau_{px}(k) - \tau_{nx}(k) \tag{11}$$

A similar procedure can be employed to determine the pulse widths for the subregions A2 to A4.

C. Minimum on/off time

In the previous analysis the inverter switches were assumed to be ideal. However, in multilevel converters the minimum on/off time must be considered to avoid turn-on or turn-off failures, specially with GTO devices. Moreover, if the minimun on/off time is not took in to account in the modulation method, there will exist unrealizable regions in the hexagon of Fig. 3 that will distort the output voltage waveforms. In this section the PWM solution presented in the previous section is modified to take into account these limitations.

The on/off time restrictions can be expressed by:

$$\begin{aligned} &\tau_{px}(k) \geq T_{min} \\ &\tau_{nx}(k) \geq T_{min} \\ &\tau_{px}(k) + \tau_{nx}(k) \leq T - T_{min} \end{aligned} \tag{12}$$

where T_{min} is the minimum conduction time for any switch of the inverter. With these restrictions and equation (10)the unrealizable regions can be determined. These regions are shown by the shaded areas in Fig. 6.

The use of complete switching patterns has the advantage of maximizing the number of commutations in the output phase voltage waveform reducing its harmonic content. However, complete switching patterns generates very narrow control pulses that may violate the restrictions expressed in (12). To avoid this problem the sector A has been divided into fifteen subregions as shown in Fig. 7. In the subregions numbered from 1 to 4, complete patterns are used and in the other subregions, reduced patterns, obtained by eliminating some

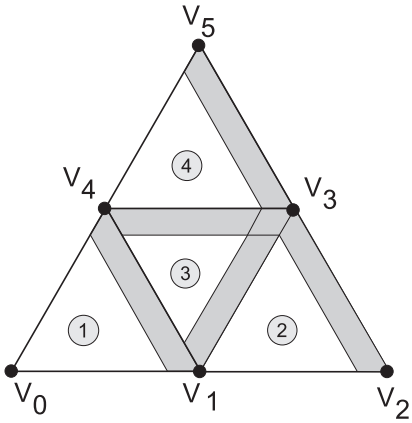

Fig. 6. Unrealizable regions for the three-level inverter considering the minimum on/off time

of the switching states of the complete patterns, are employed. The shaded region shown in Fig. 7 corresponds to the unrealizable voltage vectors in this case. As an example, the reduced patterns for the subregion A5 is /PPO/POO/OOO/OON/ONN/ and the corresponding solution is given by:

$$\begin{cases} \tau_{pa}(k) = \tau_{nc}(k) = \frac{T}{E}(v^*_{an}(k) - v^*_{cn}(k)) \\ \tau_{pb}(k) = \frac{T}{E}(v^*_{bn}(k) - v^*_{cn}(k)) \\ \tau_{nb}(k) = \frac{T}{E}(v^*_{an}(k) - v^*_{bn}(k)) \\ \tau_{na}(k) = \tau_{pc}(k) = 0 \end{cases} \tag{13}$$

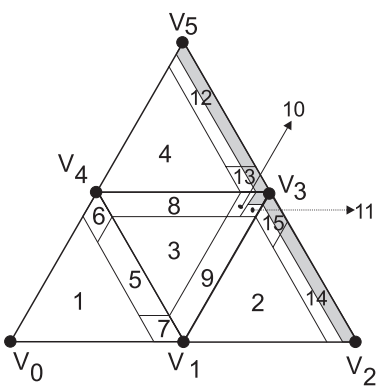

Fig. 7. Sector A regions considering the minimum on/off time

The reduced patterns for the other subregions and the corresponding solutions are omitted due to space limitations.

V. Generalizing the results

The determination of the pulse widths of the switch control signals when the reference voltage vector is inside the sector A has been considered in the previous section. In this section these results are extended to the others sectors of Fig. 3.

To determine the location of the reference voltage in the hexagon of Fig. 3 the reference phase voltages must be ordered. Table II shows the voltage ordering together with the respective vector locations.

TABLE II
Location of the reference voltage vector

Sector	Phase voltages order
A	$v^*_{an}(k) > v^*_{bn}(k) > v^*_{cn}(k)$
B	$v^*_{bn}(k) > v^*_{an}(k) > v^*_{cn}(k)$
C	$v^*_{bn}(k) > v^*_{cn}(k) > v^*_{an}(k)$
D	$v^*_{cn}(k) > v^*_{bn}(k) > v^*_{an}(k)$
E	$v^*_{cn}(k) > v^*_{an}(k) > v^*_{bn}(k)$
F	$v^*_{an}(k) > v^*_{cn}(k) > v^*_{bn}(k)$

After the ordering procedure the phase voltages are referred as $v^*_{1n}(k)$, $v^*_{2n}(k)$ and $v^*_{3n}(k)$, where $v^*_{1n}(k) > v^*_{2n}(k) > v^*_{3n}(k)$. The pulse widths are then calculated using the same expressions employed for sector A replacing $v^*_{an}(k)$, $v^*_{bn}(k)$, and $v^*_{cn}(k)$ by $v^*_{1n}(k)$, $v^*_{2n}(k)$ and $v^*_{3n}(k)$ respectively and similarly replacing τ_{pa}, τ_{pb}, τ_{pc}, τ_{na}, τ_{nb} and τ_{nc} by τ_{p1}, τ_{p2}, τ_{p3}, τ_{n1}, τ_{n2} and τ_{n3} respectively.

VI. Simulation results

The proposed PWM method was tested in simulation with a three-level inverter supplying a three-phase RL load. The DC-link voltage is $300V$ and parameters of the load are $R = 5\Omega$ and $L = 5.5mH$. The frequency of the reference voltage vector was $60Hz$ and the switching frequency equal to $720Hz$ corresponding to a frequency ratio of 12. The minimum ton/toff time, T_{min} was fixed to 10% of the switching period. Fig. 8 shows the amplitude of the fundamental component of the output voltage when the modulation index (m) varies from 0 to 1. The linearity is observed up to $m = 0.57$ as expected. Fig. 9 shows the total harmonic distortion calculated by:

$$SIG = \frac{\sqrt{\sum_{n=2}^{\infty} \frac{V_n^2}{n^2}}}{V_1} \tag{14}$$

Fig. 10 shows the output line-to-line voltage for $m = 0.4$ and Fig. 11 shows the corresponding current vector locus. Fig. 12 shows the voltage of the upper DC-link capacitor voltage.

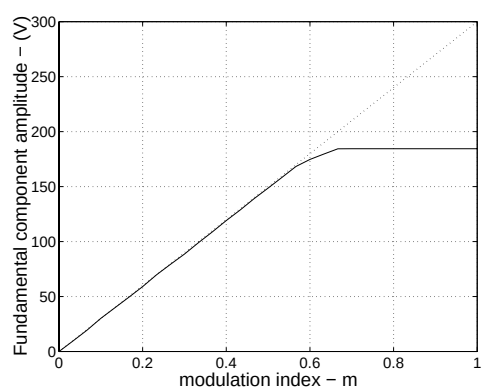

Fig. 8. Fundamental component amplitude x modulation index

The above results show that the proposed PWM technique has presented all the claimed features. The balanc-

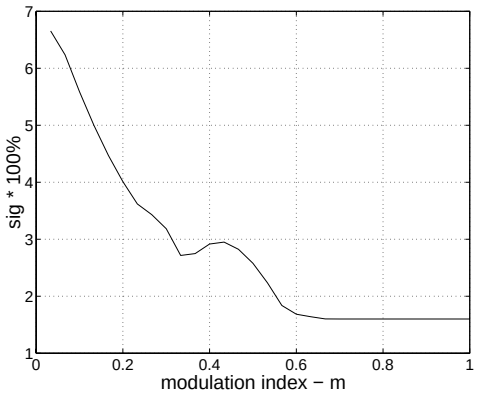

Fig. 9. SIG x modulation index

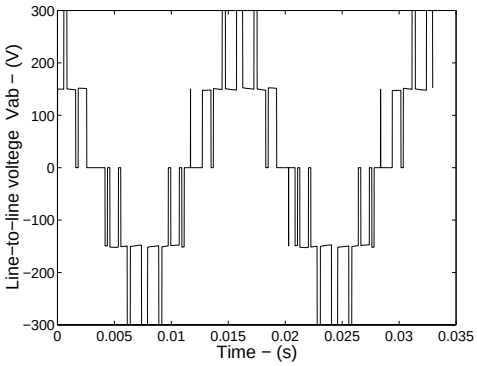

Fig. 10. Line-to-line voltage 100 V/div(f=60 Hz, m=0.4, q=12)

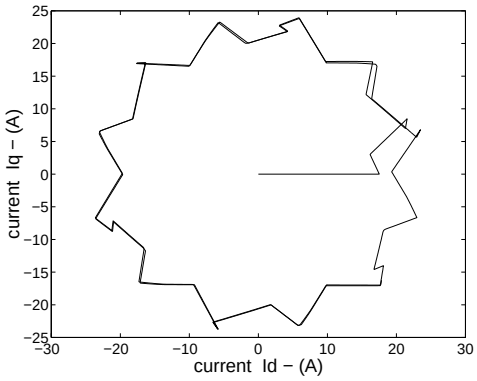

Fig. 11. I_q(5A/div) x I_d(5A/div) Current locus (charge: R=5 Ω L=5.5 mH)

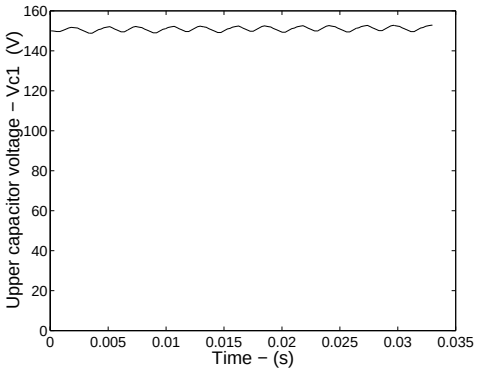

Fig. 12. Upper capacitor voltage - 20 V/div (E=300V)

ing of the DC-link capacitor voltages has been obtained and the distortion due to the on/off time restriction has been minimized.

VII. Conclusion

This paper has presented an elegant, simple and useful PWM technique for generating the control signals of the switches of a three-level inverter. The determination of pulse widths taking into account on/off time restrictions has been achieved via simple algebraic operations thus simplfying the practical implementation of the proposed modulator. The simulation results have demonstrated the validity of the proposed technique.

VIII. Acknowledgement

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