A NEW SOFT COMMUTATION PWM VOLTAGE SOURCE INVERTER

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***Abstract* – In this work a new topology of a pulse-width-modulation zero-voltage-switching voltage source inverter is presented. Besides operation with zero-voltage-switching for a wide load range, the novel topology has the feature of being modulated by any conventional pulse-width-modulation strategy employed in the hard-switching inverters. The maximum voltage applied in all switches is clamped and limited in a reduced value and it does not produce excessive current stress. Operation description, theoretical analysis, design example and experimental results are presented in the paper. The results obtained with the new inverter topology are compared with an Undeland Snubber aided inverter.**

I – INTRODUCTION

In the output of a voltage source inverter, excellent voltage and current waveforms are expected, and a non existing or a very reduced harmonic content is considered.

To achieve a very reduced or a non existing harmonic content and to reduce the audible noise in voltage source inverters it is desirable to operate at high switching frequencies.

However, when the switching frequency increases, the efficiency and reliability of the PWM converter deteriorate significantly. Some efforts have been made to reach this aim and various topologies were proposed to achieve soft switching in voltage source inverters [1, 2, 3, 4, 5, 6, 7].

A great contribution to this area is the Undeland Snubber [1]. It is a passive topology and it is not be able to regenerate the commutation energy directly.

The resonant pole inverter (RPI) [2] maybe was the first active soft switching inverter topology. This circuit provides zero voltage switching (ZVS) in all switches, but it has an excessive resonant current that also circulate in the load.

The rugged inverter (ARDPI) [3] combine the advantages of PWM strategy and soft switching techniques, but needs excessive resonant current to get soft commutation. The resonant current requires a minimum excess of twice the load current value.

The auxiliary resonant pole inverter topology (ARPI) [4] gives a good improvement regarding to this problem (theoretically). However it requires modification in the PWM strategy. In practice this topology needs the same level of resonant current that the ARDPI arrangement.

Another philosophy was proposed in the auxiliary resonant commutated pole inverter (ARCPI) [5, 6, 7]. In this topology the resonant pole is connected in parallel with the load. This type of circuit has a complex control strategy and the resonant current assumes large values that are reflected to the main switches increasing their current stress.

In this work a new topology is presented, which combines the goals of soft switching commutation in all active switches, high frequency capability, conventional PWM strategy and no excessive additional voltage or current stress.

II – CIRCUIT DESCRIPTION AND PRINCIPLE OF OPERATION

The new zero-voltage-switching pulse-width modulation voltage-source inverter with active voltage clamping (ZVS-PWM-VSI-AVC) topology was derived from the family of ZVS-PWM active-voltage-clamping DC to DC converters [7]. The proposed inverter is shown in Fig. 1 and consists of two main switches (*S2* and *S3*), two auxiliary switches (*S1* and *S4*), six diodes (*D1-D6*), six resonant capacitors (*Cr1-Cr6*), two resonant inductors (*Lr1* and *Lr2*) and two clamping capacitors (*Cg1* and *Cg2*), besides the DC bus and the load.

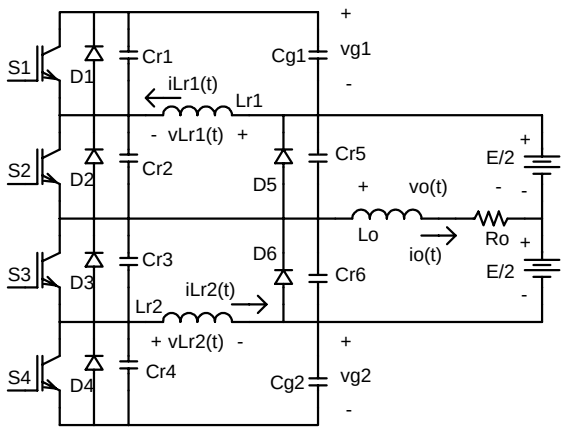

Figure 1 – The proposed ZVS-PWM voltage source inverter with active voltage clamping.

The novel soft commutation inverter presents nine stages of operation, explained as follows:

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First Stage (t_0, t_1): in this stage the main switch *S2* is conducting. The current through *Lr1* is equal to the load current and the current through *Lr2* is equal to zero. During this stage energy is transferred to the load.

Second Stage (t_1, t_2): at the instant *t=t1*, switch *S2* is turned-off and the resonant capacitors *Cr2* and *Cr5* are linearly charged. The voltage across *Cr1* varies from *zero* to *E+vg1* and the voltage across *Cr5* varies from *zero* to *E*. The resonant capacitors *Cr1* and *Cr6* are discharged and the voltages across their terminals vary from *E+vg1* and *E* to *zero*, respectively. The resonant current *iLr1* remains constant and equal to the load current.

Third Stage (t_2, t_3): when the voltage across *Cr2* equals $E+v_{g1}$ the voltage across *Cr1* becomes null, and diode *D1* starts to conduct. Simultaneously the voltage across *Cr5* becomes equal to *E* and the voltage across *Cr6* becomes null, and diode *D6* starts to conduct the load current. The inductor *Lr1* demagnetises through the clamping capacitor *Cg1* via *D1*. During this stage switch *S1* must be gated on, so that in the next stage soft commutation is achieved.

Fourth Stage (t_3, t_4): when i_{Lr1} becomes zero, diode *D1* is blocked and switch *S1* starts to conduct without commutation losses. Current i_{Lr1} changes its direction and increases linearly in a negative sense.

Fifth Stage (t_4, t_5): at the instant *t=t4*, the switch *S1* is blocked. Capacitor *Cr1* is charged and capacitor *Cr2* is discharged in linear fashion, while the current through *Lr1* remains constant and equal to the load current. The voltage across *Cr1* increases from *zero* to $E+v_{g1}$, while the voltage across *Cr2* decreases from $E+v_{g1}$ to *zero*.

Sixth Stage (t_5, t_6): when v_{Cr2} becomes equal to zero, diode *D2* starts to conduct the current i_{Lr1}. In this stage *Lr1* is demagnetized through *E* and its energy is recovered.

Seventh Stage (t_6, t_7): at the instant *t=t6* the current through *Lr1* becomes null and diode *D2* is blocked. Switch *S2* starts to conduct without commutation losses. The current through *Lr1* increases sharply, fed by *E* via *S2* and *D6*.

Eighth Stage (t_7, t_8): when i_{Lr1} becomes equal to the load current, the current in diode *D6* becomes null, blocking it. A resonance involving *Lr1*, *Cr1*, *Cr3*, *Cr5* and *Cr6* begins. The current through *Lr1* increases in sinusoidal fashion. The voltages across *Cr1* and *Cr5* decrease from $E+v_{g1}$ to v_{g1} and from *E* to *zero*, respectively, and the voltages across *Cr3* and *Cr6* increase from *zero* to *E*.

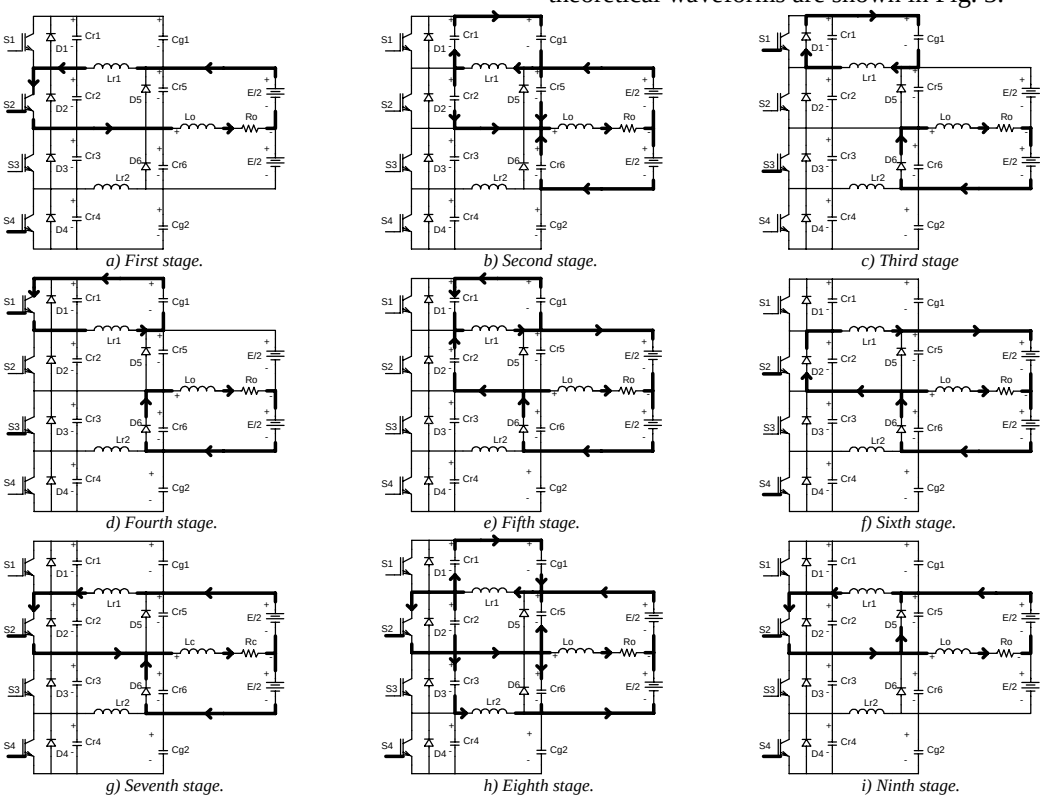
$$i_{Lr1}(t) = i_o(t) + \frac{E}{Zn} sin(w_o t) \qquad (1)$$

Where: $Zn = \sqrt{\frac{Lr}{4Cr}}$ and $w_o = \frac{1}{\sqrt{4LrCr}}$

$$Lr = Lr1 = Lr2 \text{ and } Cr = Cr1 = ... = Cr6$$

Ninth Stage (t_8, t_9): when the voltage across *Cr6* equals *E*, the voltage across *Cr5* becomes null and diode *D5* starts to conduct. The current through *Lr1* decreases as a consequence of the resistive elements present in the loop formed by *S2*, *Lr1* and *D5*. When the current through *Lr1* becomes equal to the load current, the first stage of operation restarts and one switching period is completed.

The topological stages in one period of commutation are shown in Fig. 2, and the main theoretical waveforms are shown in Fig. 3.



a) First stage. *b) Second stage.* *c) Third stage*

d) Fourth stage. *e) Fifth stage.* *f) Sixth stage.*

g) Seventh stage. *h) Eighth stage.* *i) Ninth stage.*

Figure 2 – Topological stages in one switching period.

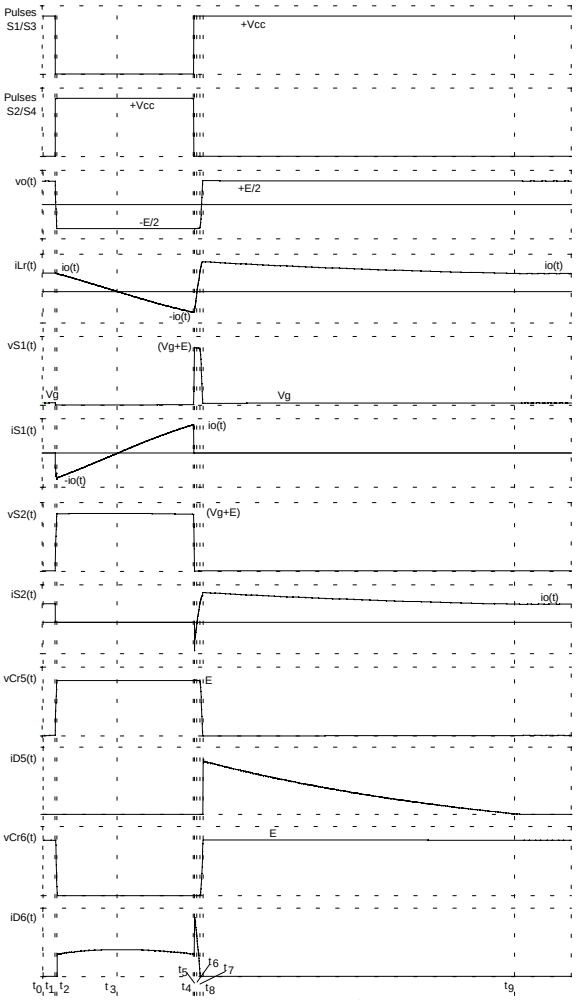


Figure 3 – The main theoretical waveforms in one switching period.

III – THE CLAMPING ACTION

The normalized clamped voltage $\overline{v_{g1}(t)}$ is expressed by (2). The normalized maximum clamped voltage is given by (3) and it is represented graphically by Fig. 4.

$$\overline{v_{g1}(t)} = \frac{v_{g1}(t)}{E} = \frac{ma\,sin(wt)}{\gamma\,\pi\;fn\left[1 - ma\,sin(wt)\right]} \qquad (2)$$

$$\overline{v_{g1_{max}}} = \frac{v_{g1_{max}}}{E} = \frac{ma}{\gamma\,\pi\;fn\left(1 - ma\right)} \qquad (3)$$

Where: ma is the amplitude modulation ratio

$$\gamma = \frac{Zo}{Zn}$$

$$fn = \frac{fo}{fs}$$

The maximum active switches voltage is the sum of the DC bus voltage and the maximum clamped voltage. The clamped voltage can be easily controlled by an appropriate combination of resonant parameters (*Cr* and *Lr*). The resonant parameters also control the soft commutation range.

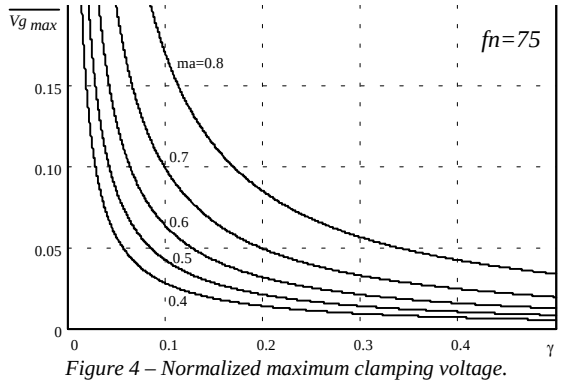


Figure 4 – Normalized maximum clamping voltage.

IV – COMMUTATION ANALYSIS

Soft commutation is achieved when the following expression is satisfied. The regions for soft commutation are graphically represented by Fig. 5.

$$wt \geq asin\left(\frac{2\gamma}{ma} + \frac{2}{\pi\;fn(1 - ma)}\right) \qquad (4)$$

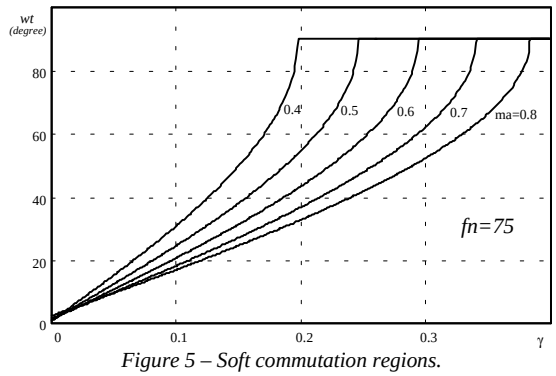


Figure 5 – Soft commutation regions.

V – DESIGN PROCEDURE

A 2.5kVA ZVS-PWM-VSI with active voltage clamping was designed to drive an induction motor with the following characteristics:

$Vo_{rms} = 120V$; $Io_{rms} = 20.8A$; $fo = 60Hz$;

$Io_{max} = 29.5A$; $ma = 0.773$; $cos\varphi = 0.95$;

$Lo = 4{,}77mH$; $Ro = 5.4\Omega$; $Zo_{60Hz} = 5.76\Omega$.

The DC bus has a medium point and its total voltage is equal to $E = 440V$.

Choosing $fn = 75$ and the soft commutation range between 20° and 160° and with the aid of Fig. 5, $\gamma = 0.1175$ is obtained. Hence:

$$Zn = \sqrt{\frac{Lr}{4\,Cr}} = \frac{Zo}{\gamma} = 49.02\Omega$$

$fs = 7.8kHz$ *(switching frequency)*

$fr = fs\;fn = 585kHz$ *(resonant frequency)*

$$Lr = \frac{Zn}{2\,\pi\;fr} = 13.3\mu H$$

$$Cr = \frac{Lr}{2\,Zn^2} = 1.5nF$$

$$Cg = \frac{1}{4\pi^2\ Lr\ fs^2} = 35\mu F \quad (clamping\ capacitor)$$

VI – EXPERIMENTAL RESULTS

A prototype of a 2.5kVA zero-voltage-switching pulse-width-modulated voltage-source inverter with active voltage clamping (ZVS-PWM-VSI-AVC) has been built, using the scheme shown in Fig. 6 and the values calculated in the previous section.

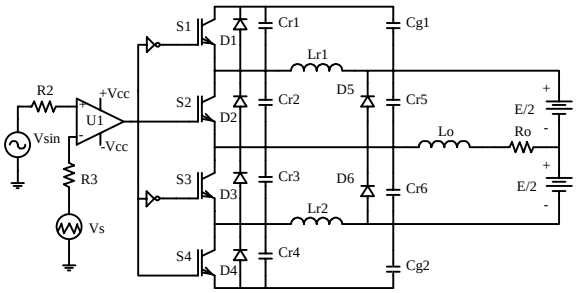


Figure 6 – The experimented inverter.

The inverter is operated under conventional sinusoidal pulse-width modulation. The relevant devices specifications are given below.

$S1 - S4 = SKM\,50GB123D$ - Semikron

$D5 - D6 = HFA15TB60$ - International Rectifier

$Lf = 1.8mH$ (output inductor filter)

$Cf = 22\mu F$ (output capacitor filter).

The following figures show the experimental results for full load condition.

Fig. 7 shows the voltage across and the current through the load.

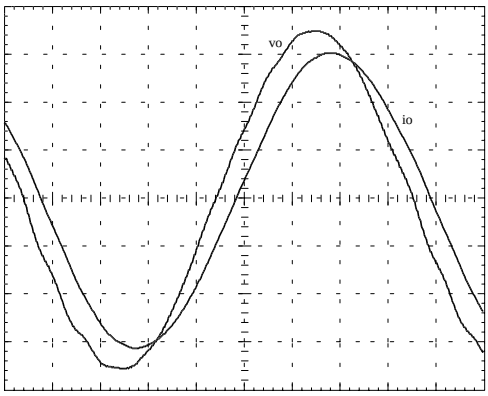


Figure 7 – Voltage across and current through the load (50V/div; 10A/div; 2ms/div).

The clamping voltages across *Cg1* and *Cg2* are shown in Fig. 8. They are limited to 40V.

The resonant current through *Lr1* is shown in Fig. 9 for one load period and in Fig. 10 for one switching period. The maximum value of the resonant current is 40A.

Fig. 11 shows the resonant current through *Lr2* for one load period and Fig. 12 shows the same current for one switching period.

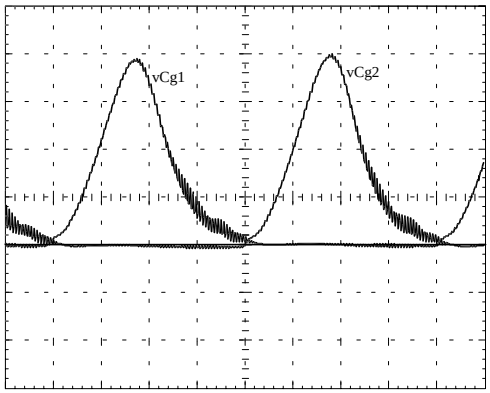


Figure 7 – Clamped voltages in Cg1 and Cg2 (10V/div; 2ms/div).

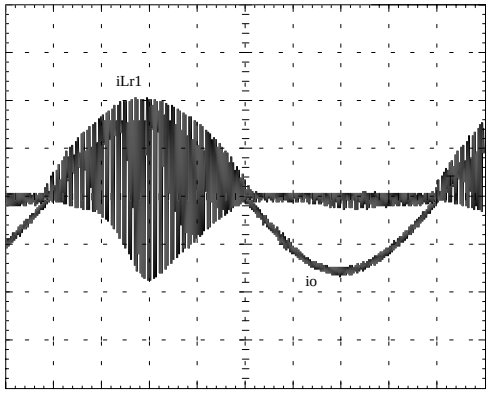


Figure 9 – Current through Lr1 superposed with the load current (20A/div; 2ms/div).

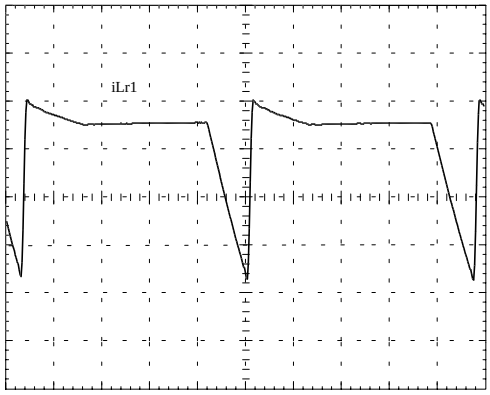


Figure 10 – Detail of Lr1 current during one switching period (20A/div; 25µs/div).

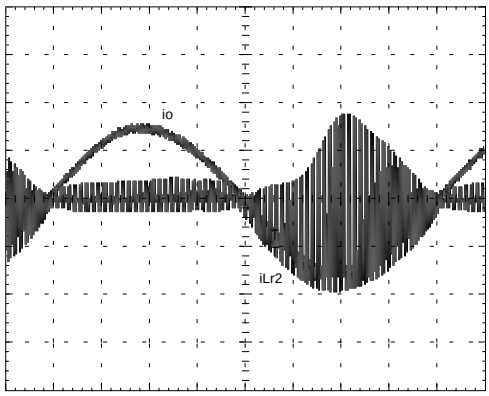


Figure 11 – Current through Lr1 superposed with the load current (20A/div; 2ms/div).

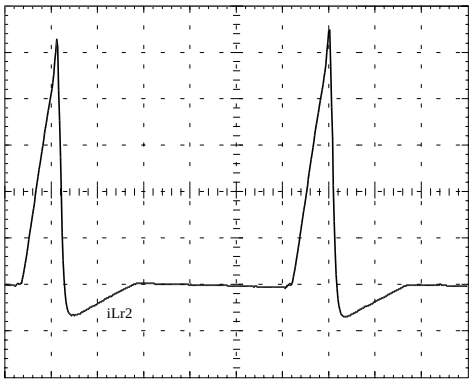


Figure 12 – Detail of Lr1 current during one switching period (10A/div; 20µs/div).

Fig. 13 shows the voltage across *S1* and the current through this switch.

In Fig. 14 it is shown voltage across and current through the main switch *S2*.

A detail of the turn-on process in the main switch is shown in Fig. 15. This figure proves that the turn-on process of *S2* is entirely lossless.

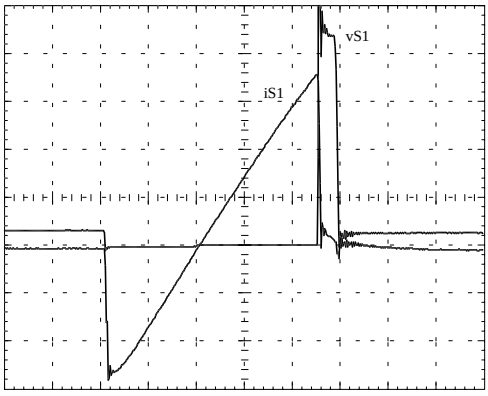


Figure 13 – Voltage across and current through the auxiliary switch S1 (100V/div; 10A/div; 5µs/div).

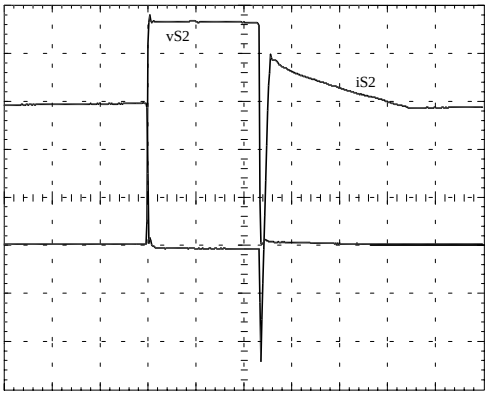


Figure 14 – Voltage across and current through the main switch S2 (100V/div; 10 A/div; 10µs/div).

In Fig. 16 a detail of turn-off process in the main switch *S2* is shown. The pronounced tail current of the IGBT produces an additional power loss that can be avoided by choosing a better switch, e.g. the fourth generation IGBTs.

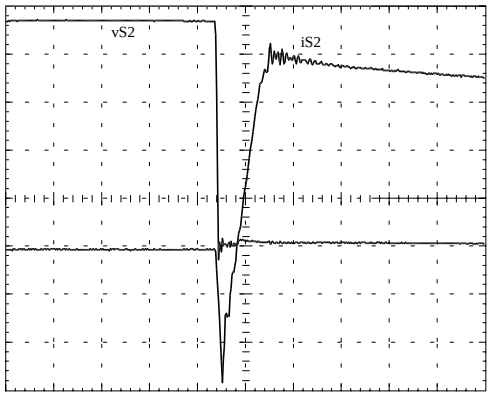


Figure 15 – Detail of the main switch S2 turn-on process (100V/div; 10 A/div; 2µs/div).

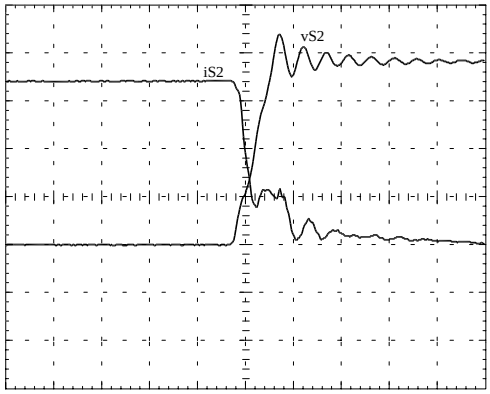


Figure 16 – Detail of the main switch S2 turn-off process (100V/div; 10 A/div; 200ns/div).

Fig. 17 shows the efficiency of the new inverter. At full load condition the measured efficiency was 96.9%.

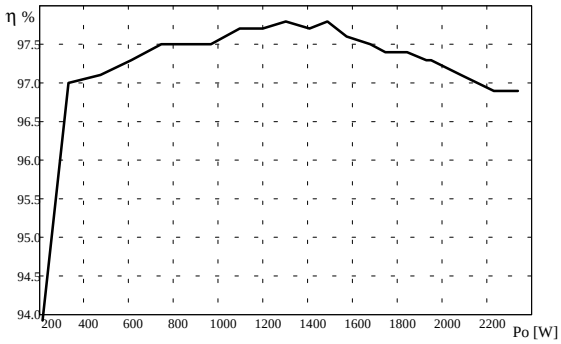


Figure 17 – Efficiency of the new inverter.

VII – Comparison with the Undeland Snubber

In order to compare the results obtained with the new soft commutation inverter another inverter using the Undeland Snubber with the same characteristics depicted in section V has been implemented.

The inverter with the Undeland Snubber applied in this case is shown in Fig. 18 and the principal components used are given bellow.

$Ls = 2.8\mu H$; $Cs = 4.1nF$

$Rg = 50$; $Cg = 40\mu F$

$S_1 - S_2 = SKM\,50GB123D$ - *Semikron*

$Ds = MUR460$ - *Motorola*

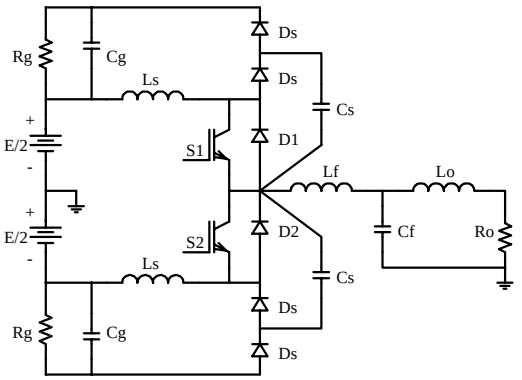


Figure 18 – Half-bridge inverter with the Undeland Snubber.

Fig. 19 shows the turn-on process of switch *S1*.

In Fig. 20 a detail of the switch *S1* turn-off process is shown. It can be seen in this figure that there is a pronounced IGBT tail current.

Fig. 21 shows the efficiency of the half-bridge inverter with the Undeland Snubber.

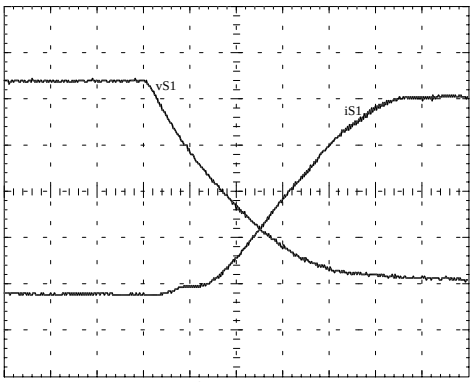


Figure 19 – Detail of the switch S1 turn-on process (100V/div; 10 A/div; 50ns/div).

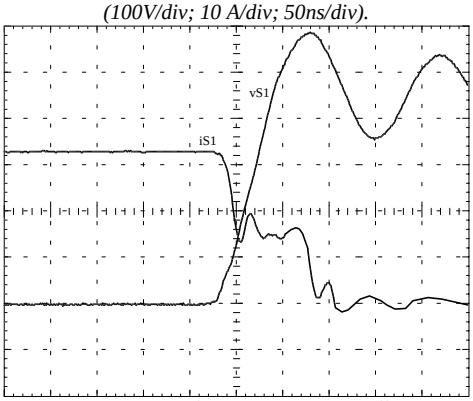


Figure 20 – Detail of the switch S1 turn-off process (100V/div; 10 A/div; 200ns/div).

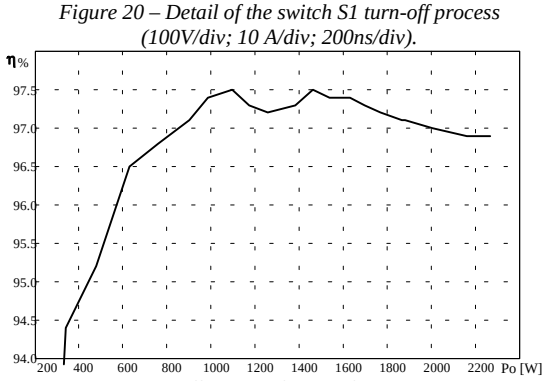


Figure 21 – Efficiency of the half-bridge inverter aided by the Undeland Snubber.

In the previous picture it can be seen that the results are equivalent compared with the new inverter proposed. In this case the inverter aided by the Undeland Snubber was favored because the switching frequency is low and the commutation losses are not very significant. When the switching frequency becomes higher the commutation loss also becomes higher and a passive solution, such as the Undeland Snubber, would be a bad choice.

In order to make a better comparison a new design using a higher switching frequency has been done.

VIII – CONCLUSION

In this paper a new soft commutation PWM voltage-source inverter was presented and analyzed. This new topology combines the advantages of a soft commutated converter using the zero-voltage-switching technique in a wide range of load current and those of a conventional pulse-width modulation. The transistor voltage stress can be limited as close as necessary from the DC bus voltage and the maximum value of resonant current also can be controlled by the resonant parameters. The new inverter has the additional advantages of integrating all of the major parasitic components and easing the implementation with power modules. Experimental results show that the new proposed inverter reduces the losses of the IGBT by allowing zero voltage condition during the turn-on and turn-off process. The efficiency at full load condition is 96.9%. A comparison between the inverter aided by the Undeland Snubber with the new topology proves that both converters presented equivalent performances.

VIII – REFERENCES

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