A FAMILY OF ZVS-PWM ACTIVE CLAMPING DC-TO-DC CONVERTERS FEATURING SOFT COMMUTATION IN BOTH ACTIVE AND PASSIVE SWITCHES

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***Abstract* - A new family of DC-to-DC converters featuring clamping action, PWM modulation and soft-switching (ZVS) in both active and passive switches, is proposed to overcome the limitations of Clamped Mode DC-to-DC converters. The new family of converters is generated and the new circuits are presented. As the resonant circuits absorb all parasitic reactances, including transistor output capacitance and diode junction capacitance, these converters are suitable for high-frequency operation.**

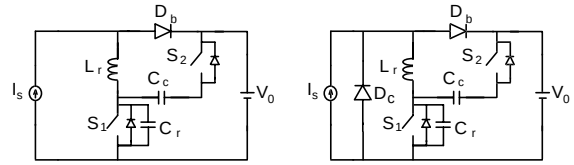
Principle of operation, theoretical analysis, simulation and experimental results are presented, taken from a laboratory prototype rated at 1600W, input voltage of 300V, output voltage of 400V, and operating at 100kHz. The measured efficiency at full load was 98%.

I. INTRODUCTION

The objective of high frequency operation in dc-dc converters is the reduction of reactive components size and cost. As in any power application, high efficiency is essential, and hence the increasing of frequency can be problematic because of the direct dependence of switching losses on frequency. The use of soft-switching techniques, ZVS and ZCS, is an attempt to substantially reduce switching losses, and hence attain high efficiency at increased frequency.

Different techniques has been proposed to operate dc-dc converters in high frequency. The Active Clamping technique [1] has the advantages of PWM modulation, soft-commutation (ZVS) on main switches and low voltage stresses due to the clamping action. Besides operating at constant frequency and with reduced commutation losses there is no significant increasing on circulating reactive energy that would cause large conduction losses.

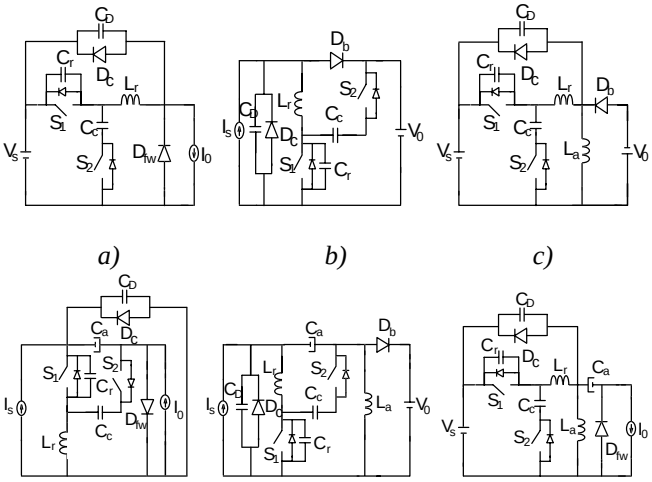
The parasitic ringings caused by the interaction of the junction capacitance of the rectifier, in the clamped mode Boost converter (Fig. 1.a) [2], and the resonant inductor are eliminated by the inclusion of an auxiliary clamping diode [3], as shown in Fig 1.b, limiting the voltage stress on the rectifier to the output voltage. Although the voltage stress on the rectifier has been eliminated, both D_b and D_c diodes still present hard switching commutation and the voltages across these devices still rise in a high dv/dt rate, which means compatibility electromagnetic problems and switching losses.



a) *b)*

Fig. 1. Clamped mode converters: a) without diode D_c; b) with diode D_c.

This paper presents an improved family of dc-dc converters featuring clamping action, PWM modulation and soft-switching (ZVS) in both active and passive switches. The inclusion of capacitor C_D and clamping diode D_c, in the Boost converter, as shown in Fig. 2.b, results in reduced voltage dv/dt and soft-switching conditions for all switching devices, including diodes D_c and D_b. Therefore all parasitic reactances are absorbed, including transistor output capacitance and diode junction capacitance, resulting in high efficiency at high frequency operation without significant increasing in voltage and current stresses on switches.



a) *b)* *c)*

d) *e)* *f)*

Fig. 2. The new family of converters: - a) Buck; - b) Boost; - c) Buck-boost; - d) Cuk; - e) Sepic; f) Zeta.

This technique is extended to all basic dc-dc converters as shown in Fig. 2.

II. OPERATION AND ANALYSIS OF THE BOOST CONVERTER

To simplify the analysis, the input filter inductance is assumed large enough to be considered as a current source (I_s). The capacitor C_c is selected to have a large capacitance so that the voltage V_c across the capacitor C_c could be considered as a constant one. The eight topological stages and key waveforms of the proposed Boost converter, to one switching cycle, are shown in Fig. 3 and 4 respectively. From Fig. 3 and 4 it can be seen that the two switches are switched in a complementary way and soft-switching is achieved for all switches and diodes. The main switch S_1 is turned off at $t=t_0$, when the switching cycle starts.

Stage 1 [t_0, t_1]; resonant stage, Fig. 3.a.

Prior to t_0, the main switch S_1 is on, the auxiliary switch is off and the clamping diode D_c is conducting. When S_1 is turned off, at $t=t_0$, the first resonant stage has started, as shown in Fig. 3.a. The capacitor C_r is charged in a resonant way. When $v_{Cr}(t)$ reaches V_c+V_0, the antiparallel diode of S_1 starts conducting and this stage ends with voltage $v_{Cr}(t)$ clamped at V_c+V_0.

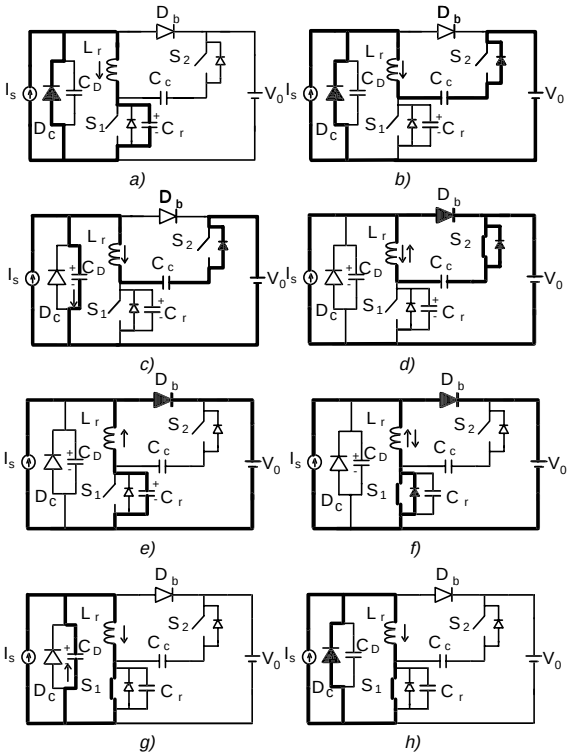


Fig. 3. Topological stages of Boost converter

This stage is described by:

$$i_{Lr}(t) = I_{L0}\cos\omega_1 t \quad (01)$$

$$v_{CD}(t) = 0 \quad (02)$$

$$v_{Cr}(t) = \sqrt{\frac{L_r}{C_r}} I_{L0}\sin\omega_1 t \quad (03)$$

where,

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}} \quad (04)$$

$$\omega_1 \Delta t_1 = \sin^{-1}\left[\frac{(V_0 + V_c)}{I_{L0}\sqrt{L_r / C_r}}\right] \quad (05)$$

$$I_{L1} = \sqrt{I_{L0}^2 - \frac{(V_0 + V_c)^2}{L_r / C_r}} \quad (06)$$

Stage 2 [t_1, t_2]; linear stage, Fig. 3.b.

In this stage, the L_r current ramps down until reaches I_s, when the clamping diode D_c becomes reversibly biased and diode D_b starts conducting.

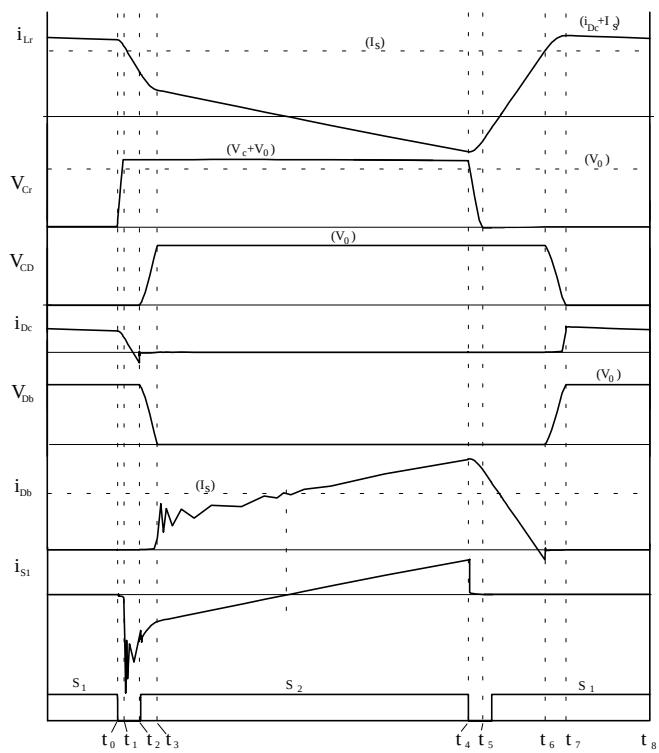


Fig. 4. Theoretical waveforms of Boost converter.

The equations to this stage are:

$$i_{Lr}(t) = -\frac{(V_c - V_0)}{L_r} t + I_{L1} \quad (07)$$

$$v_{CD}(t) = 0 \quad (08)$$

$$v_{Cr}(t) = (V_0 + V_c) \quad (09)$$

and,

$$\Delta t_2 = \frac{(I_{L1} - I_s)}{(V_c + V_0)} L_r \quad (10)$$

$$I_{L2} = I_s \quad (11)$$

Stage 3 [t_2, t_3]; resonant stage, Fig. 3.c.

When the clamping diode D_c ends conducting, the current through L_r decreases and the capacitor C_D is charged in a resonant way. When $v_{CD}(t)$ reaches V_0, the diode D_b becomes forward biased and starts conducting.
The equations that describe this stage are:

$$i_{Lr}(t) = I_s - \frac{(V_c + V_0)}{\sqrt{L_r / C_D}} \sin\omega_2 t \quad (12)$$

$$v_{CD}(t) = (V_c + V_0)(1 - \cos\omega_2 t) \quad (13)$$

$$v_{Cr}(t) = (V_c + V_0) \quad (14)$$

where,

$$\omega_2 = \frac{1}{\sqrt{L_r C_D}} \quad (15)$$

$$\omega_2 \Delta t_3 = \cos^{-1}\left[\frac{V_c}{V_c + V_0}\right] \quad (16)$$

$$I_{L3} = I_s - \frac{V_0\sqrt{1 + 2V_c / V_0}}{\sqrt{L_r / C_D}} \quad (17)$$

Stage 4 [t_3, t_4]; linear stage, Fig. 3.d.

The L_r current ramps down, because C_c is considered as a constant voltage source, until it reaches zero, when it changes its direction and rises again. When the antiparallel diode of S_2 is conducting, the auxiliary switch S_2 should be switched on to achieve a loss-less turn-on. This stage ends when S_2 is turned off at $t=t_4$.
This stage is described by:

$$i_{Lr}(t) = -\frac{V_0}{L_r} t + I_{L3} \quad (18)$$

$$v_{CD}(t) = 0 \quad (19)$$

$$v_{Cr}(t) = (V_0 + V_c) \quad (20)$$

and,

$$\Delta t_4 = (1 - D)T_s - (\Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_5) \quad (21)$$

$$I_{L4} = -\frac{V_c}{L_r}\Delta t_4 + I_{L3} \quad (22)$$

Stage 5 [t_4, t_5]; resonant stage, Fig. 3.e.

The voltage across C_r falls, due to the resonance between L_r and C_r, until it reaches zero at $t=t_4$. This stage ends when $v_{Cr}(t)$ becomes null and the antiparallel diode of S_1 begins conducting.

$$i_{Lr}(t) = -\frac{V_c}{\sqrt{L_r / C_r}} \sin\omega_1 t - I_{L4}\cos\omega_1 t \quad (23)$$

$$v_{CD}(t) = V_0 \quad (24)$$

$$v_{Cr}(t) = V_0 + V_c\cos\omega_1 t - \sqrt{\frac{L_r}{C_r}} I_{L4}\sin\omega_1 t \quad (25)$$

where,

$$\omega_1 \Delta t_5 = \cos^{-1}\left[\frac{V_0 V_c + \sqrt{(I_{L4}^2 L_r / C_r)(V_c^2 - V_0^2 + I_{L4}^2 L_r / C_r)}}{(V_c^2 + I_{L4}^2 L_r / C_r)}\right] \quad (26)$$

$$I_{L5} = -\frac{V_c}{\sqrt{L_r / C_r}}\sqrt{1 - \cos^2\omega_1 \Delta t_5} - I_{L4}\cos\omega_1 \Delta t_5 \quad (27)$$

Stage 6 [t_5, t_6]; resonant stage, Fig. 3.f.

In stage 6, S_1 is turned on without switching losses, in a ZVS way, because $v_{Cr}(t)$ became null. The current through L_r changes its polarity and ramps up to reach I_S at $t=t_6$. Then the diode D_b becomes reversibly biased and turns off.
The equations are:

$$i_{Lr}(t) = \frac{V_0}{L_r} t + I_{L5} \quad (28)$$

$$v_{CD}(t) = V_0 \quad (29)$$

$$v_{Cr}(t) = 0 \quad (30)$$

and,

$$\Delta t_6 = \frac{(I_s - I_{L5})}{V_0} L_r \quad (31)$$

$$I_{L6} = I_s \quad (32)$$

Stage 7 [t_6, t_7]; resonant stage, Fig. 3.g.

When diode D_b is turned off, capacitor C_D and inductor L_r begins resonate. The voltage across C_D reduces to zero and current through L_r rises. This stage ends when voltage across C_D becomes null and the clamping diode D_c becomes forward biased.

$$i_{Lr}(t) = \frac{V_0}{\sqrt{L_r / C_D}} \sin\omega_2 t + I_s\cos\omega_2 t \quad (33)$$

$$v_{CD}(t) = V_0\cos\omega_2 t - \sqrt{L_r / C_D} I_s \sin\omega_2 t \quad (34)$$

$$v_{Cr}(t) = 0 \quad (35)$$

where,

$$\omega_2 \Delta t_7 = tg^{-1}\left[\frac{V_0}{I_s\sqrt{L_r C_D}}\right] \quad (36)$$

$$I_{L7} = I_{L0} = I_s\sqrt{(V_0^2 C_D / L_r I_s^2) + 1} \quad (37)$$

Stage 8 [t_7, t_8]; resonant stage, Fig. 3.h.

At $t=t_7$, the diode D_c is conducting and the current through L_r is clamped at I_s+I_{Dc}. The diode D_b is reversibly biased and power is not transferred to the load. This stage ends when S_1 is turned off at the end of the switching cycle.

$$i_{Lr}(t) = I_{L7} = I_{L0} \quad (38)$$

$$v_{CD}(t) = 0 \quad (39)$$

$$v_{Cr}(t) = 0 \quad (40)$$

and,

$$\Delta t_8 = DT_s - (\Delta t_7 + \Delta t_6) \quad (41)$$

$$I_{L8} = I_{L0} \quad (42)$$

III. CURRENT THROUGH DIODE D_C

The exceeding storage energy in L_r (responsible by the increasing of its current beyond I_s) is equal to storage energy in capacitor C_D during one operation cycle, because during stage 7, C_D transfers its whole energy to L_r, resulting

in decreasing of input voltage from V_s to zero and increasing of I_{Lr} from I_s to I_s+I_{Dc}. Therefore, we have:

$$E_{CD}(t_6) = \frac{1}{2} C_D V_0^2 = \frac{1}{2} L_r I_{Dc}^2 \tag{43}$$

$$I_{Dc} = \frac{V_0}{Z_{02}} \tag{44}$$

where:

$$Z_{02} = \sqrt{\frac{L_r}{C_D}} \tag{45}$$

Thus, from equation (44), it can be noted that the peak value of current through D_c depends directly on C_D. Therefore, as greater is C_D greater will be this current and peak current through main switch S_1.

IV. DC VOLTAGE CONVERSION RATIO AND DC VOLTAGE CLAMPING RATIO

As we can see from the waveforms of Fig. 4 and mathematical expressions from section II, the behavior of this new boost converter is quite different respect to boost-buck-boost converter presented in [2]. However, using suitable approximations, it is possible to derive useful relations which can greatly simplify the design procedure.

Thus, considering that the duration of intervals (t_1,t_2) and (t_4,t_5) are very small compared to switching cycle, as can be seen from Fig. 5, from the current balance on C_c we have:

$$\int_0^{\Delta t_2}\left[-\frac{(V_c - V_0)}{L_r}t + I_{L1}\right]dt + \int_0^{\Delta t_3}\left[I_s - \frac{(V_c + V_0)}{Z_{02}}\sin\omega_2 t\right]dt + \int_0^{\Delta t_4}\left[-\frac{V_c}{L_r}t + I_{L3}\right]dt = 0 \tag{46}$$

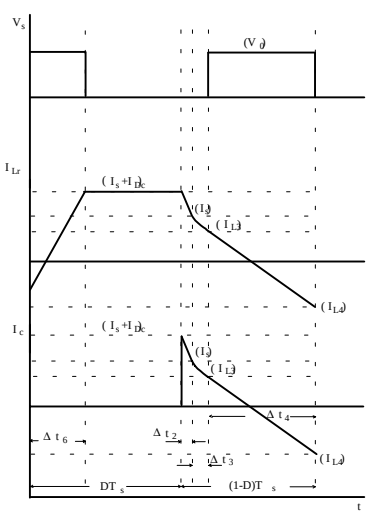


Fig. 5 - Main simplified waveforms.

By assuming $I_{L1}=(I_s+I_{Dc})$ and

$$\Delta t_4 = (1-D)T_s - \frac{1}{\omega_2}\cos^{-1}\left(\frac{\beta}{1+\beta}\right) - 2\delta \tag{47}$$

where δ represents the dead time and $\beta=V_c/V_0$, and solving equation (46), we have:

$$I_{0n} = \frac{1}{\omega_2 T_s}\left[\frac{1+\frac{\beta}{2}(\omega_2\Delta t_4)^2 + \sqrt{1+2\beta}\,\omega_2\Delta t_4}{\frac{1}{(1+\beta)} + \cos^{-1}\left(\frac{\beta}{1+\beta}\right) + \omega_2\Delta t_4}\right] \tag{48}$$

where:

$$\Delta t_2 = \frac{1}{\omega_2}\frac{V_0}{(V_0+V_c)} = \frac{1}{\omega_2 T_s}\frac{\beta}{(1+\beta)} \tag{49}$$

$$\Delta t_3 = \frac{1}{\omega_2}\cos^{-1}\left(\frac{\beta}{1+\beta}\right) \tag{50}$$

$$I_{L4n} = -\frac{\beta}{T_s}\Delta t_4 + I_{L3} \tag{51}$$

$$I_{0n} = I_{sn} = \frac{L_r I_s}{V_0 T_s} = \frac{L_r I_0}{V_s T_s} \tag{52}$$

As the average current through inductor L_r must be null in one switching cycle, we have:

$$V_0 + V_c = V_s + V_{S2} \tag{53}$$

and, as the average voltage across S_2 is:

$$V_{S2} = D(V_0 + V_c) \tag{54}$$

therefore, equating (53) with (54) gives:

$$q = \frac{V_0}{V_s} = \frac{1}{(1-D)(1+\beta)} \tag{55}$$

Note that β cannot be solved analytically and is I_{0n} dependent, and I_{0n} is the normalized load current. However, based on (48) and (55), design curves can be generated for design purposes.

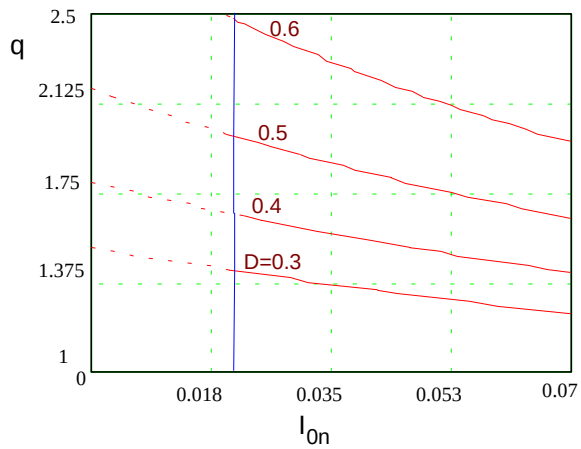
A set of design curves showing the relationship between voltage conversion ratio q and normalized load current I_{0n}, for different values of duty cycle D ($\omega_2 T_s$=48) is shown in Fig. 6.a. It can be seen that for a given value of D, a larger I_{0n} gives a lower voltage conversion ratio. This behavior is similar to that of boost-buck-boost converter [2].

In Fig. 6.b we can see a set of design curves showing the relationship between voltage clamping ratio β and normalized load current I_{0n}, for different values of duty cycle D. It can be seen that for a given value of D, a larger I_{0n} gives a larger voltage clamping ratio. In the same way, this behavior is similar to that of boost-buck-boost converter [2].

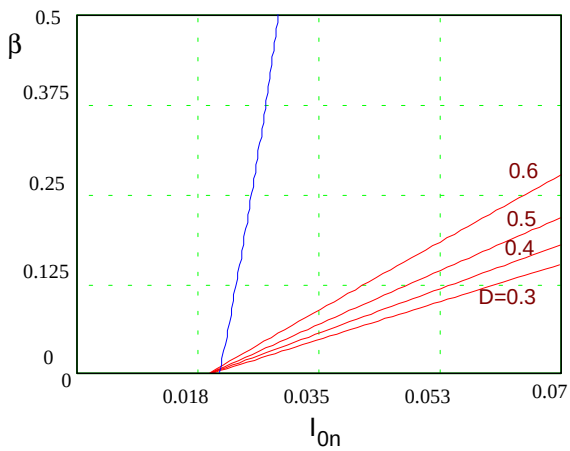
The mathematical model developed here holds while I_{L3} is greater then zero. Therefore, from equation (17), we have the following constraint:

$$I_{0n} \geq \frac{1}{\omega_2 T_s}\sqrt{1+2\beta} \qquad (56)$$

This constraint is shown in Figures 6.a and 6.b.



a)



b)

Fig. 6. a) Voltage conversion ratio; b) Voltage clamping ratio.

V. ZERO VOLTAGE CONDITIONS

In order to achieve zero voltage turn-on for S_2, there must be sufficient energy stored in the resonant inductor L_r to completely discharge the resonant capacitor C_r at t_5. Thus we have:

$$\frac{1}{2}L_r I_{L4}^2 \geq \frac{1}{2}C_r\left(V_c + V_0\right)^2 \qquad (57)$$

Then,

$$I_{0n} \geq \frac{(\beta+1)}{\sqrt{\frac{C_D}{C_r}}\omega_2 T_s} + \frac{\sqrt{1+2\beta}}{\omega_2 T_s} + (1-D)\beta - \frac{\beta}{\omega_2 T_s}\cos^{-1}\left(\frac{\beta}{\beta+1}\right) - 2\beta\frac{\delta}{T_s} \qquad (58)$$

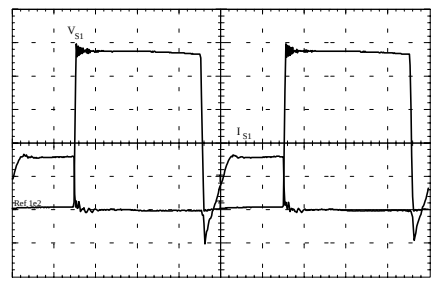
Equation (58) gives another constraint on I_{0n}. Which means that there is a minimum value of load current in CCM where ZVS turn-on for S_1 is kept, and it depends directly on L_r.

VI. EXPERIMENTAL RESULTS OF THE BOOST CONVERTER

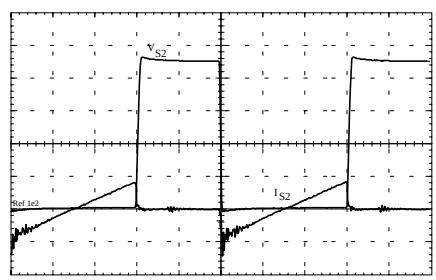
The new Boost converter was implemented, with the following specifications: output power P_0=1600W; input voltage V_s=300V; output voltage V_0=400V; switching frequency f_s=100kHz. The power stage consists of the following parameters:

- switches S_1 and S_2: Power MOSFET's IRFP460;- diode D_b: APT30D60;- diode D_c: APT15D100k - extern resonant capacitor C_D:1000pF/1.6kV- extern resonant capacitor C_{rext}: 1000pF/1.6kV;- capacitor C_c: 1.0μF/200V;- output filter C_f: 100μF/250V;- resonant inductor L_r: 37μH, core (E-45/15)-Thornton;- input filter L_f: 600mH, core (E-55) Thornton.

Experimentally obtained waveforms of the switches current and drain-to-source voltages and the resonant inductor current and voltage across the resonant capacitor are shown in Fig. 7.



a)



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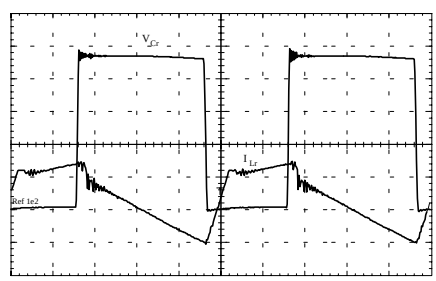
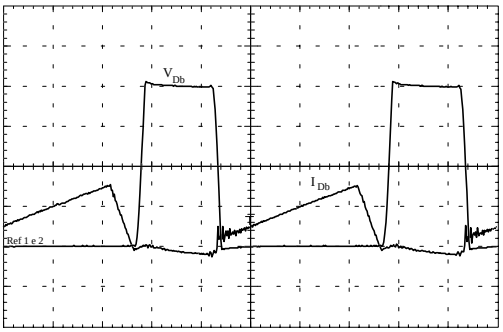


c)

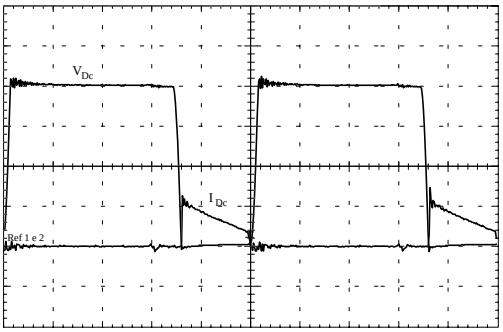
Fig. 7. a) Drain-to-source voltage across S_1 and current through S_1 and C_r; b) drain-to-source voltage across S_2 and current through S_2; c) voltage across C_r and current through L_r. (voltage: 100V/div; current: 5A/div; time scale: 2μs/div).

The voltage across diodes D_b and D_c and the current through these diodes are shown in Fig. 8. These waveforms

agree with those predicted theoretically, and as it can be noted from the waveforms shown in Fig. 7, the main switches (S_1 and S_2) present ZVS commutation with clamped voltages. From Fig. 8, it is possible to note that the diodes present ideal commutation conditions.



a)



b)

Fig. 8. a) Voltage across D_b and current through D_b (voltage: 100V/div; current: 5A/div; time scale: 2μs/div); b) voltage across D_c and current through D_c (voltage: 100V/div; current: 2A/div; time scale: 2μs/div).

In Fig. 9, the output voltage as a function of output current is shown, for different duty cycles, and in Fig. 10, the voltage across clamping capacitor for the same conditions can be noted.

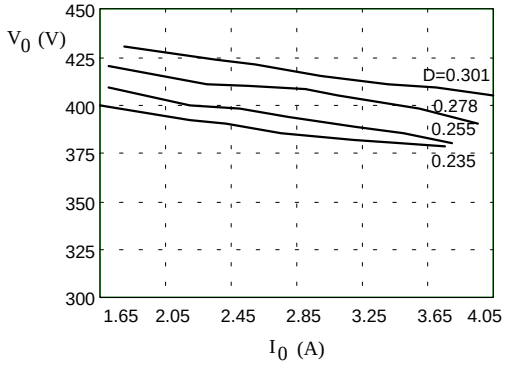


Fig. 9. Output voltage with different load conditions and duty cycle.

The experimental efficiency curve of the converter, is shown in Fig. 11, while the duty cycle necessary to keep the output voltage at 400V, is shown in Fig. 12. The converter presented high efficiency (up to 95%) from 40% to 100% of full load. At full load, the efficiency was 98%.

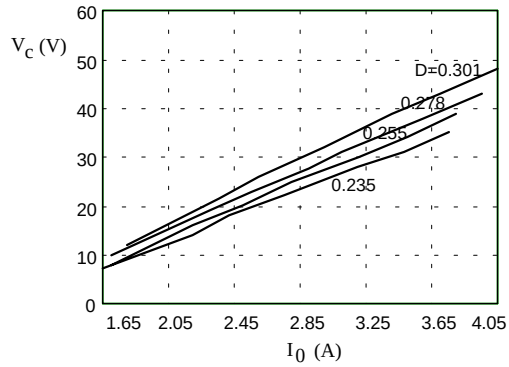


Fig. 10. Voltage across the clamping capacitor with different load conditions and duty cycle

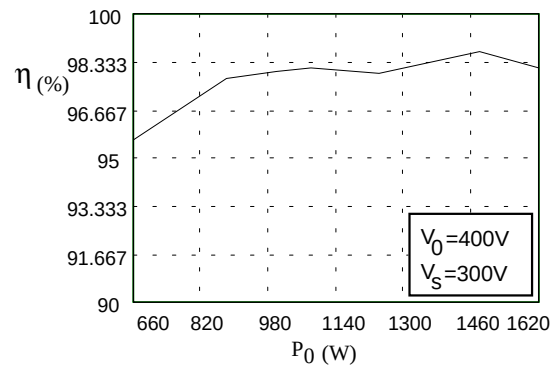


Fig. 11. Experimental efficiency curve with constant output and input voltage

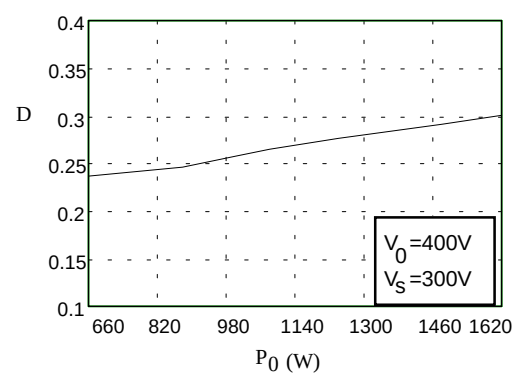


Fig. 12. Duty cycle variation to keep output voltage constant with different load conditions.

VII. CONCLUSION

A new family of DC-to-DC converters featuring clamping action, PWM modulation and soft-switching (ZVS) in both active and passive switches, is proposed to overcome the limitations of Clamped Mode DC-to-DC converters. As the resonant circuits absorb all parasitic reactances, including transistor output capacitance and

diode junction capacitance, these new converters operate with favorable switching conditions in all switching devices. Therefore, these converters are suitable for high-frequency operation.

VIII. REFERENCES

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