Switching Behavior of the PT-IGBT under ZCS Operation Based on Experimental Results and PSpice Simulations

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***Abstract* - Switching loss reduction through soft commutation techniques such as zero-current- (ZCS) and zero-voltage switching (ZVS) is widely used in converter designs. This work presents the behavior analysis of the IGBT under ZCS conditions and the design considerations of a special test circuit. The selected operation mode, single-shot, allows to limit the power source consumption, which facilitates to carry out tests in extreme conditions. The study includes an analysis of the voltage (V_0) and IGBT hold-off time dependence of the collector tail current as well as the analysis of the IGBT reverse conduction due to the reverse recovery phenomenon of the internal diode.**

***Index Terms* – Zero-current-switching, test circuit, PSpice simulations, Punch-Through-IGBT**

I. INTRODUCTION

Current researches about power semiconductor devices are oriented to increase the power switching capacity and switching frequency [1]. The search of a better performance of the converter operation bears, in occasions, to power semiconductor analysis, which is very close to converter design needs. The semiconductors used are submitted to high temperature changes, which alter the physical parameters of silicon and modify the device behavior. It is possible to design special test circuits to study and characterize power semiconductor devices [2],[3]. This allows a better control of external parameters and the reproduction of real operating conditions. In the case of hard switching (PWM), special test circuits have been used a lot [4], while in soft switching (*ZC, ZV*) application circuits are more usual for the analysis of the device behavior [5]. However, this makes it difficult to compare the results of different test conditions. Therefore, in this work a different special test circuit is proposed, which allows component evaluation under soft switching conditions and which is able to control the test parameters as independent as possible.

The aim of this paper is to give a complete analysis of the different behavior of Punch-Through-IGBTs under ZCS operation mode including the influence of variations of the circuit parameters, such as the hold-off time (anti-parallel diode conduction time) and the voltage (V_0) on the collector tail current as well as the analysis of the IGBT reverse conduction due to the reverse recovery phenomenon of the internal diode.

The study uses experimental results obtained with a special test circuit and in addition PSpice simulations performed with different models available on the market.

II. OPERATION OF THE PROPOSED TEST CIRCUIT

In the test circuit design were taken into consideration aspects such as the limitation of the number of circuit elements and the power of the source. The function mode selected, *single-shot*, limits the power source consumption and facilitates tests under extreme conditions without the risk of device damage. In this work, the test circuit is designed to reproduce the operating conditions of a power factor rectifier with ZCS type soft commutation presented in [6] and is able to control the test parameters as independent as possible.

Fig. 1 shows the special test circuit, which allows understanding the basic single-shot operation mode as it is described with more detail in [7].

Phase 1 ($t_0 < t < t_1$): The auxiliary switch K_A is turned on until the current I_L in the input inductor L_1 reaches the reference value I_{Ref} that serves as initial condition for the resonant stage. The value of I_{Ref} is modulated changing the off time of K_A.

$$I_{L1} = \frac{V_0}{L_1}(t - t_0) \qquad (1)$$

Phase 2 ($t_1 < t < t_2$): At the instant $t=t_1$, K_A is turned off. The duration of this stage t_c must be large enough to recharge the capacitor C_C to a voltage value equal to V_0 (in case V_{Cc} is much smaller than V_0).

$$t_C \geq \frac{(V_0 - V_{C0})}{I_{L_1}} C_C \qquad (2)$$

Phase 3 ($t_2 < t < t_3$): At the time $t=t_2$, the switch under test K_P is turned on and the current through the resonant inductor decreases linearly to zero from $I_{Lc} = I_{Ref}$.

$$I_{Lc}(t) = \frac{V_0 (t_2 - t)}{L_C} + I_{L_1} \qquad (3)$$

Phase 4 ($t_3 < t < t_4$): At $t=t_3$, K_P is submitted to the resonance in soft switching conditions. K_P is conducting during a time period depending on the reference current I_{Ref} and the resonance period in accordance with the values of L_C and C_C in the specific application. I_{Lc} and V_{Cc} are given by:

$$I_{Lc}(t) = \frac{V_0}{Z_C} sin(\omega_C (t - t_3) \qquad (4)$$

$$V_{Cc}(t) = V_0 \cdot \cos(\omega_C (t - t_2) \qquad (5)$$

where $Z_C = \sqrt{L_C / C_C}$, $\omega_C = 1/\sqrt{L_C \cdot C_C}$ and the time period of the resonance T_C is:

$$T_C = 2 \cdot \pi / \omega_C = 2 \cdot \pi \sqrt{L_C C_C} \qquad (6)$$

From t_2 to t_4 the current through K_P is given firstly by a linear excursion during the time period (t_3 - t_2) and then a by a positive resonance from t_3 to t_4.

$$I_{Kp}(t) = \frac{V_0}{Z_C} sin(\omega_C (t - t_3)) + I_{Ref} \quad (7)$$

The time period of the resonant mode T_C^+ is obtained from the condition $I_{Kp} = 0$ as follows:

$$t_4 - t_3 = T_C^+ = \frac{1}{\omega_C} \cdot \left[acsin(\frac{Z_C I_{Ref}}{V_0}) + \pi \right] \quad (8)$$

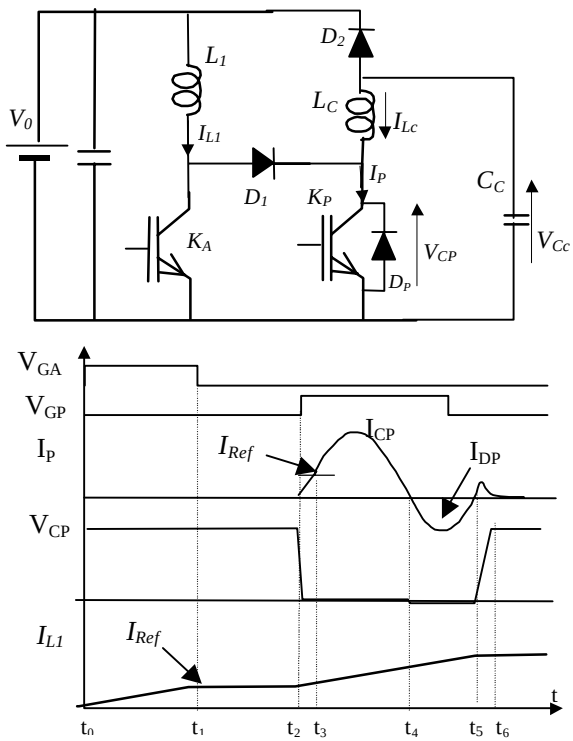

***Fig. 1**: Proposed test circuit for ZCS and operation waveforms*

Phase 5 ($t_4 < t < t_5$): At the instant $t=t_4$ the current I_{KP} becomes negative and is switched to the anti-parallel diode D_P. During this phase, characterized by the hold-off time $t_d = t_5 - t_4 = T_C - T_C^+$, the gate of the IGBT ($K_p$) is turned off.

Phase 6 ($t_5 < t < t_6$): At $t=t_5$, when positive resonance should occur again, K_P blocks the current since it is turned off and the voltage across it rises to the value of V_0 (ZCS). The capacitor C_C is recharged to V_0, which finishes the cycle.

$$V_{Cc} = \frac{I_{L1}}{C_C}(t - t_5) \quad (9)$$

III. PSPICE SIMULATION CONDITIONS

The schematic of the circuit, which was simulated with PSpice is illustrated in Fig. 2. It can be observed that for simplicity the input inductor L_1 of the test circuit was replaced by a constant current source, which has the value of the reference current I_{ref}. Three different models were tested to simulate the PT-IGBT used in all experiments (IRGPH50F from International Rectifier):

1. a model provided in the PSpice model library for a very similar device (IRGPC50H) that uses the internal PSpice IGBT model [8],[9]
2. a subcircuit model (macromodel) provided by International Rectifier in Internet for the IGBT IRGPH50H
3. a simple subcircuit model consisting of a MOSFET controlled BJT that uses the internal PSpice BJT and MOSFET models. The parameters of the BJT and the MOSFET were adjusted to match the characteristics of the IRGPH50F from the manufacturer data sheets.

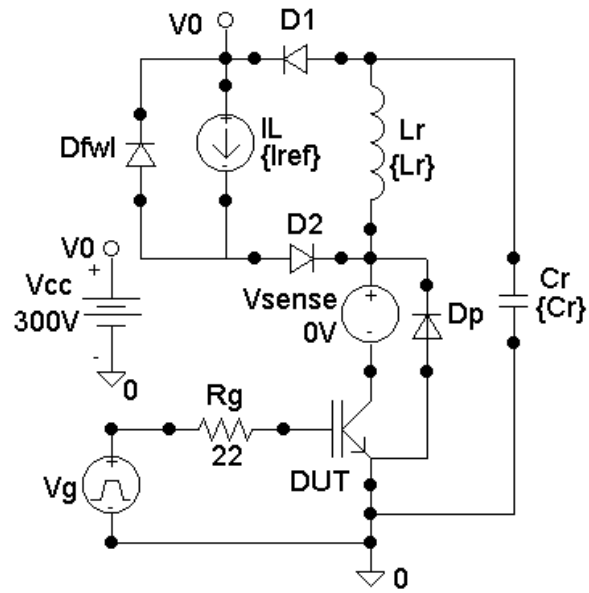

***Fig. 2**: Schematic of the circuit simulated in PSpice*

IV. TURN-OFF BEHAVIOR OF THE PT-IGBT UNDER ZCS CONDITIONS

During the conduction time of the IGBT ($t_4 - t_2$), the device carries the current I_{Kp} which causes conduction modulation in the base of the internal pnp-BJT by injection of an excess charge Q_S. The value of Q_S depends on the magnitude of the collector current (I_{Kp}) and the junction temperature, essentially. Since in ZCS mode the collector current in the switch decreases due to the resonance imposed by the external circuit, the collector-emitter voltage during this phase is still very small (Vce_{sat}) and a large amount of excess charge remains in the n^--region after the zero crossing of the collector current. During the hold-off time t_d, the stored charge decreases by two effects, first by a diode like reverse recovery current (since the base-emitter junction of the internal pnp-BJT acts like a diode) and second by excess carrier recombination in the BJT-base. The second effect removes the major part of the stored charge Q_S [1]. If there are still excess carriers in the n^--region when the IGBT is stressed with forward blocking voltage at the end of the hold-off time, the remaining charge is removed by the increasing collector-emitter voltage analogous to the tail phase under hard switching turn-off conditions. Therefore, the evacuated charge results in a current peak that causes turn-off losses of IGBTs in ZCS applications (Fig. 3a). The internal pnp-transistor of PT-IGBTs has a high emitter coefficient combined with a short high-level carrier lifetime. As a result, the excess charge existing in the base at the time of the zero crossing of the switch current recombines relatively fast.

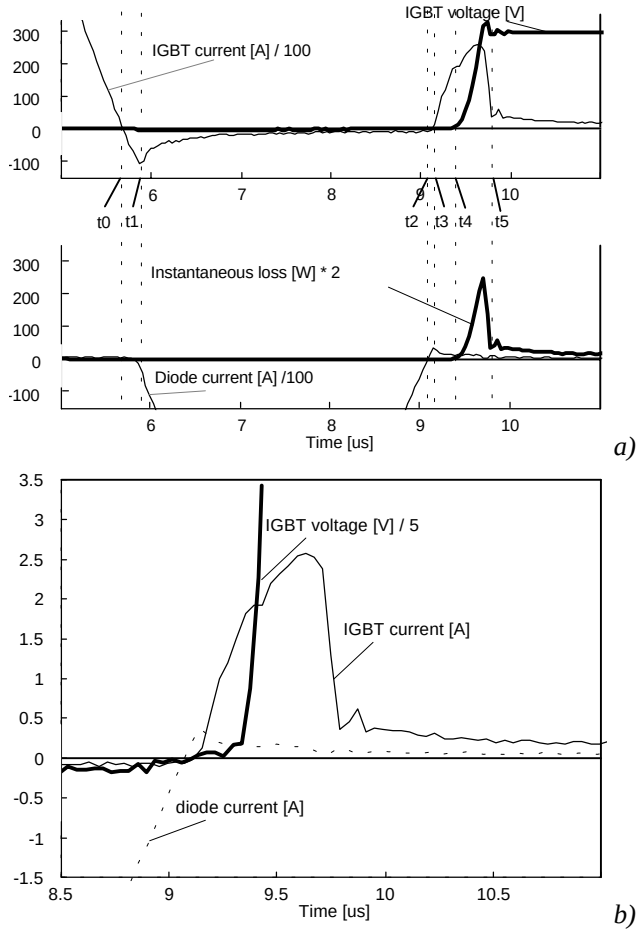

Fig. 3: *a) Different phases of the currents, voltage and loss transients*
b) Detail of the second zero-crossing in the IGBT current

V. ANALYSIS UNDER DIFFERENT CONDITIONS

In Fig. 3a can be observed the measured current through the IGBT and the anti-parallel diode. We can distinguish different phases after the first zero-crossing of the total switch current:

1. the IGBT-current does not switch immediately to the anti-parallel diode, but flows in negative direction during a certain time period t_1-t_0 (reverse recovery behavior of the IGBT)
2. the negative current switches from the IGBT to the anti-parallel diode. This phase finishes in the instant t_2, when the diode current becomes zero.
3. the switch current becomes positive (flows in negative direction through the anti-parallel diode) due to the reverse recovery behavior of the diode and reaches its maximum value at t_3. At this instant the voltage across the switch becomes zero (Fig. 3b).
4. the reverse recovery diode current decreases to zero and the tail current of the IGBT begins to rise. During this phase the voltage is still zero, since in the IGBT excess charges have to be removed from the collector edge of the n^--base of the internal BJT before the space charge region can expand allowing the blocking voltage to increase.
5. at the time instant t_4, the voltage across the switch increases fast until reaching the supply voltage V_0. During this phase the IGBT tail current reaches its maximum and at the time t_5 it has already decreased to a very small value.
6. the phase beginning in t_5 is characterized by a small tail current with a slow decay.

From Fig. 3a, which also illustrates the instantaneous losses in the zero current switch during the whole turn-off period, results that almost all losses are generated during phase 5 due to the tail current of the IGBT and the simultaneous high blocking voltage. Both, the reverse recovery current of the IGBT and the one of the diode do not cause turn-off losses since the voltage is very small in these time periods.

Therefore, in this paper will be analyzed with more detail the behavior of the IGBT tail current characterized by the tail charge Q_S (quantity of stored rest charges in the n^--region of the IGBT corresponding to the area under the tail current transient). Different cases were analyzed by experiments and PSpice simulations for V_0=300V, I_{Ref}=5A (t_d=3.6µs), f_0=100kHz, a resonant current amplitude of 15A and an IGBT turn-off instant near the first zero-crossing of the collector current:

- variation of the hold-off time t_d, i.e. the anti-parallel diode conduction time, which was adjusted with the reference current I_{Ref}
- variation of the instant when the IGBT is turned off
- variation of the junction temperature
- variation of the carrier lifetime (only simulation)

***Hold-off time t_d*:** The quantity of stored charge Q_S in the IGBT after the second zero-crossing of the current is a function of the anti-parallel diode conduction time or hold-off time t_d, since the longer this period, the more charges can be removed by recombination in the drift region of the IGBT. In addition, the higher resonant current, that flows through the IGBT before the first zero crossing (which is required to reduce the hold-off time), causes more current to be injected in the IGBT which results in a higher charge as well. Experimental tests were performed for several values of t_d between 1.4µs and 4.5µs, which were adjusted by I_{Ref}=1-10A, whereas in simulations t_d was reduced until the limit of soft commutation, i.e. reference currents up to 14A. Fig. 4 illustrates how the shape of the IGBT tail changes for different values of t_d. Experimental curves as well as simulated ones show how the tail peak increases with the hold-off time, although the tail charge (area under the current tail) is expected to decrease at a higher t_d, as verified in Fig. 8a. The simulation results obtained with the subcircuit model provided by International Rectifier have no typical tail shapes (it seems to be only a displacement current due to the output capacitance of the IGBT during voltage rising), which demonstrates that the base charge of the IGBT is not correctly modeled. Experimental results in Fig. 8a show, that the IGBT rest charge is reduced to 50%, when t_d is increased from 1.4µs to 4.5µs. Simulated values are higher than the measured ones (excepting the mentioned IR model) especially for the simple MOSFET/BJT model. However, this model shows clearly the trend of tail charge reduction at higher hold-off times, whereas the

internal PSpice model represents the quantitatively best approach.

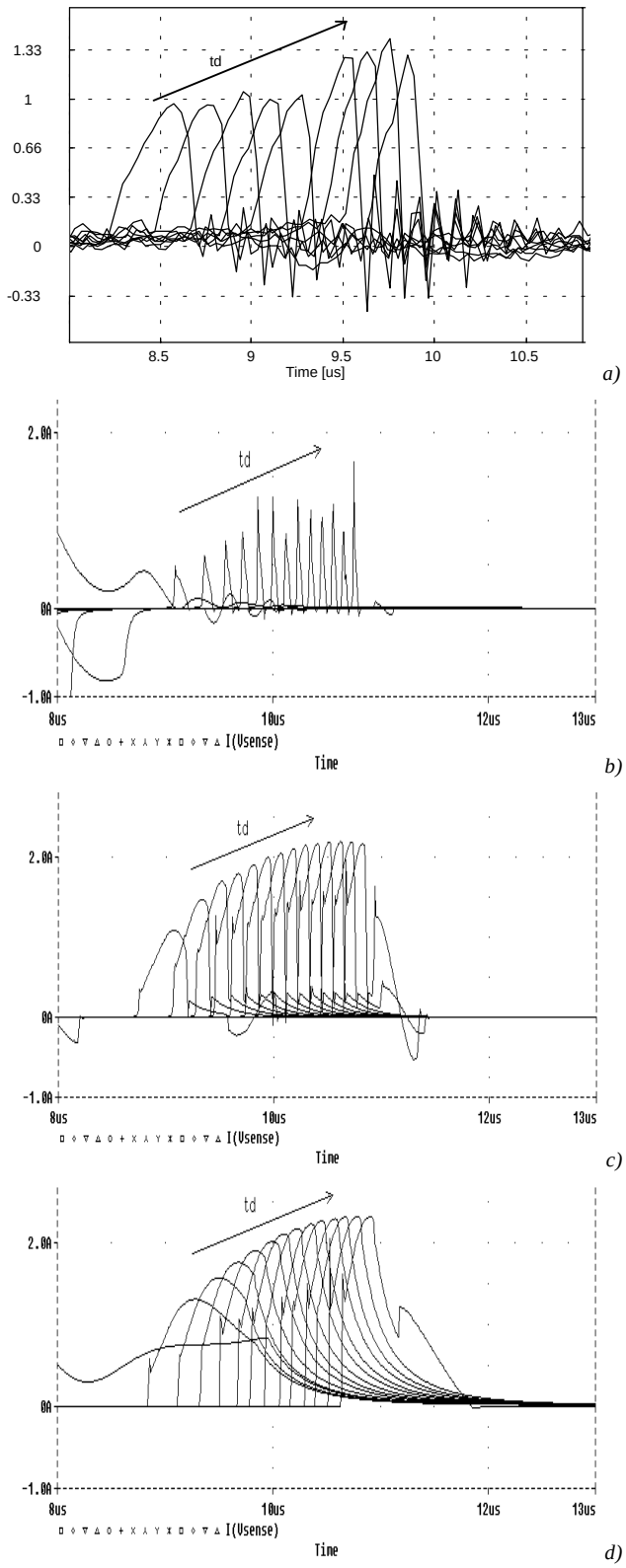

Fig. 4: *IGBT tail current transients for different hold-off times a) measured curves, b) simulated with IR model, c) simulated with PSpice IGBT model, d) simulated with MODEFT/BJT model*

IGBT turn-off instant t_{off}: For this analysis the IGBT was turned off at different times varying between the first and the second zero-crossing of its collector current. The measured transients of Fig. 5 illustrate that Q_S depends lightly on the turn-off instant for the PT-IGBT, where a variation of 22.5% was observed (Fig. 8b). The most important change occurs when the turn-off instant is varied within the reverse recovery phase of the IGBT (phase 1). This is because meanwhile the IGBT is not turned off the stored charge can be removed by an electron current through the MOS channel during the reverse conduction of the IGBT. When the reverse current switches to the anti-parallel diode this effect is no more relevant. For the PT-IGBT the relationship of electron and hole current at the collector edge of its internal BJT is always smaller than the mobility ratio, that means that the electron current is not significant enough to cause important changes depending on the instant when the IGBT is turned off. The analyzed models do not include this effect, since simulations do not present changes at all when the turn-off instant varies.

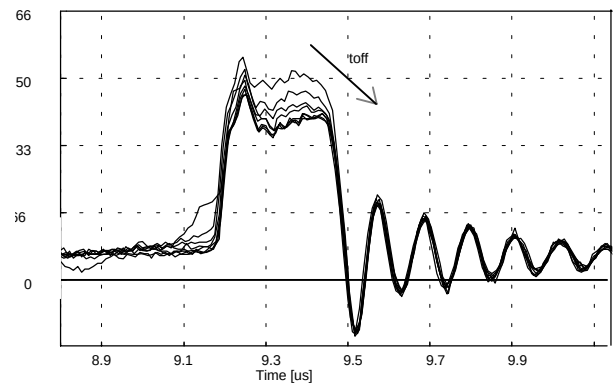

Fig. 5: *Measured IGBT tail current transients for different turn-off times*

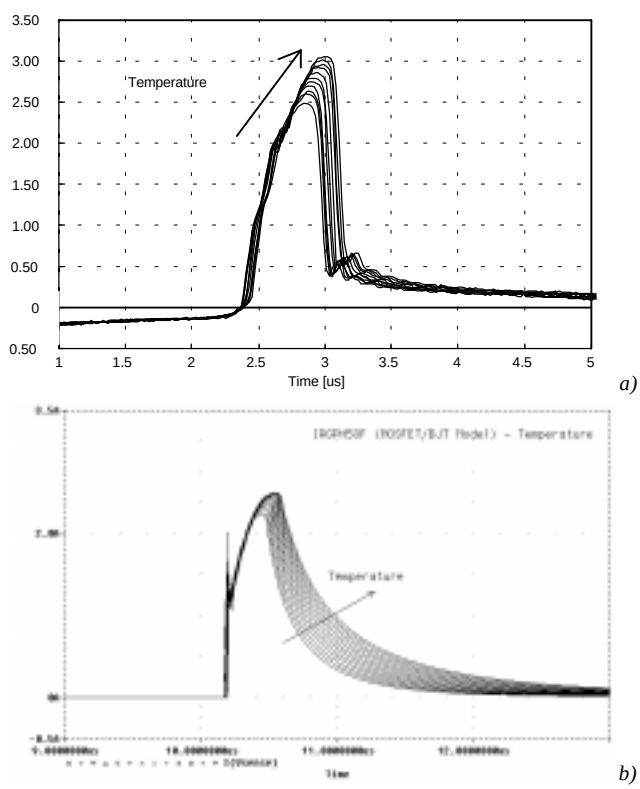

Fig. 6: *IGBT tail current transients for different junction temperatures a) measured curves, b) simulated with MOSFET/IGBT model*

***Junction temperature*:** The junction temperature T_j has been increased in experiments from 30°C to 130°C and in simulations from 20°C to 120°C. In this case, the results of Fig. 6a show that both the amplitude and the duration of the current tail are increased proportionally to the temperature increasing consequently the tail charge and the losses during ZCS turn-off (Fig. 8c). This means that a higher junction temperature is equivalent to more stored excess charges in the IGBT base which is physically correct, since carrier lifetime as well as the intrinsic concentration of silicon, increase the temperature. Fig. 6 illustrates that the temperature influence is quite marked (446% increase in Q_S) due to the strong carrier lifetime dependence on the behavior of PT-IGBTs. Temperature dependent simulations could be performed only with the simple MOSFET/BJT model, since the other ones are valid only at room temperature. Fig. 6b shows these results, which are in good agreement with the measured trend.

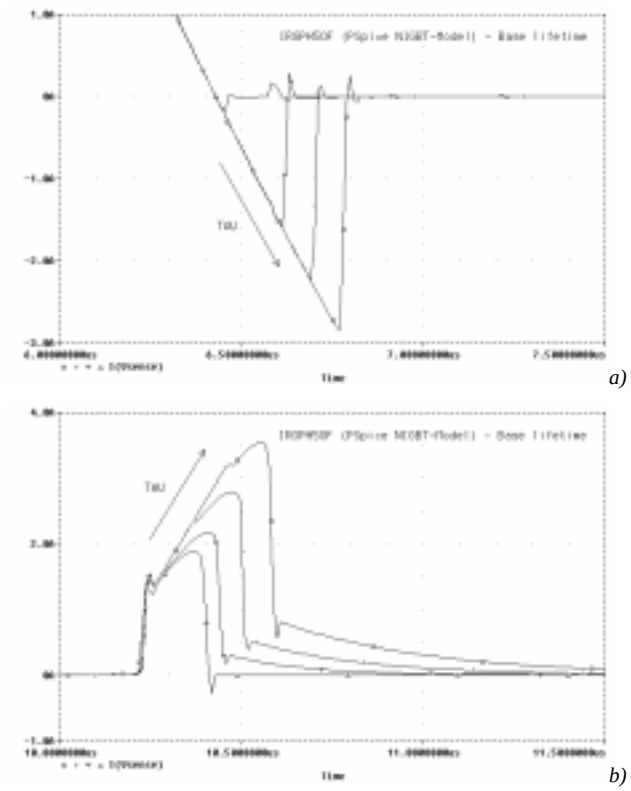

Fig. 7: ***a)IGBT reverse current and b) IGBT tail current for different base lifetimes simulated with the internal PSpice IGBT-model***

Base lifetime: The carrier lifetime in the drift region is a very important technological device parameter, which cannot be changed in the test circuit. However, the internal PSpice IGBT-model considers the base lifetime in its equations, i.e. by simulations can be obtained the lifetime dependence of the device behavior under ZCS conditions. Fig. 7 illustrates these simulation results, were the value for the lifetime parameter TAU was changed from the default value of the IRGPH50F model (204ns) to 4ns, 304ns and 404ns. The lifetime dependence of the IGBT collector current is clearly demonstrated. Fig. 7a shows the reverse current variation with TAU, which is quite similar to that of a power diode during reverse recovery. Fig. 7b represents the lifetime dependence of the tail current and it can be seen how this parameter strongly influences the switching losses generated by the device. This theoretical study leads to the conclusion that IGBT types without lifetime control would exhibit relatively high switching losses during a ZCS commutation mode.

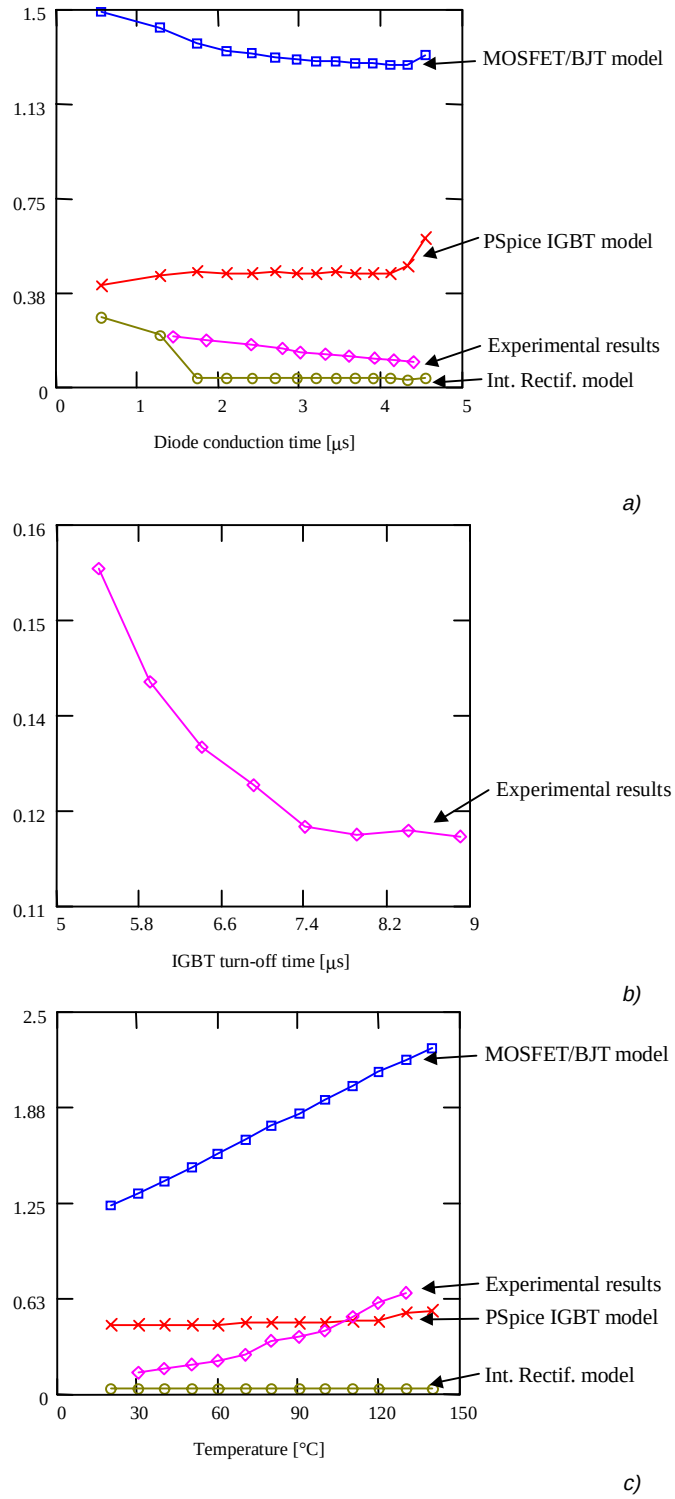

Fig. 8: *Tail charge Q_S of the IGBT versus a) hold-off time, b) IGBT turn -off time, c) junction temperature – measured data and simulation results with different models*

IV. CONCLUSIONS.

A special test circuit was designed and implemented which allows:

- to reproduce the waveforms of a real application topology, a ZCS power factor rectifier in this case
- to study in detail the device under test for a better comprehension of the switching phenomena in ZCS converters
- to make a comparative study of stored charges and losses during the tail phase as a function of different test parameters, which helps to find the maximum safe operating frequency
- to set the external parameters, which should represent the real application as: maximum resonant current frequency, voltage, temperature, wiring effects
- to evaluate the IGBT behavior under real operating conditions without destruction risk

The study of the behavior of the PT-IGBT under ZCS conditions varying test parameters such as the hold-off time, the IGBT turn-off time and the temperature, was performed by both experiments and simulations with different models available on the market.

Experiments and simulations proved, that the larger the anti-parallel diode conduction time (hold-off time) the smaller the tail charge and consequently the generated losses, since carriers have more time to recombine. Measurements showed also that switching off the IGBT at the end of the hold-off time helps to reduce the tail current up to 22.5% compared to the case when the gate is turned off at the first zero crossing of the collector current. This is due to the fact that additional charges can be removed by the MOS channel current during this phase. It has been shown by experiments and simulations that the temperature strongly influences the tail current of PT-IGBTs causing a 446% increase in the tail charge when the device is warmed up from 30°C to 130°C. The base lifetime dependence of the collector current (which is included in the temperature dependence) could be obtained separately by simulations with the internal PSpice IGBT-model that considers this parameter. A considerable increase in both the reverse current and tail current of the IGBT when the device is operating with higher lifetimes was proved by this way.

From the tested IGBT models for the PSpice simulator, the internal PSpice IGBT-model presented quantitatively the best agreement with experimental results, meanwhile the simple MOSFET/BJT model reproduces quite well the trend of the test parameter dependence of the tail charge. Therefore simulations can be used to qualitatively predict the tail charge behavior under ZCS conditions.

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