Power Factor Correction: Shifting of Input 60Hz Rectification to the Secondary of Isolation Transformer.

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Abstract: Input diode bridge introduces power losses and distortions in Power Factor Correction (PFC) circuits. A new approach is proposed which eliminates the separate input diode rectification stage and integrates the rectification into the switching converter itself. This general idea will be introduced and proposed for several topologies. Efficiency, performance and other characteristics are analyzed using one practical example; key features of the new approach are verified on the experimental prototype.

I. INTRODUCTION.

Input rectification is usual for the most topologies in AC/DC applications, so are the associated distortions and power losses.

Circuits without input rectification have been developed [1,2,3,4,5,6]. Different classes of such circuits can be determined. There are circuits that implement an idea of having 2 parts of the circuit, or sometimes 2 whole converters, working during positive and negative halves of line period respectively. These parts of the circuits usually are tried to be designed to share common components, so it simplifies the schematic and improves size and cost characteristics [6,7].

An interesting circuit is developed in [3]. It shows high efficiency and good performance, however the output voltage is doubled in comparison with traditional topologies. The lowest voltage gain is 2, and for universal input it imposes a very high output voltage.

Other class of circuits is presented by authors in [6]. The basic idea is that in order to get DC output (for example positive) from non rectified AC input, converter topologies with specific gain characteristics can be considered. If some topology has positive and negative parts of gain characteristics (i.e. it can produce positive or negative output voltage from just positive input) then it can produce strictly positive output voltage from any (positive or negative) input. Such topologies can be called topologies with bipolar gain characteristics. If suitable control is found then such topology can implement PFC as well, and therefore produce positive DC output from non rectified AC input.

As it was shown in [6], such topologies tend to have high rms currents. Therefore their efficiency can be less competitive in comparison with traditional topologies at high input voltage region where relative losses in input diode bridge are not significant.

Another class of circuits without input rectification is introduced in this paper. It is derived from traditional DC/DC or AC/DC topologies appropriately modified to operate from AC input. However, the rectification must be performed at some later section of the converter. The most desirable would be to have already existing devices, operating at high switching frequency (higher than 20 KHz) also perform at the same time the effective rectification of the low frequency (60 Hz) AC. It can be expected that this integration of both high frequency switching and low frequency rectification will result in simpler and more efficient power stage configuration. There is a number of DC/DC converters which meet this double-duty criteria. These circuits also usually require four quadrant switches and appropriate topological modifications. Example of the new approach will be considered in detail on the basis of current fed push-pull or so called Clarke converter.

A related circuit with rectification at the secondary was presented in [2] as a flyback battery charger, but in that schematic diode bridge was just moved from high voltage side to low voltage side and therefore benefits were doubtful. Circuit in [2] was also only computer simulated and lacked features proposed in this paper.

It is necessary to point out that although some particular example will be analyzed in presented work, and experimental results will be shown for that circuit: the idea is general and other topologies and control circuits can be used.

II. BASIC CONSIDERATIONS.

Consider a loss budget for an arbitrary AC/DC PFC: diode bridge will have 2-2.5 V voltage drop under high input currents, which results to about 1.5-2% loss of input power for standard 115 V input. Specifications, however, typically include 85 V as a lower boundary of converter operation. Define diode characteristic by equation (1)

$$I_D = I_0 \left(e^{\frac{V_D}{V_B}} - 1 \right) \qquad (1)$$

where I_D and V_D are diode current and voltage respectively, and I_0 and V_B are diode parameters. Then the relative losses in a diode bridge can be found as (2).

Fig.1 illustrates loss calculation for the rectifier based on **D25XB800H** (from **Shindengen**) and **MUR3060** (from **Motorola**) in case of 100W output power. It shows that at

85 V input voltage the losses are in 2.5-4% range. If line voltage is lower in some applications then losses become catastrophical.

$$\frac{P_{Bridge}}{P_{in}} = \frac{2V_B \ln\left(1+\frac{Ig}{I_0}\right)}{V_g} \bullet 100\% \qquad (2)$$

Notice that increasing the power will raise the relative losses since voltage drop on the input diodes will increase with the current. This big value of losses in only one discussed component is important and possibly dominating, considering overall efficiency above 90%.

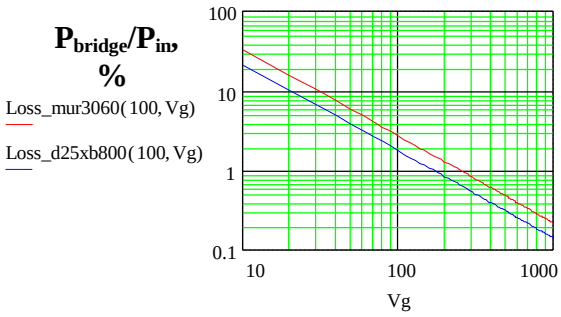

Fig.1: Relative losses % in a diode bridge as a function of input voltage *Vg* for 100W output.

The usage of active rectifier will be more expensive and becomes inappropriate when voltage drop on the on-resistances of the switches is higher than voltage drop on the diodes (which happens under high enough current). Other fact to consider is that any rectifier is a switching network, introducing corresponding EMI noise. The elimination of input rectification is therefore an attractive goal.

Topology without input rectification potentially has the following advantages in AC/DC application:

1) does not have uncontrollable losses in input rectifier bridge (efficiency improvement)

2) does not have 4 high-power elements (cost, size)

3) circuit has less nonlinear elements: simpler design and analysis, better performance in terms of EMI, input filter excitation, control

4) simplified input filter considerations (cost, size)

The drawbacks are expected to be that topologies, as well as control circuitry, have to be modified for non rectified input.

III. THE GENERAL CONCEPT.

The general idea can be best illustrated in Fig.2, where typical isolation section of the switching converter is shown. The two diodes operate at the switching frequency and generate rectified (DC) voltage regardless of the polarity of the voltage applied to the primary side. In this way, the diodes can perform the double-duty: high frequency switching and rectification as well as same time the rectification of the low (60 Hz) line frequency.

Typical converters may have primary side with either simple winding (such as flyback converter) or tapped (two windings) primary side (such as in push-pull and bridge-type converters). Thus, the next section will give examples of both general cases.

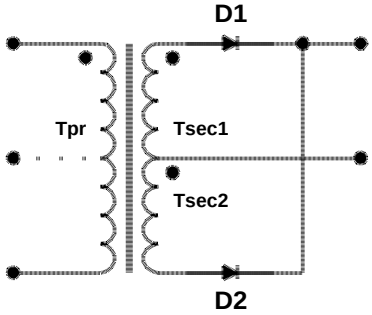

Fig.2: General isolation transformer with two secondaries and following rectifiers.

Some topologies with isolation transformer have only single secondary winding. Sometimes it is possible to add another one and create schematic in Fig.2 without violating the operation of the converter. Then same idea of line rectification can be applied. Example of such case is flyback converter, illustrated in the next chapter.

Using non rectified input voltage at primary side of the converter would normally lead to the need to implement four quadrant (ideal) switches. Such switches have to conduct current in any direction and block voltage of any polarity since the input voltage is not rectified any more. Possible solutions are shown in Fig.3.

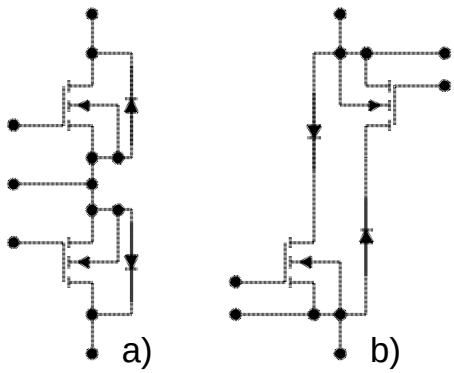

Fig.3: Implementation of the four quadrant switches.

Fig.3 a) shows combination of two current bi-directional switches and Fig.3 b) refers to combination of two voltage bi-directional switches. The version a) is more attractive because of simpler control of the switch and less DC losses.

IV. EXAMPLES OF MODIFIED TOPOLOGIES.

Fig.4 shows flyback derived topology (input EMI filter is not shown). It implements the general presented idea of line rectification on the secondary of isolation transformer

and has less losses and device count than topology described in [1].

Control and operation of such converter is pretty much similar to traditional case of flyback power factor corrector. Isolated drive is needed for the four quadrant switch, and some modifications are possibly needed for voltage/current sensing of the modified converter. Turns ratio of the transformer should be such that only one diode is operating at each half of the line cycle, as in traditional flyback.

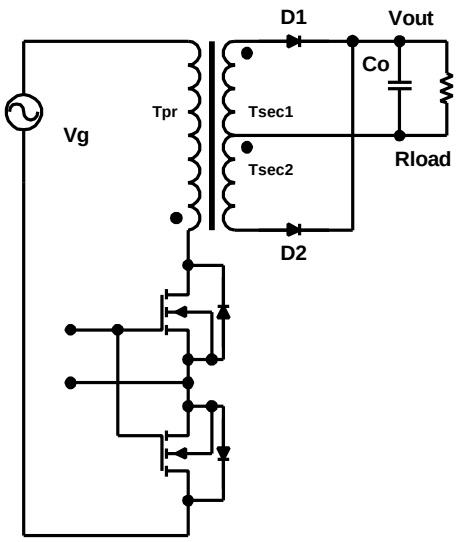

Fig.4: Modified flyback topology.

Similar modifications can be done to many other topologies, as it was mentioned in section III, so the following discussion will concentrate on one practical example.

Fig.5 shows current fed push-pull, which is also called isolated boost or Clarke converter. Switches A and B are driven with overlaps, and overlapping part of the switching period corresponds to on time of the switch in parent boost converter. Operation and waveforms are therefore similar to the simple boost case.

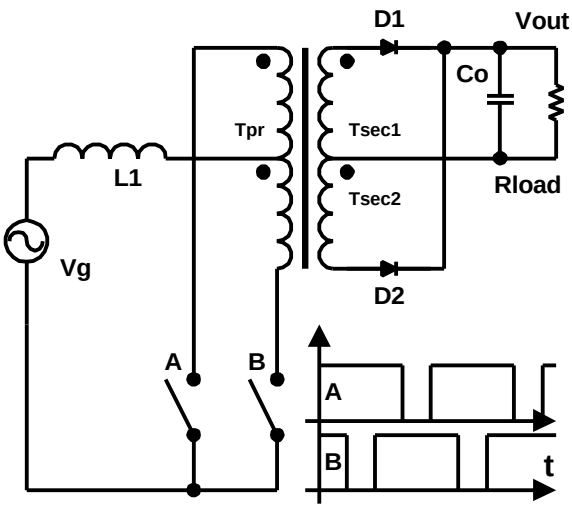

Fig.5: Clarke converter as power factor corrector without separate input rectification stage.

The implementation of the Clarke converter in Fig.5 was discussed, for example, in [7], but with the conventional diode bridge rectification stage. Our approach, outlined in section IV is to eliminate the diode bridge stage all together and still achieve power factor correction. This is possible in this topology as described earlier, thanks to integration of rectification at high switching frequency and low frequency (60 Hz AC) in the same switching devices of the original basic DC/DC isolated topology. Basic converter has to be appropriately modified, for example, the original primary side switches A and B (Fig.5) must be replaced with four quadrant switches.

Sometimes additional switch is used to clamp middle point of the primary winding to the ground during the overlap time of switches A and B, so losses in primary winding and switches is decreased, [7]. Such switch C will be used in the prototype, as it will be shown in later sections (Fig.10). Soft switching for A and B switches can be provided this way. It is especially useful if IGBTs are used as main A and B switches, so additional switch eliminates the losses during long turn off of IGBTs. Switches A, B and C have to be four quadrant switches and are implemented as shown in Fig.3 a) with MOSFETs.

V. ANALYSIS OF THE CHOSEN TOPOLOGY.

Operation of the chosen topology (isolated boost or Clarke converter) is very close to one of the boost, with similar gain characteristics and dynamics. By time interval *DTs* we will understand overlap time interval when both switches A and B are on.

Ideal gain is then easily derived as shown in (3) and plotted in Fig. 6, where *N*=1.5 is a transformer turns ratio.

$$M(D) = \frac{Vo}{Vg} = \frac{N}{1-D} \qquad (3)$$

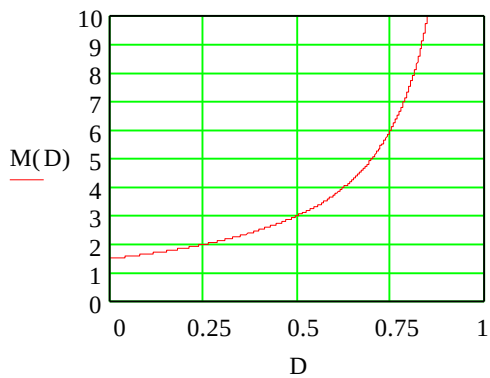

Fig.6: Ideal gain *M(D)* for the isolated boost.

Let's now introduce parasitic element to represent losses in the components of the converter, Fig.7. Simple assumptions are made, for example assuming low ripple in input current; not all losses are taken into account. *Rl* represents resistance of the inductor, *Rs* is on resistance of the switch plus resistance of the transformer winding, *Vd* is

a voltage drop across the diode.

Efficiency of the converter can be therefore expressed as (4), where *Pout*, *Vo* and *Io* are output power, voltage and current respectively, *Ploss* represents losses, and *Vg* and *Ig* are input voltage and current. It is clear that *Ig/Io=M(D)*, since no additional paths for current were created (where *M(D)* is an ideal voltage gain from (3)). $M_R(D)$ represents real voltage gain of the converter.

$$h = \frac{Pout}{Pout + Ploss} = \frac{V_o I_o}{V_g I_g} = \frac{M_R(D)}{M(D)} \qquad (4)$$

Expressing losses in parasitic resistances and diode by rms currents and then by output voltage and load resistance, final equation is achieved (5)

$$Ploss = \left(\frac{VoN}{(1-D)Rload}\right)^2 Rl + \left(\frac{VoN}{(1-D)Rload}\right)^2 \left(1-\frac{D}{2}\right)^2 Rs + \frac{Vd}{N}\frac{Vo}{Rload\sqrt{1-D}} \qquad (5)$$

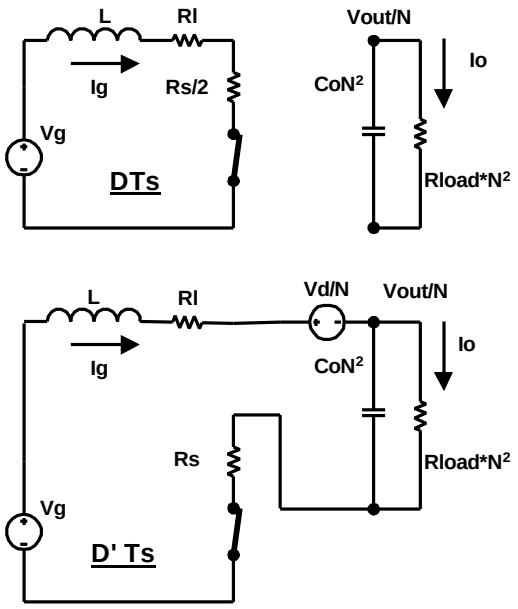

Fig.7: Equivalent circuit with parasitics for *DTs* and *D'Ts* time intervals.

Finally, efficiency can be expressed as:

$$h = \frac{1}{1 + b(D)} \qquad (6)$$

where

$$b(D) = \frac{N^2 Rl + N^2\left(1-\frac{D}{2}\right)Rs + DRs + \frac{Vd}{Vo}\frac{(1-D)^{3/2}}{N}}{(1-D)^2 Rload}$$

Predicted efficiency as a function of duty ratio for isolated boost is shown in Fig.8.

Predicted voltage gain, as a function of duty ratio *D*, can be expressed from (4) via efficiency and ideal gain and plotted (Fig.9). Value 1.5 was used for *N*.

Derived characteristics are similar to ones of the conventional boost converter, as expected.

Operation of the boost is a common knowledge, the isolated boost or current fed push pull can be analyzed similarly. The main interest is therefore in the difference of new modified isolated boost in terms of losses or efficiency.

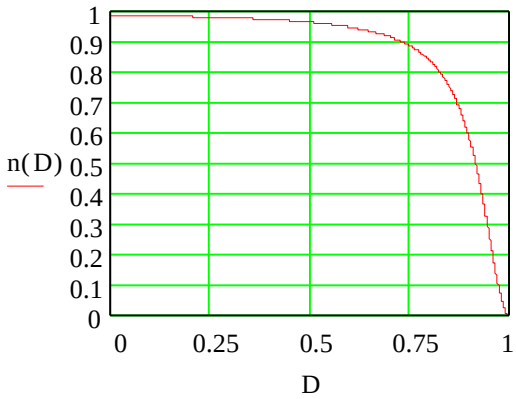

Fig.8: Efficiency as a function of duty ratio for isolated boost.

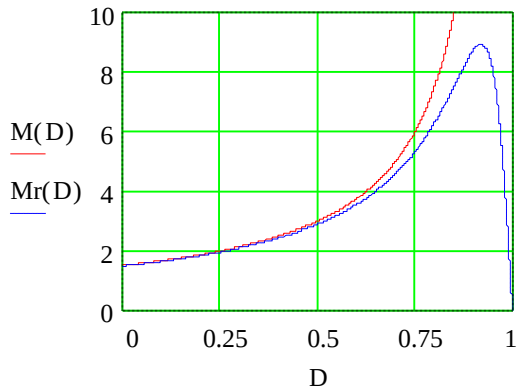

Fig.9: Ideal voltage gain *M(D)* and predicted voltage gain *Mr(D)*.

Eliminating of input diode bridge eliminates losses illustrated in Fig.1. However, it is not the only difference from traditional PFC with input rectification. Implementing four quadrant switches, see Fig.3 a, creates additional conduction losses. Clearly, expected overall benefit in efficiency is a difference between losses in the diode bridge and losses in additional MOSFET of each "ideal" switch in Fig.3.

Trade off should be more dramatic at low input voltages because of one more reason. Since input current approaches infinity when input voltage *Vg* approaches 2 diode voltage drops in case of traditional PFC, and 0V in case of new configuration: more benefit in efficiency is expected at low input voltages.

This circuit was logical to compare with traditional isolated boost with usual single MOSFET switches and diode bridge, so discussed trade-offs would be clearly illustrated. Data is presented in the next section.

VI. DESIGN OF PFC AND EXPERIMENTAL DATA.

The general boost topology can be controlled in many ways, especially popular are PWM with zero current sense (UC3852 from Unitrode) and average current control (UC3854). These integrated circuits could be used with additional circuitry to produce overlapping signals A and B in Fig.5; however another integrated circuit UCC3857 (average current control) is specifically well suited for isolated boost. Switch C is added to improve the converter performance.

There is no difference in converter operation at positive or negative halves of the line cycle, but control IC needs certain polarities of input signals to function properly. Additional circuitry was therefore used to ensure such polarity for input voltage and input current senses, as in Fig.10.

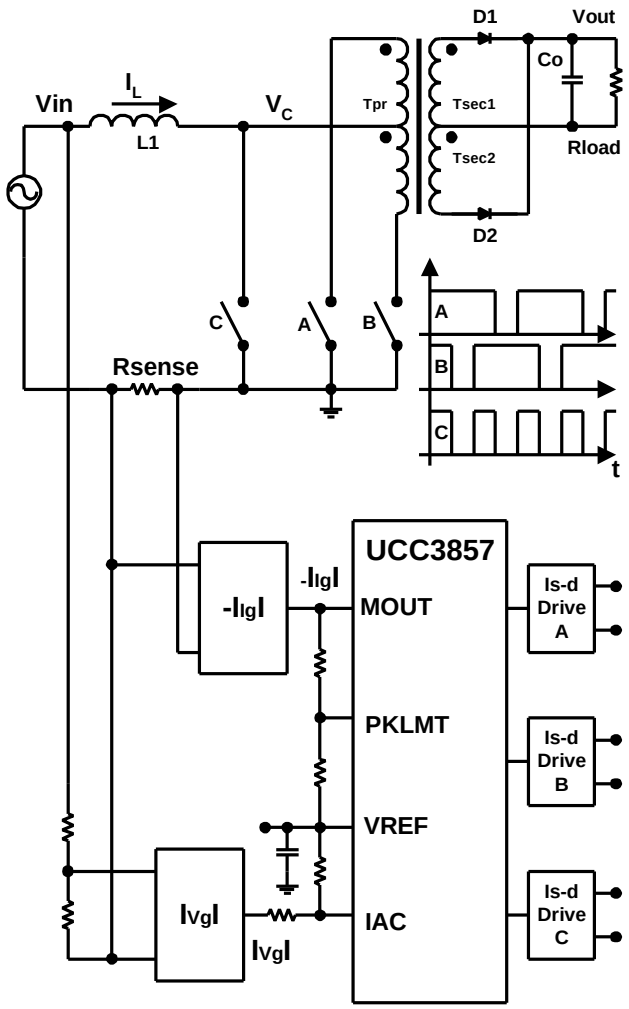

Fig.10: General schematic of new Power Factor Corrector without input rectification.

There are two absolute value circuits, one for current sense and one for input voltage sense. It was found that input called *IAC*, which senses input voltage and effectively sets the value of average current, is a current sink with some constant voltage potential. Stepping input voltage down for absolute value circuit and using respectively scaled down resistor at *IAC* input can therefore result in significant distortion of current waveform, unless bias to *Vref* is used.

Isolated drives were implemented to drive four quadrant switches. Detailed schematic is shown in Fig.10. Output voltage can be any value because of isolation transformer. It was chosen to be 160 V, so 500 Ohm load would provide 50 W output power and allow a range of low input voltages.

Exactly the same circuit was used to measure performance of traditional isolated boost with input rectification. It is important to point out, that in that case original single MOSFET switches were used to provide fair comparison with new topology.

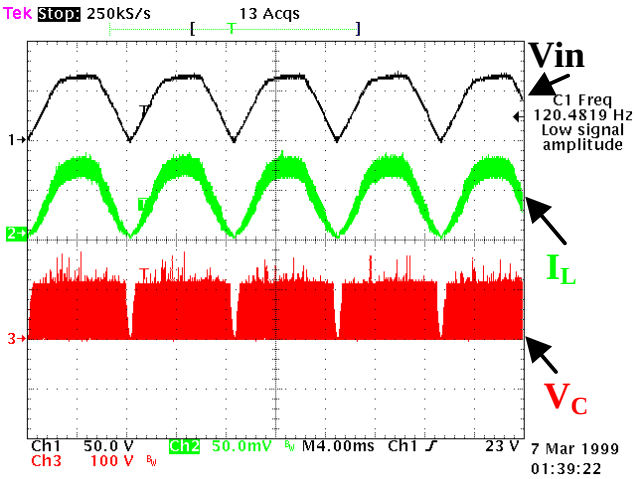

Fig.11: Waveforms for the traditional isolated boost topology. (with input rectifier). *Vg*=50Vrms, *Pout*=50W.

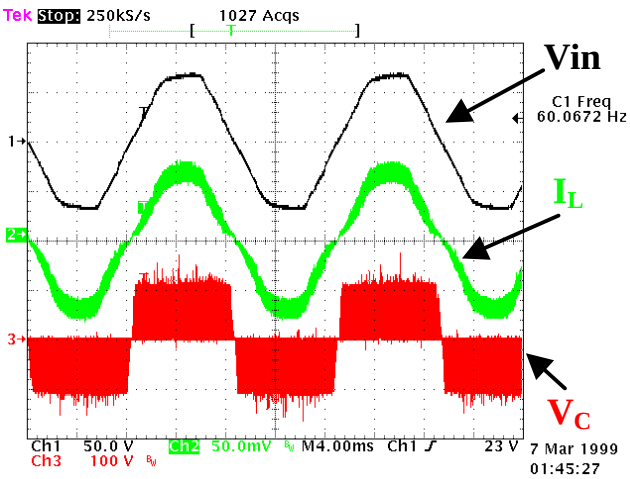

Fig.12: Waveforms for the new topology. *Vg*=50Vrms, *Pout*=50W.

Waveforms for traditional and new topologies are

shown in Fig.11 and Fig. 12 respectively. Upper trace is a voltage right before input inductor *Vin*, lower trace is inductor current I_L, and voltage of the middle point of the transformer primary V_D (voltage across switch D in Fig.7) is shown at the bottom – same way for both topologies.

Fig.13 shows measured efficiency for new (top trace) and traditional (bottom trace) topologies, for output power 50 W. New circuit clearly has better efficiency; the difference between two sets of measurements is shown in Fig.14.

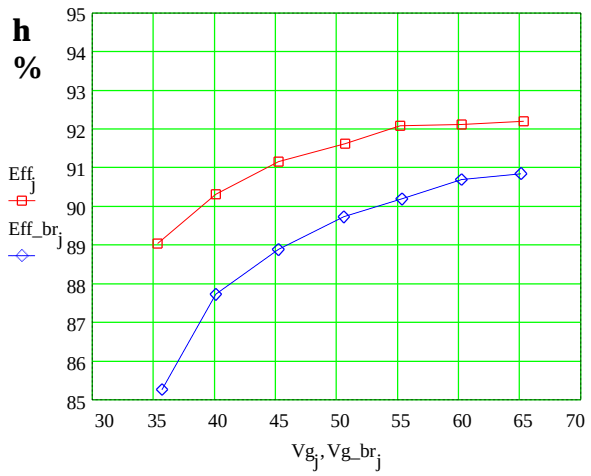

Fig.13: Efficiency measurements % vs. *Vg*.
Top trace: new topology.
Bottom trace: traditional isolated boost.

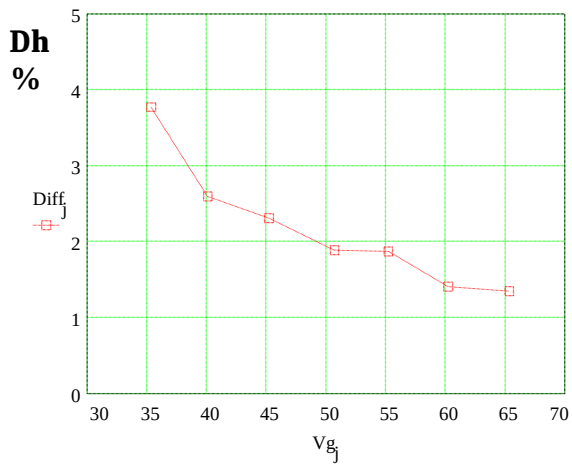

Fig.14: Efficiency advantage of the new topology, %, as a function of input voltage *Vg*.
(Difference of efficiency values shown in Fig.14).

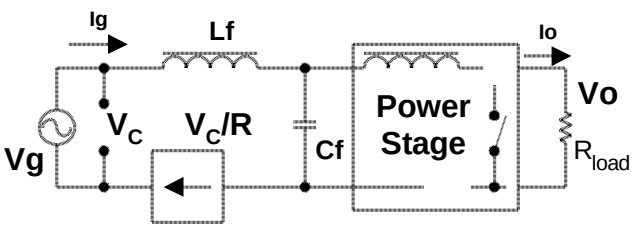

Fig.15: Incorporating input filter into PFC.

It is also necessary to point out, that the absence of input rectification allows incorporation of input filter into Power Factor Correction, Fig.15. Voltage sense *Vc* and controlled current *Vc/R* can be moved to the very input of the circuit. In other words: PFC (input current shaping) happens at the very input of the circuit, before the input filter, so the highest PF value is achieved. In this case the value of PF is restricted only by the control scheme. In addition, wider range of filter design can be implemented without concern about affecting power factor.

VII. CONCLUSION.

New approach of implementing Power Factor Conversion circuits was presented. Example circuit was analyzed, prototype was built and measured characteristics were presented.

New family of PFCs promises improved efficiency, especially at low input voltages, in comparison to traditional topologies with input rectification. The absence of input rectifier also allows including input filter into power factor corrector operation and therefore improving Power Factor. This approach also allows more freedom in input filter design.

New topologies also introduce some additional options for input filter design, EMI suppressing, etc. because of well defined connection of the power stage to power lines.

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