Power Electronics Applications To Emerging Computers and Telecommunications Systems

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Abstract - **Trends in power electronics in information systems are presented. Concepts used to achieve loss-less switching in power supplies are discussed. New power architectures, which results in fewer power conversion stages are presented along with the concepts of high frequency triport power supplies and high frequency ac distribution.**

I. INTRODUCTION

The computer, cable-TV, entertainment, consumer electronics and telecommunication industries are now entering the age of technology and business innovation to achieve new digital / fiber infrastructures. These infrastructures, currently known as 'Information Superhighway', will be capable of providing a platform for a wide range of broad band, multimedia, entertainment, communication and information services. Power electronics is an integral part of these infrastructures and has been challenged to provide cost effective, energy efficient, uninterrupted and reliable network power solutions.

Fig.1 shows a typical network diagram of the information superhighway. This information superhighway is a network of many networks namely; core networks, transport networks, and access networks. The core networks require substantially higher power than the access networks and usually powered by a centralized power plant. The power supplies used in these networks require very high efficiency and power density.

Fiber to the curb, Fiber to the home and Hybrid Fiber-Coax networks have emerged as some of the preferred approaches for distributing wide range of aforementioned services to the users. New concept such as high frequency triport UPS is presented in the paper to power these access networks.

Future designs of terra bit routers and personal computers using GHz processors for data networks require sub-voltage level power distribution at very high current (>100 A) and slew rate (>1 A/ns). A new concept of high frequency power distribution architecture for these routers and personal computer is given in the paper.

II. POWER ELECTRONICS IN CORE NETWORKS

Core networks are the high capacity, high performance and high-speed networks used to process and transport heavy traffic information in an information system. The communication equipment's used in these networks require high power with battery back-up. Fig.2 shows a typical power distribution system.

The high power (10kW-100kW) ac/dc rectifier uses modular approach in which several medium power ac/dc converters (0.5kW-3 kW) are connected in parallel. Each medium power ac/dc converter employs a power factor correction circuit followed by a dc/dc converter circuit. The output of the rectifier is connected to a battery bank to supply uninterrupted dc power to the communication equipment bay.

Each equipment bay in current designs distributes the dc power via input filters to the electronic cards used in the design of the communication equipment. This type of power architecture is commonly called 'distributed power' and is shown in Fig.4. The main requirements for the power supplies used in these systems are (a) high efficiency, (b) high power density, (c) low EMI, (d) high reliability, and (e) low cost.

In order to achieve the above requirements the power supply should be operated at very high and constant frequency and must have significantly reduced switching losses. A number of converter topologies have been reported in the literature, which may satisfy these requirements. Presented here are some of the converter topologies on which the author has direct experience and are currently either being used and/or being designed in the telecommunication systems.

A. Resonant Reset Zero Voltage Switching Forward Converter.

The forward converter topology is one of the most popular topologies used for the distributed power supplies in advanced telecommunication and computer systems. These systems require the supplies to have high power density and efficiency. Fig. 4 shows the proposed ZVS forward converter topology [1]. It has two functional sub-circuits. One is the auxiliary circuit that is drawn inside the dashed line block. The other, outside the block, is the conventional forward converter, which will be referred to as the "power circuit" hereafter.

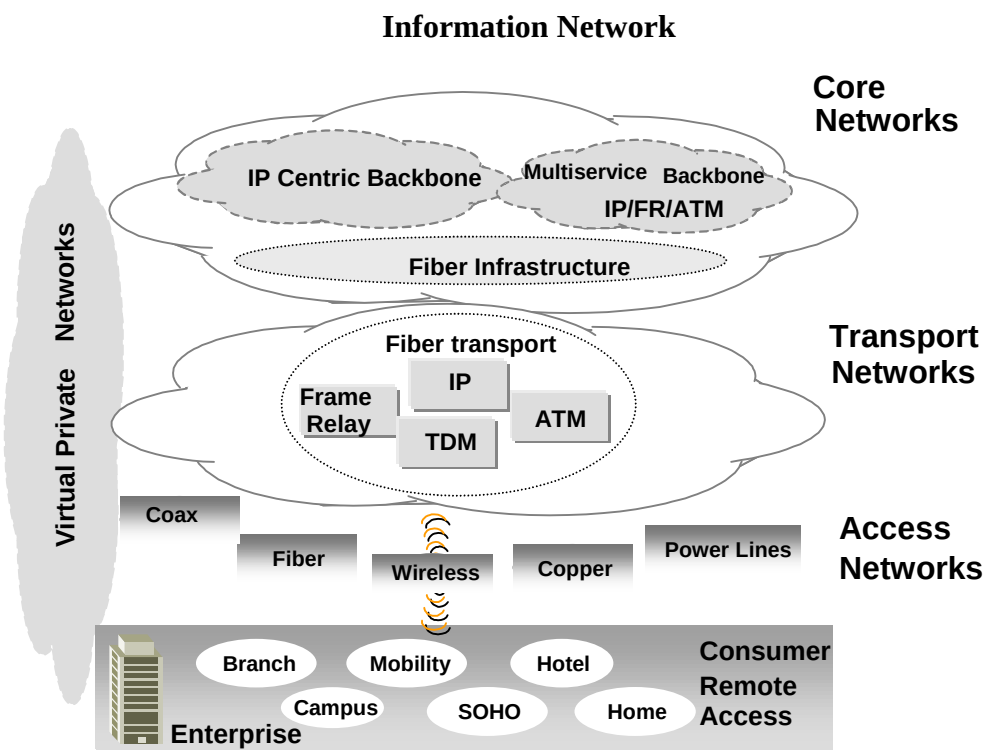

Fig.1. Information superhighway.

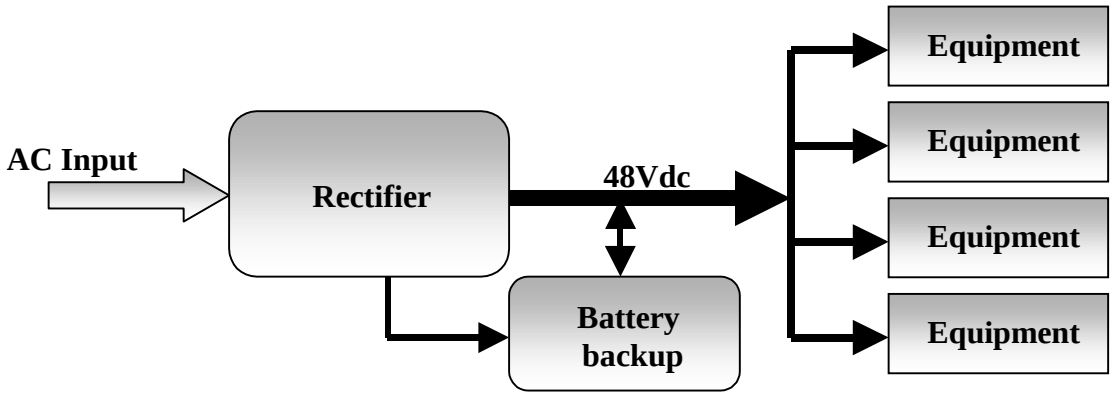

Fig.2. A typical power distribution system for core network equipment's.

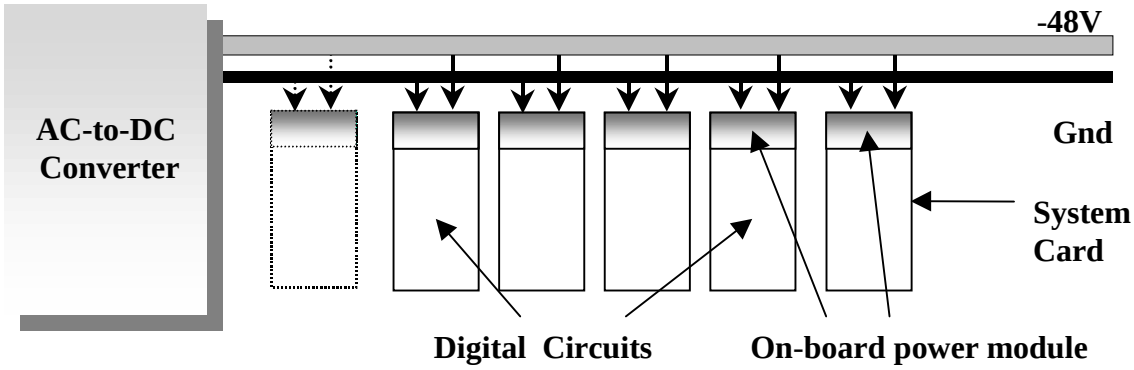

Fig.3. Distributed power architecture

The power circuit is comprised by a power transformer (T_r) with a magnetizing inductance L_m and a turns ratio of k, the main switch (Q_1), the output rectifiers (D_{o1} and D_{o2}) the output filter, L_o and C_o, and the load R_L.

The auxiliary circuit consists of the auxiliary switch, Q_2, a snubber capacitor for the main switch, C_{snb}, a current limit inductor, L_s, which is inserted into the secondary side of T_r, a resonant tank, L_a and C_a, a center-tapped auxiliary transformer, T_a, with a turns ratio of k_a, and two auxiliary diodes, D_1 and D_2.

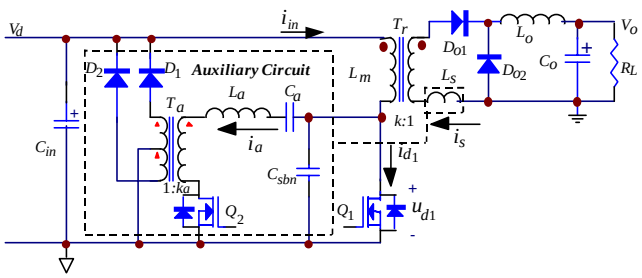

Fig.4. Resonant self-reset forward converter topology.

The advantages of the circuit topology as shown in Fig.5 are (i) both the switches of main and auxiliary circuits achieve ZVS both at turn-on and turn-off independent of the load and input voltage, (ii) the transformer is self-reset. The experimental results obtained from a prototype circuit show a typical efficiency of greater than 90% at the power level of 100W.

B. Asymmetrical Pulse Width Modulated (APWM) Resonant Converter

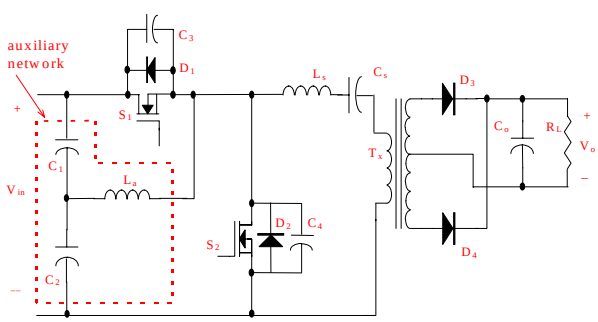

Fig.5.Resonant APWM converter topology.

Fig. 5 shows an APWM resonant DC/DC converter topology [2]. This circuit can be broken into functional blocks: the compensating network (C1, C2, La), a chopper, a series-resonant tank (Ls,Cs), a power transformer (Tx), a rectifying block (D3, D4) and the output filter. The chopper consists of the two switches (S1,S2), the two snubber capacitors (C3,C4) and two compensating diodes (D1,D2). Switches, S_1 and S_2, are controlled by two complementary gating signals. The gating signal of S_1 has a duty cycle of D and that of S_2 is 1-D. Whenever S_1 is on, the power from the source is transferred to the load and the output of the chopper sees a positive voltage of V_{in} from the source. When S_2 turns on, the source is separated from the rest of the power circuit and the output of the chopper sees the voltage across S_2 which is zero volt. The energy from the resonant components now freewheels through S_2 and supplies power to the load. By varying D, we can control the output voltage.

The advantages of the circuit topology as shown in Fig.5 are (i) both the switches achieve ZVS both at turn-on and turn-off independent of the load and input voltage, (ii) the transformer leakage energy is recovered, and (iii) the transformer is self-reset. The experimental results obtained from a prototype circuit show a typical efficiency of greater than 90% at the power level of 30W. This circuit is best choice for very high frequency operation (above 1MHz).

C. Auxiliary Commutated Full-Bridge Converter

Fig.6 shows the proposed ZVS full bridge converter topology [3]. It consists of two functional sub-circuits. One sub-circuit is a conventional full bridge converter, which is referred to as the power circuit hereafter. The other is an auxiliary network shown in the shadowed area in Fig.6.

The power circuit employs the following devices: (i) S_1, S_2, S_3, and S_4, four MOSFET switches, (ii) T_r, the power transformer with a turns ratio of k, (iii) D_1 and D_2, two rectifiers, (iv) L_o and C_o, the output filter, and (v) R_o, the load.

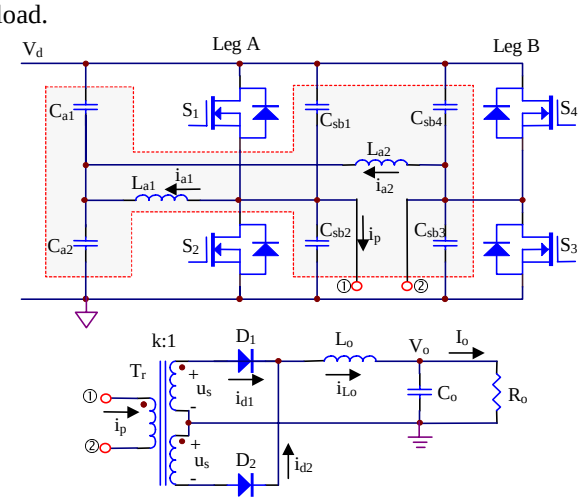

Fig.6 Auxiliary commutated full-bridge converter topology.

The auxiliary circuit is comprised by eight passive devices, i.e., (i) C_{sb1}, C_{sb2}, C_{sb3}, and C_{sb4}, four drain-to-source snubber capacitors, each across one switch, (ii) C_{a1} and C_{a2}, a capacitive voltage divider, and (iii) L_{a1} and L_{a2}, two auxiliary inductors.

Phase shift pulse width modulation is used as the control technique for output regulation in the proposed converter topology. In terms of power transfer from the input to load, the power circuit operates in almost exactly the same way as does a conventional full bridge converter, and the auxiliary circuit hardly interferes with this transfer. However, the auxiliary circuit does have significant

influences on the switching transients of the switches: it simply removes the switching losses from all the switches, at both turn-on and turn-off.

The advantage of the circuit topology as shown in Fig.6 is that all the switches achieve ZVS both at turn-on and turn-off independent of the load and input. The experimental results obtained from a prototype circuit show a typical efficiency of greater than 96% at the power level of 2kW

D. Zero Voltage Switching Boost Converter

Fig.7 shows a ZVS boost converter topology. It consists of two functional sub-circuits. One sub-circuit is a conventional boost converter, the other is an auxiliary network shown in the dashed area in Fig.7. The boost converter topology is mainly employed in designing a power factor corrected ac/dc power supply.

The auxiliary circuit is an energy recovery circuit. The energy recovery circuit consists of Lr, Cr auxiliary transformer Tx and auxiliary switch S2 and diode Dx1 Dx2

The objective of this energy recovery circuit is to achieve zero voltage switching for the main MOSFET and to eliminate reverse recovery current problem of the diode. The experimental results obtained from a prototype circuit show a typical efficiency of greater than 96% at the power level of 2kW.

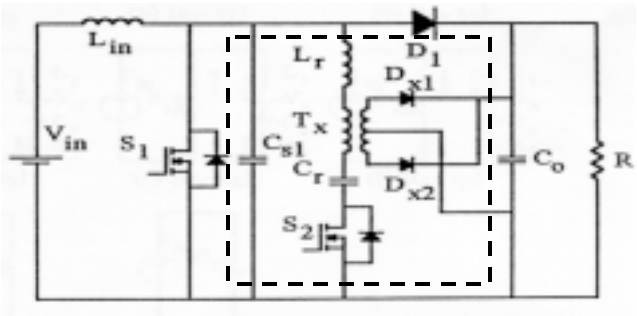

Fig.7. Zero voltage switching boost converter topology.

III. POWER ELECTRONICS IN ACCESS NETWORKS

In recent years, a number of access networks as given below have emerged for distributing a wide range of information services to the user.

1) Hybrid Fiber-Coax (HFC) Networks.
2) Fiber to the Curb (FTTC) Networks.
3) Fiber-to-the-Home (FTTH) Networks.

In order to power these networks a number of different types of uninterruptible power supplies (UPS) are required. These UPS can be classified according to the nature of input source and output load, that is, AC/AC UPS to power HFC networks [4], and AC/DC UPS to power FTTC networks and FTTH.

Although the power rating and output voltage characteristics of the above UPS are different, they have some common features in terms of isolation between input/output/batteries, high efficiency, low weight and volume, low cost and high reliability.

A common approach to design the above types of UPS either employs low frequency transformer for isolating the input or uses a high frequency link in which many cascaded conversion stages are used. This results in either bulky and heavy or low efficiency UPS. Recently, a new "High Frequency Triport" concept is introduced [5] for designing these UPS in which the isolation between the input/output/battery is provided by means of a single high frequency transformer. This results in a light and compact converter. The general block diagram of a High Frequency Triport UPS is shown in Fig.8. Based on the power requirements and input/output waveshape characteristics as determined by the applications, a number of triport configurations can be derived. This section gives three UPS configurations for (i) local powering of HFC or FTTH, (ii) network powering of FTTC, and (iii) network powering of the HFC network.

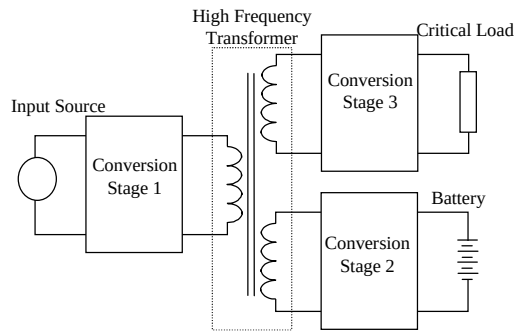

Fig.8. Generalized high frequency triport converter topology.

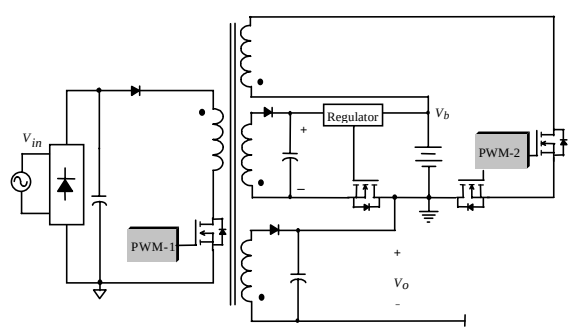

Fig.9. UPS for FTTH networks.

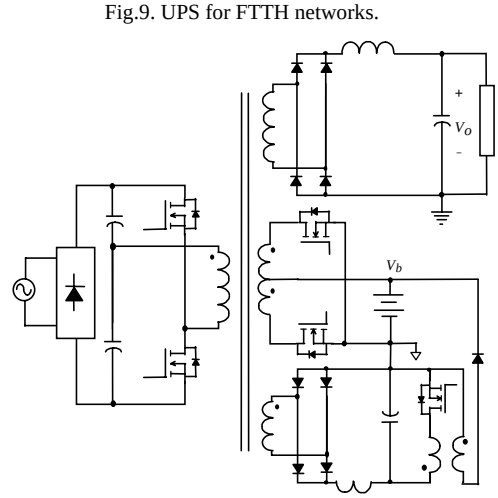

Fig.10. UPS for FTTC networks.

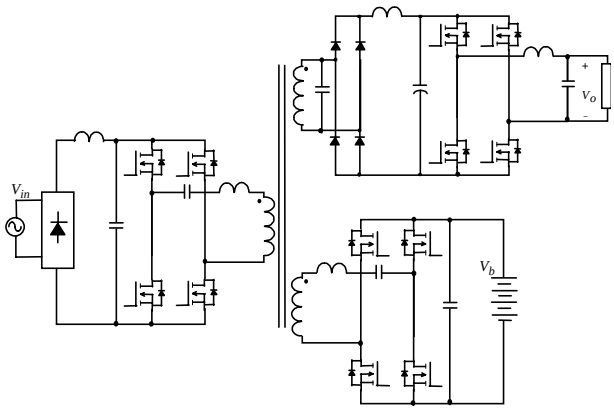

Fig.11. UPS for HFC networks.

A. UPS for Local Powering of HFC / FTTH Networks

Fig.9 shows a triport UPS topology based on a flyback converter as the power requirements for the application is low

(5W-20W). This topology has a reduced number of components. Taking into account the power required to charge the battery is low (6W), a linear regulator is used for the control of the battery. A detailed analysis and design guideline of this circuit is given in [6].

The experimental results for line-operating mode show the converter efficiency between 70 and 80% from 50% to 100% of the full load. For the backup mode the efficiency is almost 80% at full load. This confirms a high efficiency topology for both operating modes.

B. UPS for Powering FTTC Networks

The topology of Fig.10 is a good candidate for the implementation of the UPS for the FTTC. This is because the power requirement in this case is moderate (120W), and the topology of Fig.11 provides good transformer utilization and low output current and voltage ripples with a considerable low number of active switches. A detailed analysis and design guideline of this circuit is given in [4].

The performance of the UPS was evaluated experimentally. During both operation modes, the system efficiency is always above 85%, which demonstrates the good performance of the proposed topology.

In this circuit, the transient from the line-operating mode to the back-up mode and vice-versa can be virtually eliminated from the output by the proper selection of the output filter capacitor.

C. UPS for Powering the HFC Networks

In this case, the power requirement is higher, about 1100 W, and input power factor correction is needed to limit harmonic current injected into the utility grid. The implemented circuit is shown in Fig. 11. A detailed description of the operation principle of this converter can be found in [7]. The proposed UPS topology has the following merits (i) it provides ZVS operation for high frequency converter allowing operation at high frequency, (ii) provides high input power factor without dedicated power factor correction circuit, (iii) it has a high quality output waveform with flexibility in the selection of the output frequency and waveform.

The performance of the UPS was evaluated experimentally. The input power factor is closed to unity and the THD of the input current in smaller than 5% at full load. The overall efficiency of the UPS if about 87% at full load. Due the energy storage element in the output dc bus and the inverter that controls the output voltage, the output voltage is virtually unaffected by disturbances in the incoming ac line and during the switching over from the line operating mode to backup mode and vice versa.

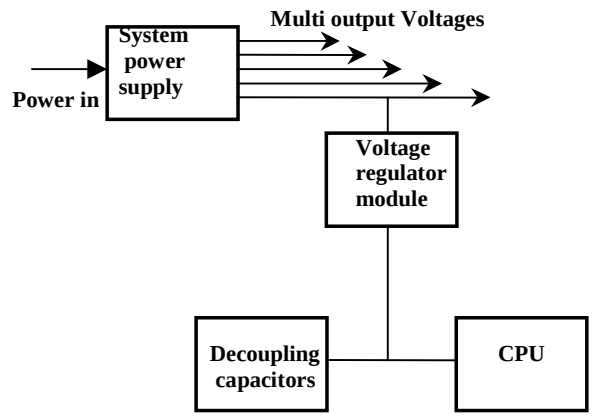

Fig.12. CPU power distribution.

V. POWER ELECTRONICS IN COMPUTERS

This section gives an overview of past, present and future development in desktop personal computer (PC) power requirements. A dramatic increase in processor speed results in an overwhelming increase in current and its dynamics (very high slew rate). This already challenging technical requirement is further magnified by voltage reduction, potentially to sub-volt levels.

In the past, there was virtually no challenge in powering computers. A multiple output very slow power supply called “Silver Box (SB)” was able to meet the requirements of every power demand. Later, as silicon development progressed, multiple voltages of lower than 3.3V were required. Voltage Regulator Modules (VRMs) were the logical solution on the processor Mother Board (MB). Today, the number of additional VRMs is increasing. In addition, a large number of decoupling capacitors are needed in proximity to the processor to meet the requirements of very high slew rate of the current. Those requirements resulted in a rapid increase in the cost of the power delivery system as well as a large reduction in the overall efficiency.

The above problems define the issues associated with

power delivery for desktop computers today and in the near future. Most stringent requirements in power delivery system are clearly related to the processor (Fig.1). The processor power delivery consists of a system power supply (SB), voltage regulator module (VRM), de-coupling capacitors, processor and distribution. The system power supply accepts the input line AC voltage and converts it into low voltage DC, usually 5V, 3.3V, or in some cases 12V. The Voltage regulator module (VRM) then re-processes this intermediate voltage into lower DC voltage (<3.3V), which is then supplied to the processor together with the de-coupling capacitors. The high current, high slew rate and tightly regulated low voltage are, however, not related only to VRM and the distribution between VRM and the processor, but involve the overall power architecture. Possible power architectures are described below.

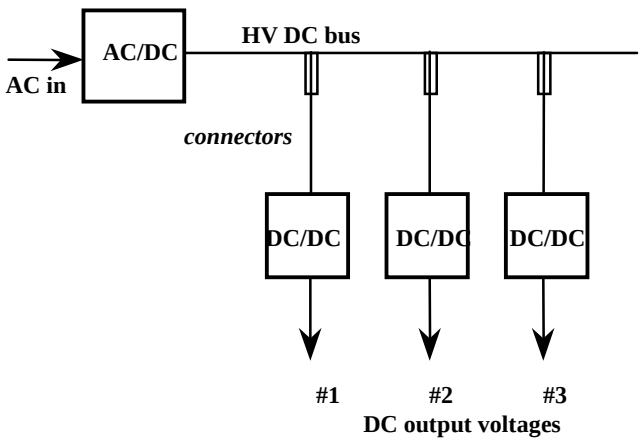

Fig.13. Low voltage power distribution for personal computer.

A. Low Voltage DC Distribution

This is a commonly employed approach today in PCs. This approach is depicted in Fig.13. Input line AC voltage is brought to SB and is converted into several low DC voltages, which are then distributed through wiring and connectors to the various parts of the computer. Most of the low voltages serve only as the input for several VRMs where these voltages are converted into even voltage levels but at higher currents. This, "traditional" approach has the following drawbacks.

- high and rapidly increasing cost
- limited performance (lower efficiency, lower di/dt)
- lower form factor

Most of the above drawbacks are direct results of duplicated power conversion stages, distribution of low voltage at high current levels, and low switching frequency. Many power supply vendors have been spending a lot of time and resources in an attempt to improve this system by adopting some of the following factors:

- Increase in switching frequency (up to 2 MHz)
- Multi-phase interleaved converters
- Sophisticated control schemes including digital
- Current step forecast along with predictive control
- Droop resistor
- Active current bypass
- Use 12VDC rather than 5V / 3.3VDC for VRMs input

The above solutions belong to a category of "incremental technology" and offer only a partial solution to the fundamental issues of powering the future generation processors. Increase in switching frequency improves the loop response and reduces slightly the size of some components. Switching frequency limit is about 2 MHz based on today's technology. In an effort to break this barrier, two or more converters are paralleled (multi-phased) and interleaved.

Sophisticated digital control usually requires a complex set of interleaved converters and may increase the dynamic performance. Current step forecast that accompanies predictive control algorithm and involves active bypass circuitry could improve dynamic performance dramatically. All these strategies work well but impact negatively on the cost, form factor and reliability due to the increased component count. An interesting impact on the performance can be observed if 12 V is used as the intermediate voltage supplying the VRMs. Clearly this improvement would be more visible if even higher voltage will be used.

B. High Voltage DC Distribution

The high voltage DC power architecture is shown in Fig. 14. In this type of distribution, a system power supply (silver box) generates only a single voltage at a much higher voltage level than the previous low voltage distribution. This system is capable of dealing effectively with most issues defined above. There are, however, two drawbacks in this architecture, namely, duplicated power conversion, and no provision to effectively deal with the negative high di/dt. It should be appreciated, however, that high voltage DC distribution has been used very successfully within the telecommunication industry for many years. In the computer industry 48VDC has been introduced recently in the high power servers domain. With increasing current levels and decreasing voltage the overall power delivery efficiency will drop. Even if this approach could efficiently deal with frequent positive current steps, it does not provide a simple solution such as "energy steering" for the negative current steps. The higher cost is still a big concern.

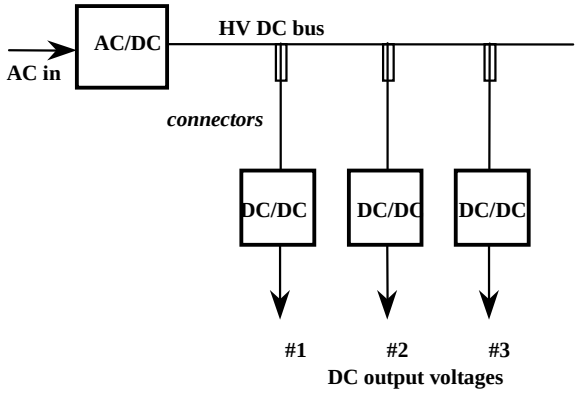

Fig.14. High voltage power distribution for personal computer.

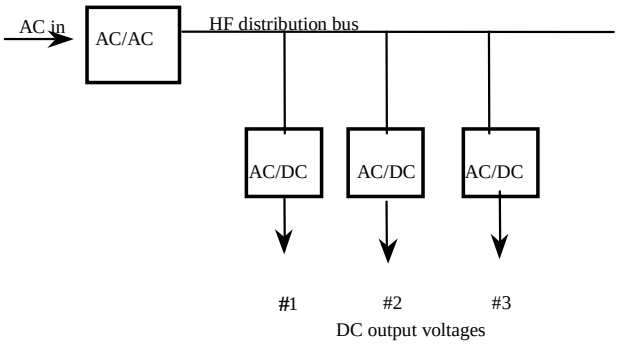

Fig.15. High frequency power distribution for personal computer.

C. High Frequency AC (HFAC) Distribution

In order to overcome most of the above problems at low cost a high frequency ac distribution system as shown in Fig. 15 is presented in this section [8]. The system power supply (silver box) generates high frequency and high voltage. The HFAC is then fed to an individual ac-dc converter (ACVRM) and converted into DC of specific parameters at the point of use. The HFAC brings the following advantages:

- Low cost
- High efficiency (80%)
- Better form factor
- Better reliability
- Active energy steering

HFAC is conceptually the simplest architecture, which deals with all power delivery issues defined above. This includes elimination of duplicated power conversions, and active energy steering without additional components.

The new generation of processors requires not only high di/dt but also very frequent current steps. The energy corresponding to the positive current step must be sourced by the power delivery system. During the negative current step however two things could happen. The energy could either be stored and or damped. Damping is technically the simplest but results in poor efficiency.

Inevitably, the efficiency for dynamic power systems must be re-defined, so that it reflects how the power delivery system deals with the frequent current changes. The efficiency must be measured under a specific frequency of specific current step(s). The frequency of those steps, their amplitude and di/dt will be part of the specification of future VRMs and power delivery systems. In HFAC, the excess energy can easily be “steered” to the high frequency bus side and be re-used when needed.

Fig. 15 shows a power distribution system in which low frequency ac (LFAC) is converted into high-frequency ac (HFAC) and distributed to various load located ac-dc voltage regulator modules (ACVRMs). The ACVRM converts the high frequency ac voltage to a desired regulated dc voltage at the load. Typical ac bus frequencies are 500KHz or 1 MHz but may be as high as 10 or 20 MHz. The high frequency distribution voltage can either be trapezoidal or sine wave in shape. We have found that a trapezoidal ac voltage wave of 60 volts peak to peak and with rise times of 50 to 100 ns (maximum) gives acceptable EMI performance. Distribution using sine wave gives the inherent dv/dt limit, however, the frequency of a sine wave would be limited to less than 4.5 MHz to limit the maximum dv/dt of a sine wave to the same value as quoted above for a trapezoidal wave.

VI. CONCLUSIONS

New converter topologies and distribution architectures for information networks have been presented. Concepts used to achieve loss-less switching in power supplies have been discussed. New power architectures, which results in fewer power conversion stages have been presented along with the concepts of high frequency triport power supplies and high frequency ac distribution.

VII. REFERENCES

[1] Y. Xi, P. K. Jain, Y.F.Liu and R. Orr, "A zero voltage switching and self-reset forward converter topology", *IEEE Applied Power Electronics Conference, Dallas,USA, March 1999.*

[2] S.Mangat, P. K. Jain, Y.F.Liu and Y. Xi, "A modified asymmetrical pulse width modulated resonant converter topology", *IEEE Power Electronics Specialists Conference, Fukuoka,Japan, May 1998.*

[3] P. K. Jain, W.Kang, H.Soin and Y. Xi, "Load and line independent zero voltage switching full-bridge converter topology", *IEEE International Telecommunications Energy Conference, San Francisco, USA, October 1998*

[4] P. Jain, H. Jin and M. Qiu, “Modeling and simulation of power distribution systems for hybrid fiber/coax network,” Proceedings of 17th International Telecommunications Energy Conference, Oct. 1995.

[5] P. K. Jain and H.Pinheiro, "High frequency triport UPS for emerging fiber networks", *IEEE International Telecommunications Energy Conference, San Francisco, USA, October 1998*

[6] M. Jain, M.Daniele and P. Jain, “A High Frequency Triport Topology for Low power DC UPS,” *IEEE Power Electronics Specialists Conference, Fukuoka,Japan, May 1998.*

[7] H.Pinheiro, P. Jain and G. Joos, “A New AC Power Supply based on Series-Parallel Resonant Converter,” *Conf. Rec. of PESC’97,* vol.1, pp. 310-316.

[8] J.Drobnik, L.Huang, P. Jain and R.Steigerwald, “PC platform power distribution system,” *IEEE International Telecommunications Energy Conference, Denmark, June 1999.*