A Family of ZVS-PWM DC-to-DC Converters for High-Input Voltage Applications

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***Abstract* – This paper analyses a familiy of isolated ZVS-PWM DC-to-DC converters based on the multilevel techniques with half of the input voltage across their switches. A comparison involving the size of reactive elements employed, stress of the semiconductor devices, number of semiconductors devices, simplicity and efficiency is made and summarised. Experimental results of a prototype designed for an output power of 1.5kW, input voltage of 600V, output current of 25A and switching frequency of 50kHz are included, in order to verify the theoretical analysis.**

I. Introduction

Considering that the designer of high-frequency high-input voltage power supplies not always will find semiconductors capable of sustaining the desired voltage, it has been studied several alternatives where only a fraction of the input voltage is applied across the switches of the converters. Among these alternatives are: the series connection of switches and the use of multilevel topologies.

In the series connection of switches the static and dynamic sharing of the voltage across the switches is quite difficult to obtain and requires specific techniques.

With this technique, everything is done to contrive all the switches to commutate at the same time. When this is achieved, the dV/dt generated at each commutation is the sum of the dV/dt generated by all the switches. Such dV/dt will induce important noise that can be dangerous for the surrounding low-level circuits [2].

Recently multilevel cells have drawn tremendous interest in the power industry [2]. They consist in a commutation cell using series-connected semiconductors in which clamping circuits ensure the voltage sharing instead of forcing the switches to commutate at the very same time. Hence, multilevel cells solve the problems of static and dynamic sharing of the voltage across the blocking switches and limits the dV/dt to standard values, reducing EMI problems.

This paper presents a family of isolated DC-to-DC converters based on multilevel techniques, presented in Fig. 1, which are controlled by pulse-width modulation featuring ZVS commutation and half of the input voltage as the maximum voltage applied across the switches.

II. Circuits Description and Principle of Operation

Converter 1 is based on the NPC (Neutral Point Clamped) multilevel inverter [4] where the clamping diodes D_{c1} and D_{c2} impose the voltage across the blocking switches. The gate signals of the switches are presented in Fig. 2 where D is the duty-cycle and T_s is the switching period.

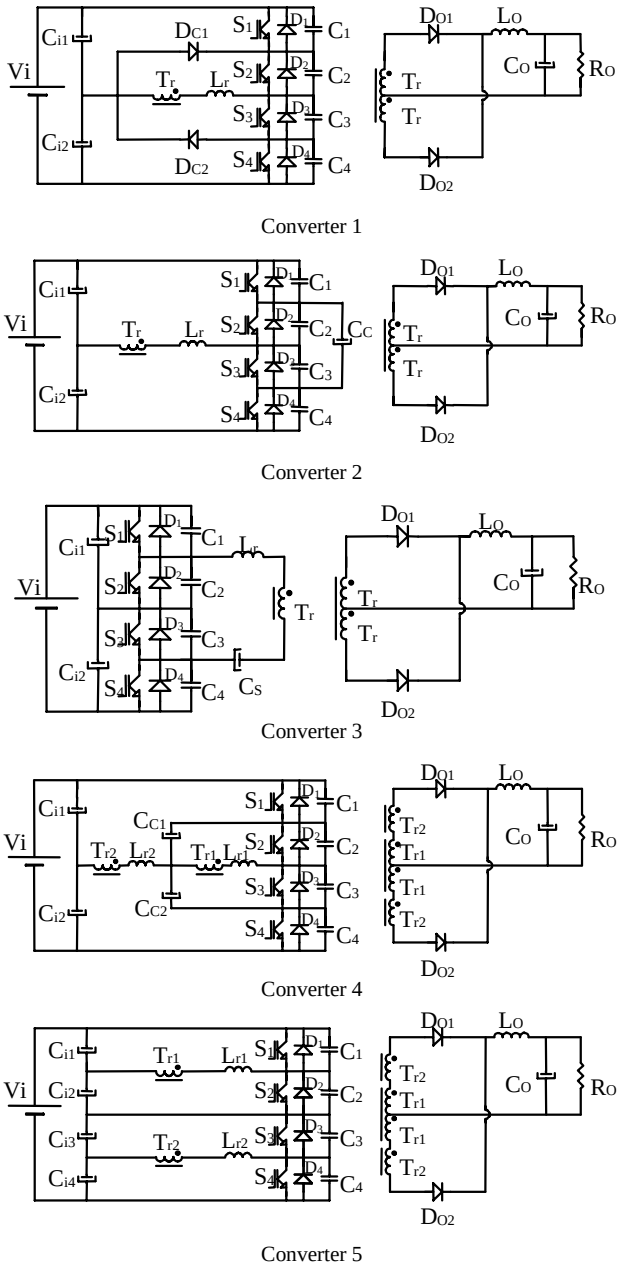

Fig. 1 - Isolated ZVS-PWM DC-to-DC converters based on multilevel techniques.

The complete analysis including operation principle, main waveforms, theoretical analysis for this converter is presented in [5].

Converter 2 is based on the flying capacitor multilevel cell [2]. With the gate signals shown in Fig. 3 the voltage across the blocking switches is imposed by the input voltage (Vi) and the voltage across the capacitor C_C, which will be equal to Vi/2. The complete analysis of this converter is presented in [3].

Converter 3 is a variation of the converter 2 with the input voltage (Vi) and the capacitors Ci_1 and Ci_2 imposing the voltage across the blocking switches. As the switches go through their cycle of switching, as presented in Fig. 4, each switch has Vi/2 applied across it while it is "off". C_s is a dc-blocking capacitor that blocks the dc voltage from being applied to the series combination L_r and T_r, allowing a three-level voltage across the power transformer T_r. For a complete analysis refer to [6].

Converter 4 consists in a cascade connection of the primary side of two half-bridge converters. One of the converters is formed by capacitors C_{i1} and C_{i2}, switches S_1 and S_4 and transformer T_{r2}. The other one is formed by capacitors C_{C1} and C_{C2}, switches S_2 and S_4 and transformer Tr_1. The voltage across the blocking switches is imposed by the input voltage (Vi) and the voltage across the capacitors C_{C1} and C_{C2}. The complete analysis of this converter can be found in [7].

Converter 5 is a series association of the primary side of two isolated half-bridge inverters with the secondary of their transformers connected in series. The voltage across the capacitors C_{i1} to C_{i4} impose the voltage across the blocking switches. The complete analysis of this converter is presented in [8].

The gate signals for converters 4 are presented in Fig. 3 and Fig. 5 respectively.

In all converters the resonant inductance Lr (or L_{r1} and L_{r2}) along with snubber capacitors C_1 to C_4 provides a resonant transition permitting zero-voltage turn-on that eliminates turn-on switching power losses. The energy stored in L_r charges and discharges the snubbing capacitors C_1 to C_4 bringing the switch voltage to zero before the switch is turned-on (zero-voltage commutation).

However, the wider the load range with zero-voltage commutation is the higher is the reactive voltage drop across resonant inductor L_r. So, a good design involves sacrificing the soft-commutation at light load, where the conduction losses are low, to obtain high efficiency at full-load.

Capacitors C_1 to C_4 also provide capacitive turn-off snubbing reducing the commutation losses.

The diodes D_1 to D_4 conduct inverse-polarity current and clamps the switch at a reverse voltage (–1 V).

The transformer T_r (or T_{r1} and T_{r2}) provides galvanic isolation and voltage transformation between the source and the load.

The output stage of the converters is formed by the association of the secondary windings of the transformers with rectifiers D_{o1} and D_{o2} and an output filter composed of the inductor L_o and capacitor C_o.

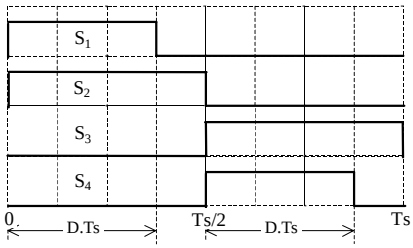

Fig. 2 - Gate signals for converter 1.

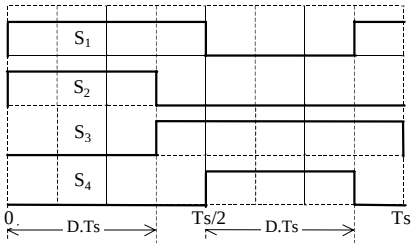

Fig. 3 - Gate signals for converter 2 and 4.

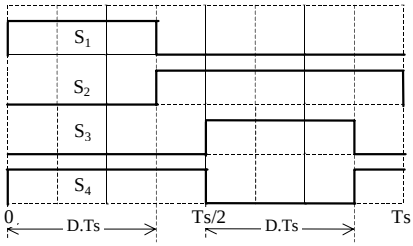

Fig. 4 - Gate signals for converter 3.

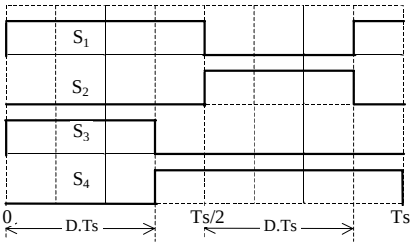

Fig. 5 - Gate signals for converter 5.

IV. Design and Experimental Results

In order to compare experimentally the behaviour of the converters, five prototypes were built with the input data presented in Table I.

The design procedures of the converters studied in this paper are presented in [4], [5], [6], [7] and [8].

Table I
Input Data

Input voltage - Vi (V)	600
Output voltage – Vo (V)	60
Output power – Po (kW)	1.5
Switching frequency – fs (kHz)	50
Input voltage ripple - ΔVi (V)	15
Output inductor ripple - ΔIo (A)	2.5
Output voltage ripple - ΔVo (V)	0.06
Clamping capacitor voltage ripple - ΔV_{Cc} (V)	3
Minimum ZVS load range (%)	30-100
Maximum duty-cycle – D_{max}	0.4

TABLE II
CONVERTER COMPONENTS

COMPONENT	CONVERTER				
	1	2	3	4	5
M_1-M_4	IRFP460 - 500V, 20A (Harris)				
L_r - L_{r1} - L_{r2}	16μH - ferrite core E42/15 - IP12 (Thornton)		20.5μH - ferrite core E42/15 - IP12 (Thornton)	8μH - ferrite core E30/7 - IP12 (Thornton)	
C_{i1} - C_{i2} - C_{i3} - C_{i4}	3μF/400V - polyester (Icotron)				
C_c - C_{c1} - C_{c2} - C_s	-	7μF/400V - polyester (Icotron)			
D_{c1}-D_{c2}	MUR840 400V, 8A (Motorola)	-			
T_r - T_{r1} - T_{r2}	2 ferrite cores E65/26 - IP12 (Thornton) Primary: 17 turns - 22AWG Secondary: 10 turns center tapped – 22AWG			Ferrite core E65/39 - IP12(Thornton) Primary: 17 turns - 22AWG Secondary: 10 turns center tapped - 22AWG	
D_{o1} - D_{o2}	MUR1560 - 600V, 15A (Motorola)				
D_g	MUR140 - 400V, 1A (Motorola)				
C_g	10nF/400V - polypropylene (Icotron)				
R_g	24kΩ/5W				
L_o	89μH - ferrite core E55/21 - IP12 (Thornton)				
C_o	220μF/100V - electrolytic (Icotron)				

The power stages of the converters implemented are shown in Fig. 5,7,9,11,and 13. The components used are presented in Table II.

The total resonant inductance is composed by the leakage transformer inductances and the external inductance L_r, yielding for each converter 24μH.

The MOSFET's body diodes were used for D_{1-4} of Fig.1, and the MOSFET's C_{oss} capacitances (480 pF) were used for C_{1-4}.

Experimentally results of an output power Po of 1.5 kW, output current Io of 25 A, input voltage Vi of 600 V and switching frequency fs of 50 kHz are shown in Fig. 6, 8, 10, 12 and 14.

The figures present, for each converter, the three-level voltage, the current through the resonant inductor and the switches voltage and current. For each case the duty-cycle was set in order to obtain output voltage Vo equal to 60 V for full load (25 A). All the observed waveforms agree well with the theoretical waveforms.

It is important to emphasise that the peak voltage across the switches, for all the prototypes, is 300 V, half of the 600 V dc input voltage. All the converters present similar switches voltage and current waveforms and zero-voltage switching.

The output voltage as function of the load current of the converters for Vi equal to 600 V and constant duty-cycle is presented in Fig. 15. The output voltage decreases with an increase of the output current due to the reduction of the effective duty-cycle, caused by the amount of reactive power that circulates in the circuit.

Fig. 16 shows the measured efficiency of the power circuits as a function of the output current for constant input voltage equal to 600V and constant duty-cycle. In general, the measured value at full load (25 A) is above 92%. The main source of losses are diode and MOSFET conduction losses, magnetic and snubber losses. The switching losses at full load are practically zero due to zero-voltage turn-on and capacitive turn-off snubbing.

The efficiency for all the converters clearly decreases for load currents lower than 5 A, when the ZVS commutation is lost and the converter starts to operate with hard-switching.

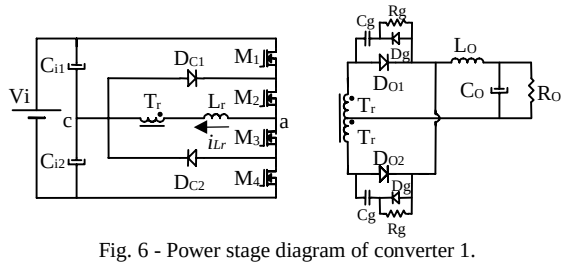

Fig. 6 - Power stage diagram of converter 1.

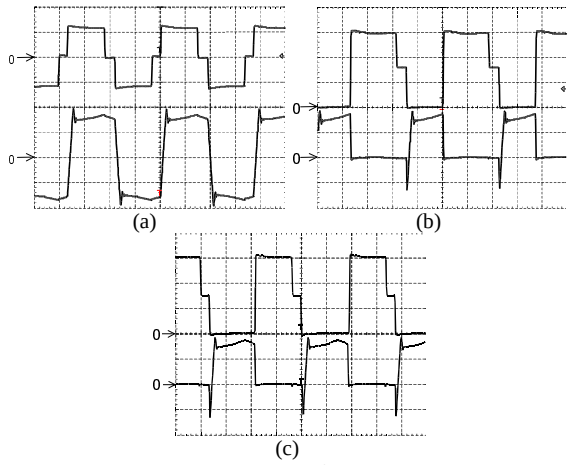

Fig. 7 - Experimental waveforms - converter 1.
(a) upper trace: voltage v_{ac} (250 V/div. 5μs/div.)
lower trace: current i_{Lr} (5 A/div. 5μs/div.)
(b) upper trace: voltage drain-to-source v_{DS1} (100 Volts/div. 5μs/div.)
lower trace: drain current i_{D1} (5 A/div. 5μs/div.)
(c) upper trace: voltage drain-to-source v_{DS2} (100 Volts/div. 5μs/div.)
lower trace: drain current i_{D2} (5 A/div. 5μs/div.)

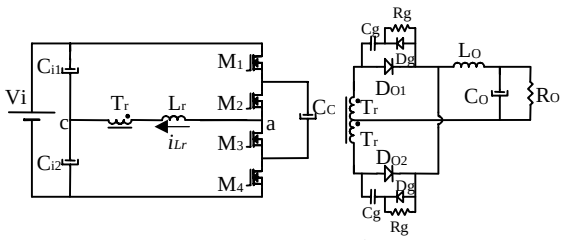

Fig. 8 - Power stage diagram of converter 2.

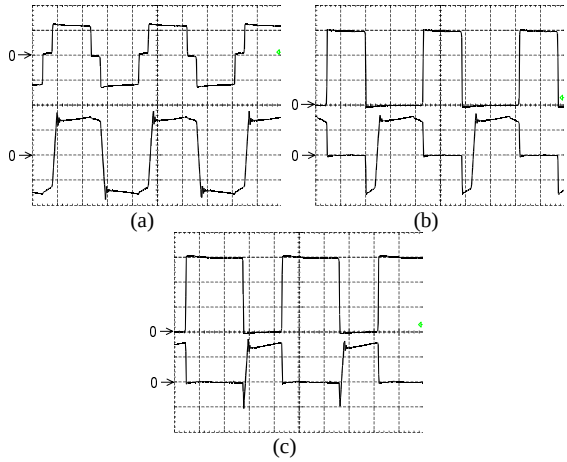

Fig. 9 - Experimental waveforms - converter 2.
(a) upper trace: voltage v_{ac} (250 V/div. 5µs/div.)
lower trace: current i_{Lr} (5 A/div. 5µs/div.)
(b) upper trace: voltage drain-to-source v_{DS1} (100 Volts/div. 5µs/div.)
lower trace: drain current i_{D1} (5 A/div. 5µs/div.)
(c) upper trace: voltage drain-to-source v_{DS2} (100 Volts/div. 5µs/div.)
lower trace: drain current i_{D2} (5 A/div. 5µs/div.)

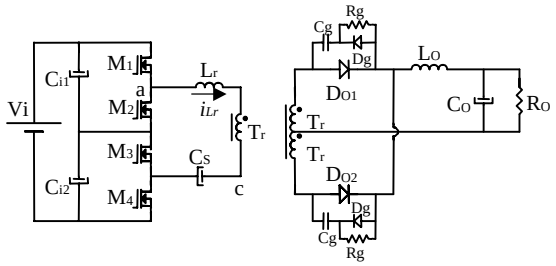

Fig. 10 - Power stage diagram of converter 3.

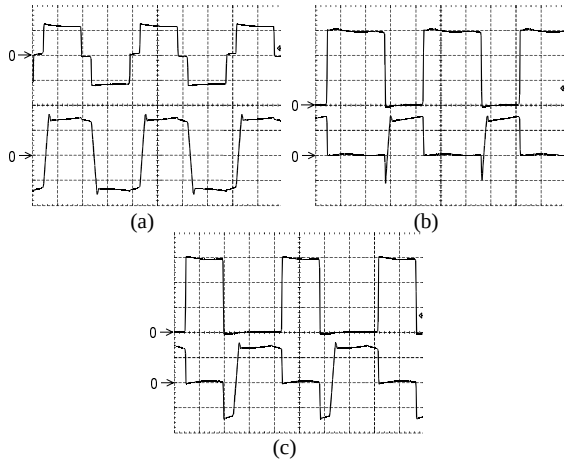

Fig. 11 - Experimental waveforms - converter 3.
(a) upper trace: voltage v_{ac} (250 V/div. 5µs/div.)
lower trace: current i_{Lr} (5 A/div. 5µs/div.)
(b) upper trace: voltage drain-to-source v_{DS1} (100 Volts/div. 5µs/div.)
lower trace: drain current i_{D1} (5 A/div. 5µs/div.)
(c) upper trace: voltage drain-to-source v_{DS2} (100 Volts/div. 5µs/div.)
lower trace: drain current i_{D2} (5 A/div. 5µs/div.)

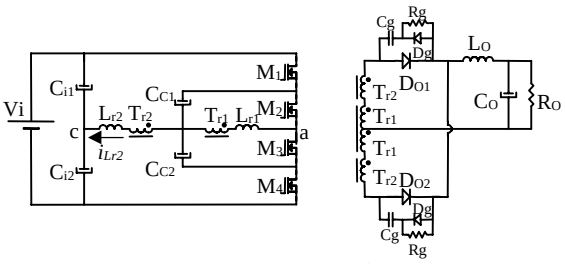

Fig. 12 - Power stage diagram of converter 4.

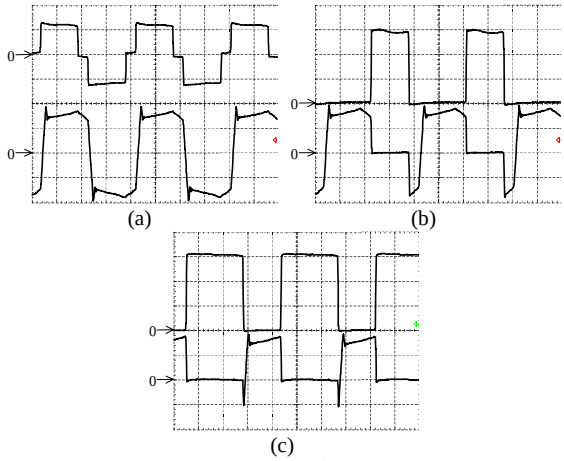

Fig. 13 - Experimental waveforms - converter 4.
(a) upper trace: voltage v_{ac} (250 V/div. 5µs/div.)
lower trace: current i_{Lr2} (5 A/div. 5µs/div.)
(b) upper trace: voltage drain-to-source v_{DS1} (100 Volts/div. 5µs/div.)
lower trace: drain current i_{D1} (5 A/div. 5µs/div.)
(c) upper trace: voltage drain-to-source v_{DS2} (100 Volts/div. 5µs/div.)
lower trace: drain current i_{D2} (5 A/div. 5µs/div.)

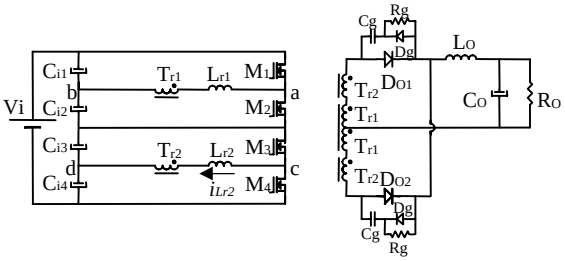

Fig. 14 - Power stage diagram of converter 5.

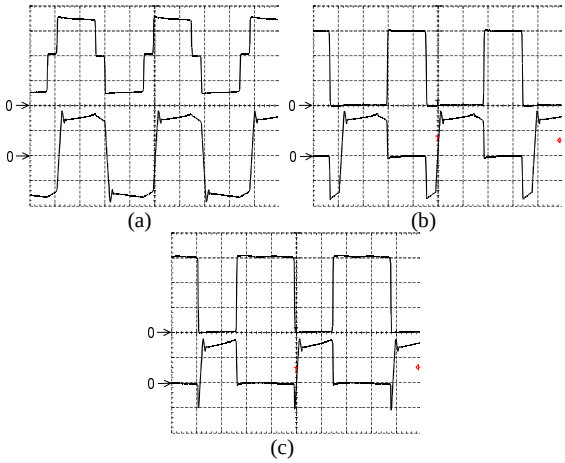

Fig. 15 - Experimental waveforms - converter 5.
(a) upper trace: voltage $v_{ab}+v_{cd}$ (250 V/div. 5µs/div.)
lower trace: current i_{Lr1} (5 A/div. 5µs/div.)
(b) upper trace: voltage drain-to-source v_{DS1} (100 Volts/div. 5µs/div.)
lower trace: drain current i_{D1} (5 A/div. 5µs/div.)
(c) upper trace: voltage drain-to-source v_{DS2} (100 Volts/div. 5µs/div.)
lower trace: drain current i_{D2} (5 A/div. 5µs/div.)

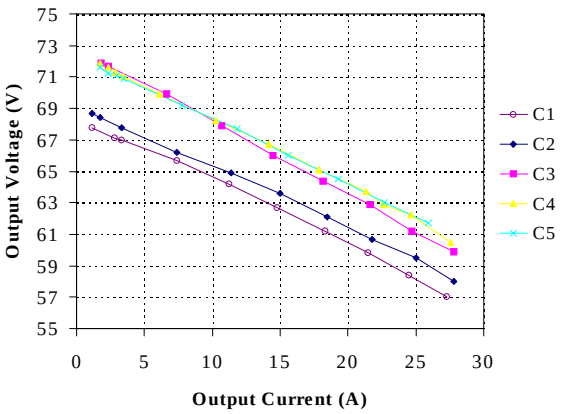

Fig. 16 - Output voltage as a function of output current.

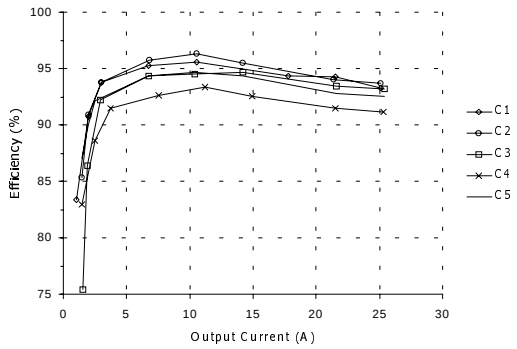

Fig. 17 - Efficiency as a function of output current.

IV. Analysis

A. Semiconductor Devices and Heatsinks

Table III presents the number of active switches and power diodes employed by each converter along with their voltage and current stress.

It can be noticed that all converters use the same number of active switches and converter 1 employs more power diodes than the others.

From the point of view of switches stresses, all the converters present the same results, with the same peak voltage across the switches (half of the input voltage) and the same volume of heat-sinks.

B. Transformers and Inductors

From Table IV, one can observe that the converters based on the association of converters, which employ two transformers, have a volume of their magnetic elements greather than the volume of magnetics used in the converters based on NPC and flying capacitor cells.

On the other hand, the use of two transformers can be interesting for high power applications, when the power processed can be naturally shared between the transformers.

C. Capacitors

Table V presents the number of capacitors, and their capacitances, used by the converters studied.

Converter 1 presents the lower volume of capacitors since its input capacitors are similar to those specified to the other converters, and there is no need of clamping capacitors.

Converter 5 presents the higher value of capacitance, however as the capacitor voltage specification is lower, it can be said that the total capacitor volume of this converter will be equivalent to those of the other converters.

In general, for high-frequency applications capacitor clamping is more suitable because the total amount of capacitance required can be decreased proportionally with the switching frequency.

D. Efficiency and ZVS Load Range

The efficiency measured for the converters are similar, with converters 4 and 5 presenting lower efficiency at full load in comparison with the other converters. This can be explained by the transformer core losses of converters 4 and 5 that are higher.

Considering the ZVS load range, converter 1 presents larger ZVS load range than the others.

V. Conclusions

This paper presented a family of isolated ZVS-PWM DC-to-DC converters suitable for high-input voltage applications.

A comparison involving the size of reactive elements, stress of semiconductor devices, number of semiconductor devices, and efficiency were made and summarized. Experimental results were presented, in order to verify the theoretical results.

The five topologies presented similar characteristics, with slight differences among them.

A choice of the best alternative depends on the application where the converter will be employed. In general, for an application of high power and high frequency the converter 2, based on the flying capacitor cell, seems to be more appropriate because presents high efficiency, no need of extra diodes as the converter based on the NPC cell, less volume of magnetics in comparison to converters 4 and 5, that needs two transformers, and can be naturally extended for more than three-levels, allowing its use for higher input voltage levels.

VII. References

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TABLE III
SEMICONDUCTORS DEVICES AND HEATSINKS

CONVERTER	C1	C2	C3	C4	C5
Active switches	4				
Power diodes	4	2			
Peak voltage - V_{Smax}	300V				
I_{S1rms}	4.83A	5.48A	4.83A	5.48A	
I_{S2rms}	5.48A	4.83A	5.48A	4.83A	
I_{S3rms}	5.48A		4.83A	5.48A	
I_{S4rms}	4.83A		5.48A	4.83A	
Thermal resistance R_{thha} (1)	1.92 °C/W				

(1) thermal resistance hetasink to ambient for two switches in one heatsink

TABLE IV
TRANSFORMERS AND INDUCTORS

CONVERTER	C1	C2	C3	C4	C5
Number of transformers	1			2	
Transformers area product (2)	22.773 cm^4			14.233 cm^4	
Total core volume of the transformers	156,4 cm^3			234,6 cm^3	
Number of resonant inductors	1			2	
Resonant inductors area product	0,921cm^4			0,426cm^4	
Total core volume of the resonant inductors	17,6 cm^3			8 cm^3	
Number of output filter inductor	1				
Output filter inductor area product	7,75cm^4				
Total volume of output filter inductor	42,5cm^3				

(2) Ap=Ac.Aw where: Ac = core effective area (cm^2) ; Aw = window area (cm^2) – for each transformer

TABLE V
CAPACITORS

COMPONENT	CONVERTER				
	C1	C2	C3	C4	C5
Input capacitors	2	2	2	2	4
Capacitance	2μF	2,5μF	0,5μF	2,5μF	7μF
Peak voltage	300V				180
Clamping or series capacitors	-	1	1	2	-
Capacitance	-	5μF	7μF	5μF	-
Peak voltage	-	300V		180V	-
Output filter capacitor	1				
Capacitance	10μF				
ESR	0,24Ω				
Peak voltage	60V				

TABLE VI
EFFICIENCY(3)

	CONVERTER				
	C1	C2	C3	C4	C5
Therorectical efficiency	94,2%			93,8%	
Experimental efficiency	93%	93,7%	93,2%	92%	92,5%
ZVS load range	20-100%	23,3-100%			

(3) full load