PWM CONTROL FOR PARALLEL CONVERTERS IN THE CURRENT SHARING MODE

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Abstract - This paper presents a new suitable approach for current sharing control in the parallel DC/DC converters operation. In order to investigate the validity and quality of the proposed control, two Buck converters with different input voltage and different output filter inductors are studied. Proposed Topology, design procedure, simulation and experimental results are presented in this paper.

I - INTRODUCTION

One of the numerous advantages of current mode control is the ability to easily parallel several power supplies for increased output power.

Many power supply manufacturers have found it economically feasible to make standard modular power supplies which are easily paralleled for higher current applications. If special provisions are not made to equally distribute the load current among the paralleled supplies, then one or more units will hog the load current leaving the other units essentially idle. This results in greater thermal stresses on specific units and a reduction in the system reliability. For example, reliability predictions will indicate that a component operating at 50 degrees above ambient will have one-sixth the lifetime of the same component operating at 25 degrees above ambient [1].

There are many techniques of current mode control to parallel converters and one can put them in parallel with just one module or various modules. One of various problems found in parallel converters is the current rise control in both converters.

The prerequisites for parallel operation are few in number, but important to insure proper operation. First, each power supply module must be current mode controlled, and capable of supplying its share of the total output power. All modules must be synchronized together to obtain approximately the same currents value at each converter and avoid the current stresses at one of them.

II - LOAD SHARING STRATEGIES

There are a number of schemes to achieve load sharing [1], [2], [3], [7], [8] and [9]. Among these, stand out the following ones:

0 The Droop Method

The simplest method to load sharing is referred to as the droop method. It is an open loop technique which programs the output impedance of the power supplies to obtain load sharing. This method exhibits very poor current sharing at low currents and improve at higher currents, but can still have large current imbalances between supplies. An example of this method is shown in Figure 1 where as the individual currents increases, the feedback voltage will decrease.

The disadvantages to the droop method are: degradation of load regulation, each module must be individually tweaked to achieve good current sharing, and difficulty in current sharing between parallel modules with different power ratings.

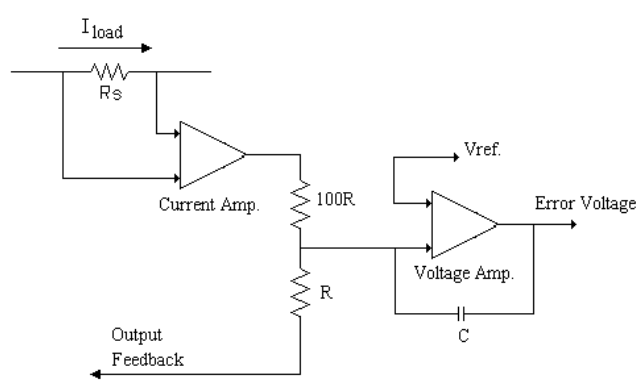


Figure 1 - The Droop Method

B. Average Current Method

For automatic current sharing no external controller is required and a single share bus interconnects all the supplies. This requires an adjustment amplifier that compares a current signal from the share bus to the individual units current, and adjusts the reference of the voltage amp until equal load current distribution is achieved.

The Average Current Method is a patented technique where each power module's current monitor drives a common share bus via resistor, as shown in Figure 2.

The adjust amplifier will sense if there is a differential across the resistor, equating to a load current imbalance, and adjusts the reference accordingly. The node where all resistors connect is a representation of the average load current contribution. While this scheme performs accurate current limit, causing the share bus to be loaded down and the output voltage to regulate to the lower adjust limit. A similar failure mode will exist if the share bus is shorted or if any unit on the share bus is inoperative.

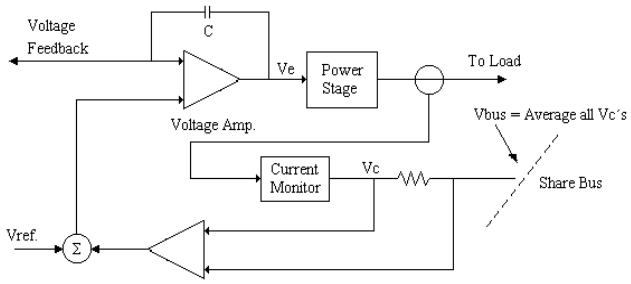


Figure 2 - Average Current Method

C. Proposed Approach to Current Sharing Control

In order to overcome the disadvantages cited above, this paper presents an approach to current sharing control. Figure 3 shows the block diagram that is a representative of the proposed idea.

Can be observed that the current mode control is able to be applied for more than just two parallel converters. Note that the sample of output voltage is the same to all of them. It can be seen at electric's theory. Although, the current is not the same to all of them, by the impedance characteristics of each converter. The proposed approach showed bellow operates fine sharing the currents.

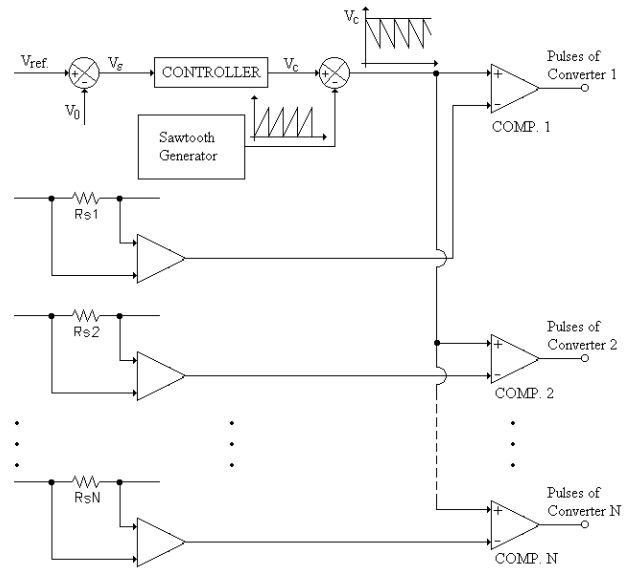


Figure 3 - Current Control Block Diagram

III - PROPOSED TOPOLOGY

As can be seen, the Figure 5 shows the Proposed Topology with the control circuit used in this project. Now, will be made an explanation based on the figure presented.

Take a sample of the output voltage, at node 3. This sample goes to block U1 and is compared with the reference signal, pass by an integrator and results in the Vc (control signal). U11 is responsible to the short circuit protection. Blocks U3 and U17 are responsible to force the maximum duty cycle equal to 0.5 and they work like buffers.

The blocks U0 and U12 are responsible to current sample of each converter. U5 and U13 have a high frequency filter to avoid an unwished oscillations which disturb the good work of the converters and they work like buffers.

The block U2 is the locate where plus the control signal to the sawtooth wave. The output signal of it, node 116, goes to blocks U4 and U18 (comparators). They compare the control signal plus the sawtooth wave with the current signals or the maximum duty cycle signal. Diodes present at the output of the operational amplifiers are responsible to observe that only the higher signals, at nodes 112 and 315, will be compared varying, with it, the duty cycle. The output signals of U4 and U18 are, respectively, D1 and D2 (duty cycle).

Figure 4 shows the control signal with sawtooth wave. Can be observed that the amplitude of sawtooth wave is shorter than amplitude of control signal. Thus, the signals variations of both of them (converters), into the sawtooth wave will provoke a small current error between the converters. At the load sharing strategies, the strategies *A* and *B* have disadvantages when one of the converters hog most of the load current. In this strategy, the current are always being monitored and the error is small, for high load and be higher for light load.

It can be seen in Figure 4. For high load, the V_c is greater than the amplitude of sawtooth wave. Otherwise,

for light load, the amplitude of sawtooth wave make difference on the V_c signal and you have one current greater than another at the end of the process.

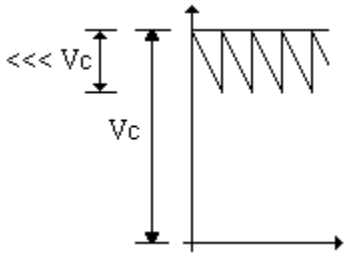


Figure 4 - Control signal with sawtooth wave

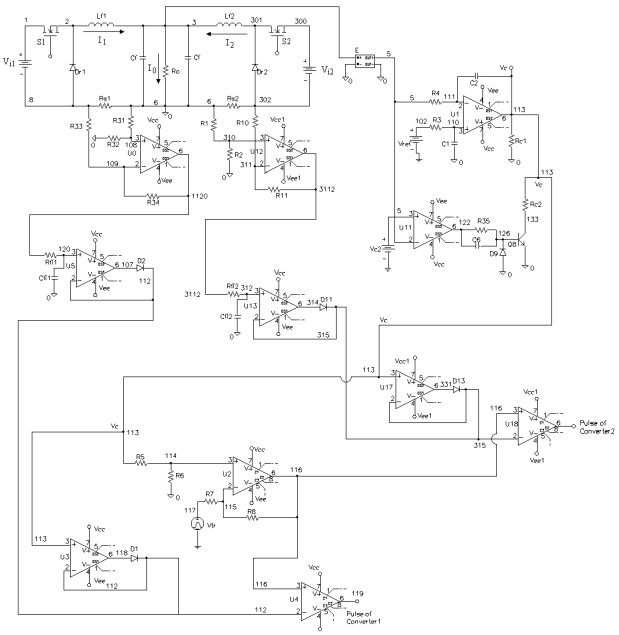


Figure 5 - Parallel Buck converters operating in the sharing current mode including the proposed control circuit.

IV - SIMULATION AND EXPERIMENTAL RESULTS

In order to investigate the validity and quality of this proposed approach, Parallel Buck converters shown in Figure 5, operating in the sharing mode control was studied by simulation and experimental.

The simulation parameters are:

V_{i1} = 110V; V_{i2} = 120V; L_{f1} = 340μH; L_{f2} = 300μH; R_0 = 12Ω; R_{s1} = 0.01Ω; R_{s2} = 0.01Ω;

$V_0 \cong$ 50V; F_s = 50kHz.

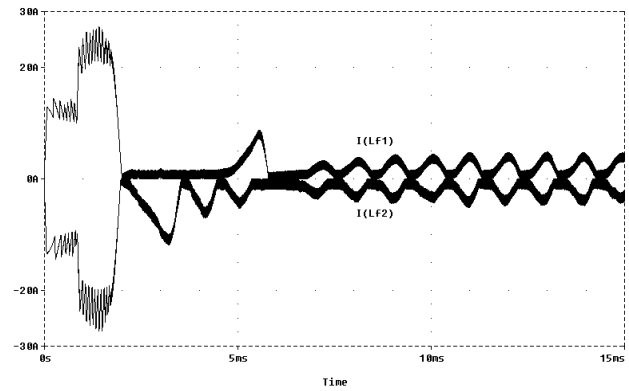
Due to the visualization of the system response and the time of simulation, different values to filter capacitor were used. The filter capacitor has two values on the simulation: C_f = 1000μF (without disturbance) and C_f = 10μF (with disturbance).

Figures bellow shows the waveforms obtained by simulation for Parallel Buck converter of Figure 5. Note that deliberately L_{f1} and L_{f2} have been taken different and, V_{i1} and V_{i2} have different values too.

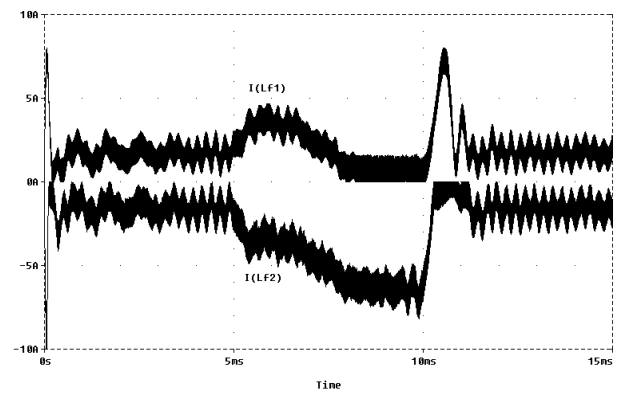
To make simulation, a disturbance was added to the reference signal at block U1 in order to verify the system response. This disturbance is a square wave which oscillates to 6 voltage at 5ms and goes back to 4 voltage at 10ms. The simulation without perturbation has a reference signal at 5V. It was made a simulation without perturbation to compare the results.

At experimental results, the reference signal was a square wave with 1kHz varying between 4 - 6 voltages.

The figures below shows it.

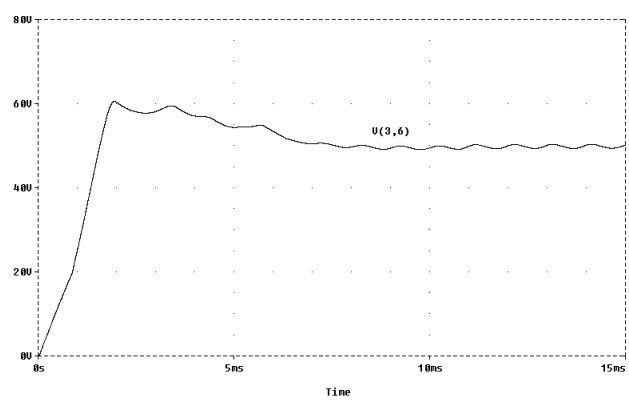


(a)

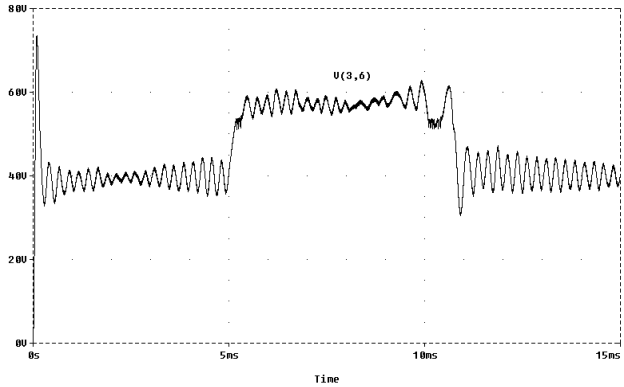


(b)

Figure 6 - Transient response of the I_1 and I_2 on the filter inductors L_{f1} and L_{f2} , respectively.
(a) Without disturbance and (b) With disturbance.



(a)



(b)

Figure 7 - Transient response of the output voltage (V_0 = V(3,6)).
(a) Without disturbance and (b) With disturbance.

The voltage with disturbance oscillates about 40V (0 to 5ms and 10ms to 15ms) and goes to 60V (5ms to 10ms). The reference signal is responsible to determine the voltage stabilization value.

The duty cycles of each converter in working mode are different between themselves. They depend on the current of each converter. Sometimes, they can be equal.

As can be seen, despite different values of V_{i1} and V_{i2}, L_{f1} and L_{f2}, the proposed Current Mode Control provides an operation sharing almost the same current values for both converters. They are symmetrical because the MicroSim_7.1© toke I_{Lf2} inverted. The simulation has presented as predicted. The experimental results are near closing the simulation results.

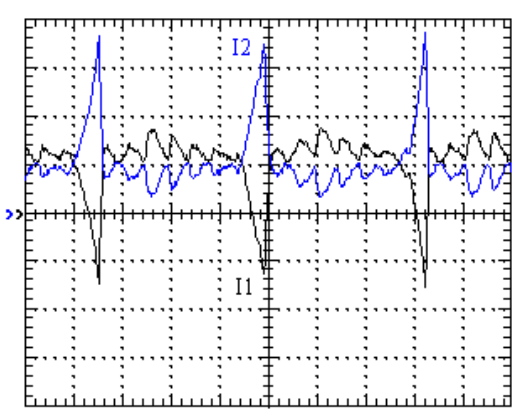
Now, to the experimental results the following parameters were used:

L_{f1} = 340μH; L_{f2} = 300μH; C_{f1} = 1000μF; C_{f2} = 1000μF;

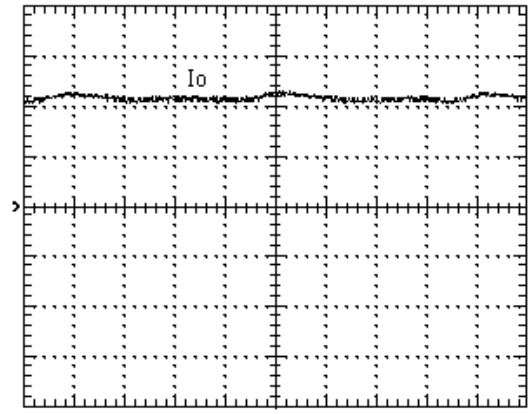
$R_0 \cong 12\Omega$; $R_{s1} \cong 0.01\Omega$; $R_{s2} \cong 0.01\Omega$; $V_0 \cong 56V$; F_s = 50kHz.

The lecture of amperimeter were: I1 ≈ 2.20A and I2 ≈ 2.15A.

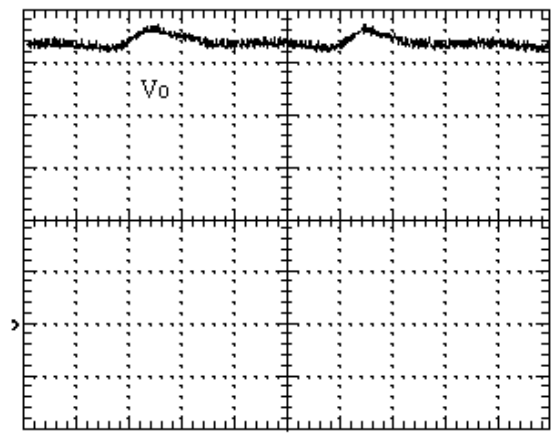
The figures bellow shows the experimental results.



(a) 2A/div (vertical) 2.5ms/div (horizontal)



(b) 2A/div (vertical) 2ms/div (horizontal)



(c) 10V/div (vertical) 5μs/div (horizontal)

Figure 8 - Transient response of experimental results
(a) Transient response of I1 and I2
(b) Transient response of I1+I2=I_0
(c) Transient response of V_0

V - CONCLUSION

In this paper, a current mode control applied to the parallel Buck converters has been presented.

The purpose of this article has been to show the strategy applied to share the currents between the converters and also to compare the response of the system in simulation and experimental evidencing the current distribution among non-identical converter modules.

It can be seen that the current really share between both of the parallel Buck converters analyzed and there are not current stresses in some of them. The currents, in both of them, are approximately the same and validate the proposed current mode control. The Figure 8 (c) prove that the output voltage has a good condition of stability, and the Figures 8 (a) and (b) prove that the current response is acceptable. It was shown that both converters share the load current and this is a strategy of control better than the strategies *A* and *B* already cited.

Like cited during the paper, there are many strategies to share the current in parallel converters. The Buck converter topology was adopted to construct the prototype. It means that the control strategy defended

here is not applied only in Buck converter topologies, but can be adapted to different converter topologies that are connected in parallel.

VI - ACKNOWLEDGEMENT

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