Exact Modelling of Interaction between Gate Pulse Generators and Power Electronic Switches for Digital Real Time Simulators

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Abstract: In recent years, digital real time simulators for studies of electromagnetic transients phenomena which allow the testing of equipment have been developed. A particular challenge represents the accurate real time simulation of gate pulse generating units of power electronic systems. In digital real time simulators, solution output is generated at equidistantly spaced time instants. However, simulated gate pulses can be issued at any time point in between these instants. Nonetheless, the correct simulation of many power electronic circuits makes the correct simulation of the gate pulse generation instants a mandatory requirement in order to obtain high quality simulation results. In this paper, a solution to this problem is proposed. It is demonstrated how accurate simulations of gate pulse generating units are obtained while satisfying the constraints of digital real time simulators.

Keywords: Real time simulators, modelling, EMTP solution techniques, power electronic contollers, HVDC systems.

I. Introduction

The development of digital real time simulators for electromagnetic transients [1], [5], [7], [10], [11], [13] is very challenging. On the one hand, the solution algorithms must lead to realistic and reliable simulation results, on the other hand very fast computational speed must be achieved.

In power electronic simulations, a correct simulation of the gating instants is fundamental since it strongly influences the interaction of the controller and network models which must be represented correctly in order to obtain accurate solution output. In this context, an algorithm, which was developed for the digital real time simulator ARENE [1], [5], [13], is proposed through which it is possible to simulate the time instants at which power electronic gate pulses are triggered exactly while adhering to the constraints given in digital real time simulators. In digital real time simulators, all computations which have to be performed to advance the simulation time between two adjacent discrete solution instants must never exceed in duration the constant integration step size.

In Section II, the basics for efficient and accurate simulations of changes of the network structure are reviewed. In Section III, a control system simulation algorithm for exact simulations of gating instants is proposed. In Section IV, the performance of this algorithm is assessed by means of case studies. In Section V, conclusions are given.

II. Simulation of Network Structure Changing Phenomena

In order that the exact simulation of gate pulses can significantly improve the overall solution accuracy, it is a requirement that switching processes within the network are simulated correctly. The related problems and solution techniques for digital real time simulators are reviewed in the following.

A. Electromagnetic Transients Program

The Electromagnetic Transients Program (EMTP) [2] is the most widely used digital simulator for studies of electromagnetic transients in power systems. It is based on the use of nodal analysis techniques. The popularity of simulators of the EMTP type is explained by the usually excellent accuracy of the generated simulation results as well as the extensive capabilities which allow the program to be used for a wide field of applications.

In simulations of power electronic circuits, however, numerical problems can occur as a consequence of the way power electronic switch state changes are simulated. The change of a switch state is usually not simulated at the same instant at which the condition for this change is satisfied.

B. Clock Synchronized Structure Changing

In what follows, the Clock Synchronized Structure Changing (*CSSC*) [12] algorithm, through which network structure changing phenomena in electromagnetic transients simulators can be represented efficiently and accurately, is reviewed.

A conceptual flowchart of the *CSSC* algorithm is shown in Fig. 1. After initializations have been performed, a loop is rerun for each of the pending integration steps, which are also referred to as time steps, until the termination condition is met. After entering the loop, the simulation time is incremented, the nodal voltages and the state variables [6] are calculated. Then, all elements

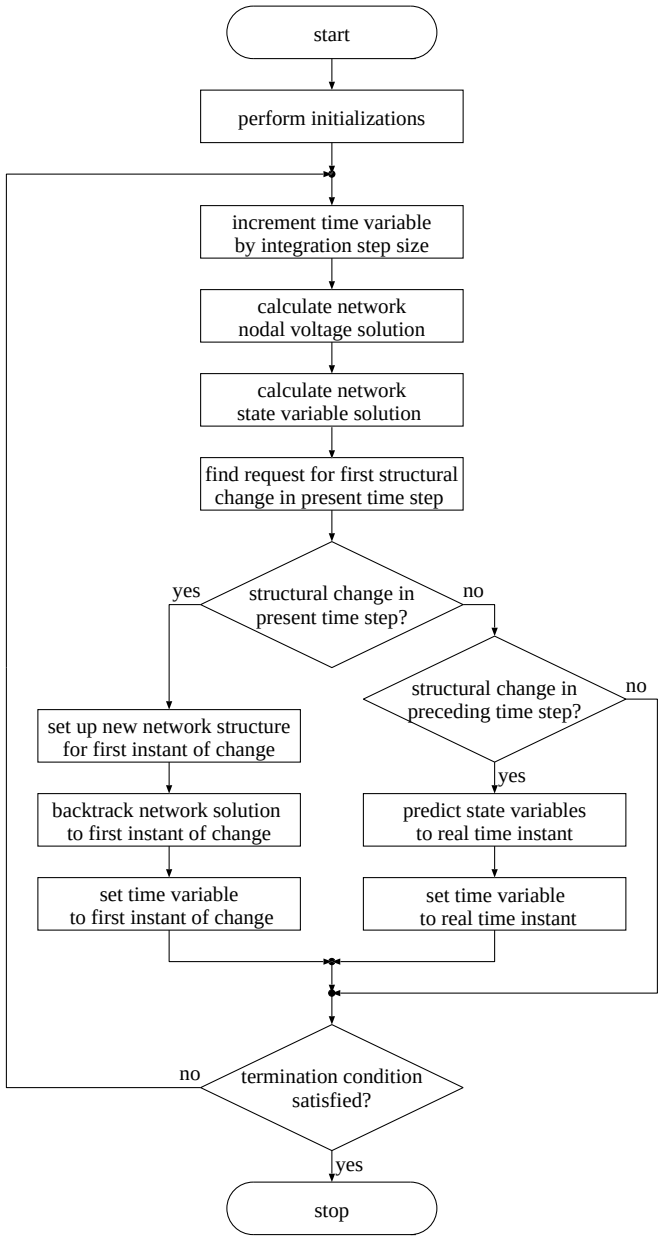

Fig. 1. Conceptual flowchart of an electromagnetic transients simulator with *CSSC* algorithm [12]

which can modify the network structure, e. g. the power electronic switches, are polled to check whether conditions for a structure change are satisfied.

If at least one condition for a structure change is met, then the network structure is modified according to which change is requested first. By employing interpolations between the solutions of the present and preceding integration steps, the time and the state variables are backtracked to the instant of change.

Since the integration step size in digital real time simulators is constant, the solution obtained in the next time step will lag behind the real time as a consequence of the backtracking. In order to make up for the lost time, a resynchronization scheme is necessary to synchronize simulation time and real time. This is achieved by employing linear extrapolations to predict the values of the simulation time and the state variables to the actual real time instant.

The *CSSC* algorithm is very efficient. Both backtracking and prediction procedures are by themselves computationally very simple. Furthermore, backtracking and prediction procedures are always invoked in different integration steps.

III. Exact Simulation of Gate Pulse Generations

In what follows, a novel algorithm, referred to as *CSPG*, for Clock Synchronized Pulse Generation concept, is discussed. Through this algorithm, the instants at which gate pulse signals are triggered are simulated efficiently and exactly. The functioning of the algorithm is explained by considering the modelling and simulation of a voltage controlled oscillator (VCO) as part of a gate pulse generator (GPG) of a high voltage direct current (HVDC) control system.

In Subsection III-A, a brief description of a GPG is given. In Subsection III-B, it is described how the exchange of data between network and control system simulations is organized at each integration step. In Subsection III-C, the *CSPG* algorithm is presented. In Subsection III-D, this algorithm is discussed.

A. Gate Pulse Generator Description

The gate pulse generators of modern HVDC control systems are based on the principle of equidistant firing control [3]. As the name indicates, in steady state gate pulses are generated at equidistant time intervals. In order to simulate such systems, this fundamental characteristic must be represented correctly.

A diagram of a typical gate pulse generator is depicted in Fig. 2. The control voltage V_c is proportional to the error of the quantity being regulated. This input is obtained from a control system of higher level. In steady state V_c becomes zero. The actual time period of the AC voltage is given by T. The number of gates to be supplied is n. The reference voltage of the VCO is V_r:

$$\frac{V_\mathrm{r}}{\mathrm{V}} = \frac{T}{\mathrm{s}}\frac{1}{n} + \frac{V_\mathrm{c}}{\mathrm{V}} \,. \tag{1}$$

In the VCO V_r is compared with a sawtooth waveform with the slope 1 V/s. As soon as the rising sawtooth in-

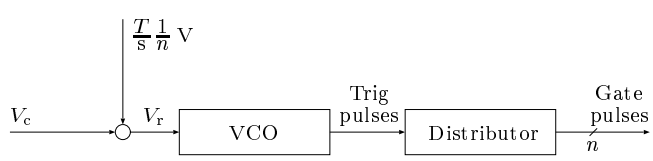

Fig. 2. Gate pulse generator diagram

tersects the reference voltage, the sawtooth is reset to 0 V. In addition, a trig pulse is sent to the distributor which transmits a pulse to the thyristor to be gated.

In steady state the reference voltage is constant: $V_\mathrm{r} = (T/\mathrm{s})1/\mathrm{n}\,\mathrm{V}$. Trig pulses are then issued at intervals equal to T/n.

B. Control System Simulation Input and Output

The *CSPG* algorithm is designed for simulators in which the network and control system equations are solved separately. It is therefore important to address how the exchange of information between the two solution procedures is organized.

In integration step k, the inputs of the control system model coming from the network side are based on the network solution found in integration step $k-1$. At each integration step, the control system equations are solved before the network state variable solution is established. In integration step k, the inputs of the network device models coming from the control system side are derived from the control system solution of integration step k.

C. Clock Synchronized Pulse Generation Algorithm

The sequence of steps of the *CSPG* algorithm is clarified by means of Fig. 3 in which the simulation of a VCO sawtooth function cutting the reference voltage V_r is studied. The VCO solution is obtained as part of the solving of the control system equations. The real time instant after the integration step k is denoted by $t_\mathrm{r}(k)$, the simulation time instant after the integration step k is denoted by $t_\mathrm{s}(k)$. The integration step size is Δt. The filled circles mark final solution points used for output while the unfilled circles mark intermediate solution points. It is assumed that over the time interval considered in Fig. 3 the only change of the network structure is the one provoked through the trig pulse.

In integration step $k-1$, from instant $t_\mathrm{r}(k-2)$ to $t_\mathrm{r}(k-1)$, the sawtooth ramp is incremented by the constant value $\Delta t\,(\mathrm{V/s})$. Neither a structure change in the previous nor in the present integration step has occurred. The solution is thus retained as the final one and used for output at $t_\mathrm{r}(k-1)$.

In integration step k, from instant $t_\mathrm{r}(k-1)$ to $t_\mathrm{r}(k)$, the intermediate solution after incrementing the ramp by $\Delta t\,(\mathrm{V/s})$ yields a sawtooth voltage which exceeds V_r. A trig pulse is issued to the distributor. The distributor instantly sends a gate pulse to the corresponding power semiconductor switch model. Furthermore, the time instant at which the intersection occurred is calculated and passed to the *CSSC* algorithm. There, the requests for all changes of the network structure are prioritized as a function of their respective occurrence in the time domain. If the gate pulse, which was issued by the GPG, constitutes the first request for a structure change to occur within integration step k, then the sawtooth of the VCO will be backtracked to the intersection instant $t_\mathrm{s}(k)$.

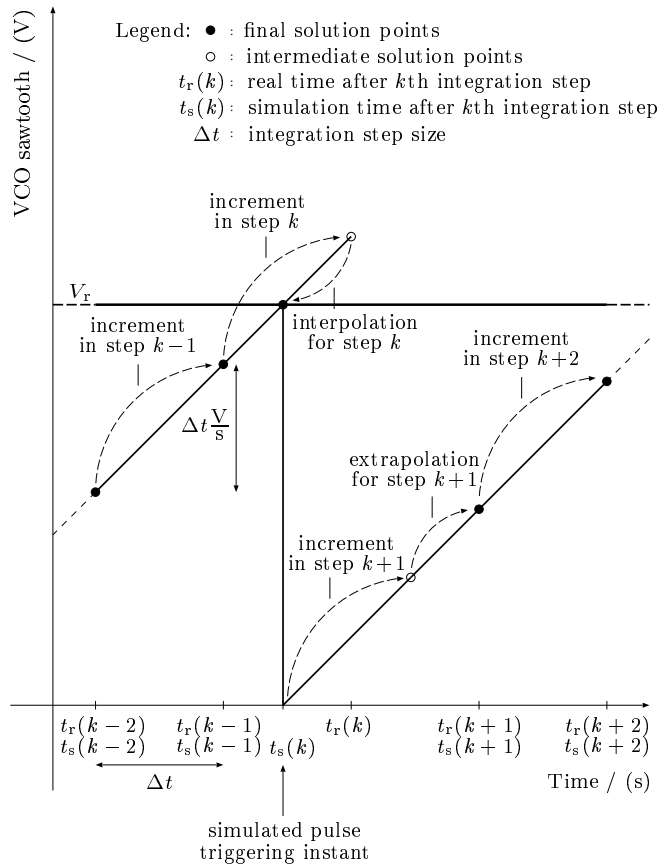

Fig. 3. Simulation with *CSPG* concept: exact pulse triggering instant detection

As part of the *CSSC* algorithm, the corresponding new network structure is set up and the network state and time variables are backtracked, see Fig. 1.

The results of these interpolation procedures are used for output at time instant $t_\mathrm{r}(k)$ because the solution found at $t_\mathrm{s}(k)$ represents reality more accurately than the intermediate solution points found in integration step k, see Fig. 3.

In integration step $k+1$, from instant $t_\mathrm{r}(k)$ to $t_\mathrm{r}(k+1)$, the instant at which the intermediate solution is found does not coincide with the real time instant $t_\mathrm{r}(k+1)$. This is a consequence of the constant integration step size. If, as assumed in Fig. 3, no further structural change is requested, linear extrapolation of the sawtooth function of the VCO to $t_\mathrm{r}(k+1)$ will be employed.

As part of the *CSSC* algorithm linear extrapolation to $t_\mathrm{r}(k+1)$ is equally performed for the time and network state variables.

In integration step $k+2$, from instant $t_\mathrm{r}(k+1)$ to $t_\mathrm{r}(k+2)$, the ramp is incremented by the constant value $\Delta t\,(\mathrm{V/s})$. No requests for switch state changes are encountered.

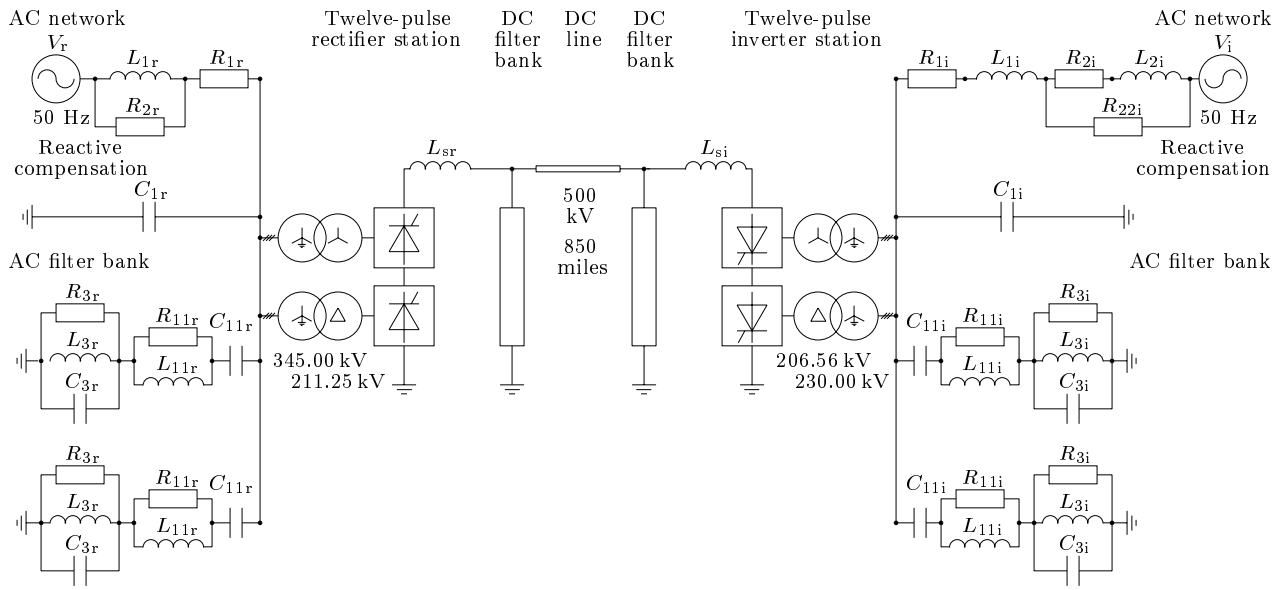

Fig. 4. CIGRE HVDC benchmark network [4]

D. Discussion

Through the *CSPG* algorithm, the exact instants at which gate pulses are issued are calculated. This makes *CSPG* very suitable for use in electromagnetic transients simulators where a backtracking-prediction method is used for correct simulation of switch state changing processes.

These methods are computationally highly efficient and allow to accurately simulate switch state changes even though the integration step size is constant. The solution procedure of the digital real time simulator ARENE is based on these algorithms.

In the method described in [9], backtracking is used to improve the accuracy of the control system solutions as well as for the synchronization to maintain an equidistant solution output. However, the presented method requires computationally relatively expensive additional intermediate network solutions at each integration step.

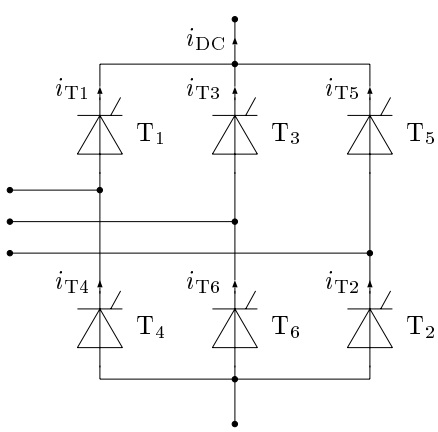

Fig. 5. Six-pulse bridge

Alternative techniques to detect gating instants more accurately could involve the use of a variable integration step size [8]. However, in digital real time simulators a constant integration step size is preferred.

IV. Case Study: Simulation of HVDC Benchmark System

In the following, the proposed *CSPG* scheme is tested by running simulations of an HVDC benchmark system.

A. Simulation Setup

The test network is depicted in Fig. 4 [4]. Both rectifier and inverter station comprise two six-pulse bridges as depicted in Fig. 5, which are connected in series. The most important circuit data are summarized in Table I.

TABLE I
HVDC benchmark model parameters [4]

Rectifier side	Inverter side
$V_r = 1.08$ p. u.	$V_i = 0.94$ p. u.
$R_{1r} = 3.74\,\Omega$	$R_{1i} = 0.74\,\Omega$
$R_{2r} = 2160.00\,\Omega$	$R_{2i} = 0.74\,\Omega$
	$R_{22i} = 24.81\,\Omega$
$L_{1r} = 150.80$ mH	$L_{1i} = 36.50$ mH
	$L_{2i} = 36.50$ mH
$C_{1r} = 3.34\,\mu$F	$C_{1i} = 7.52\,\mu$F
$R_{11r} = 83.00\,\Omega$	$R_{11i} = 36.90\,\Omega$
$R_{3r} = 50.00\,\Omega$	$R_{3i} = 22.20\,\Omega$
$L_{11r} = 15.10$ mH	$L_{11i} = 6.71$ mH
$L_{3r} = 9.69$ mH	$L_{3i} = 4.31$ mH
$C_{11r} = 6.57\,\mu$F	$C_{11i} = 14.78\,\mu$F
$C_{3r} = 78.90\,\mu$F	$C_{3i} = 177.50\,\mu$F
$L_{sr} = 597.00$ mH	$L_{si} = 597.00$ mH

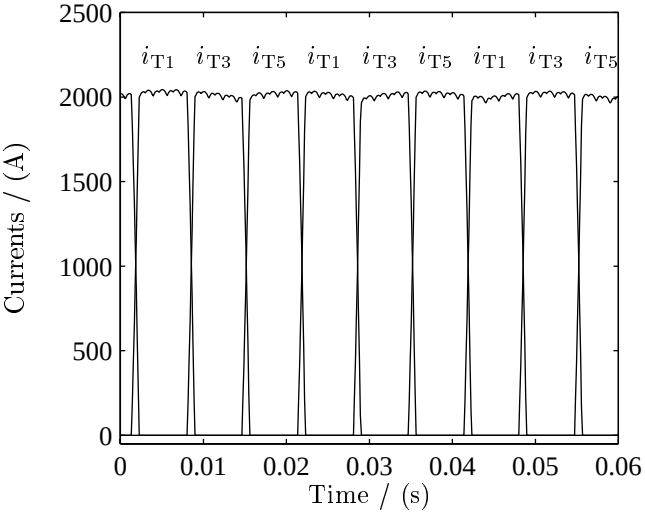

Fig. 6. Thyristor valve currents under steady state condition: simulation without *CSPG*

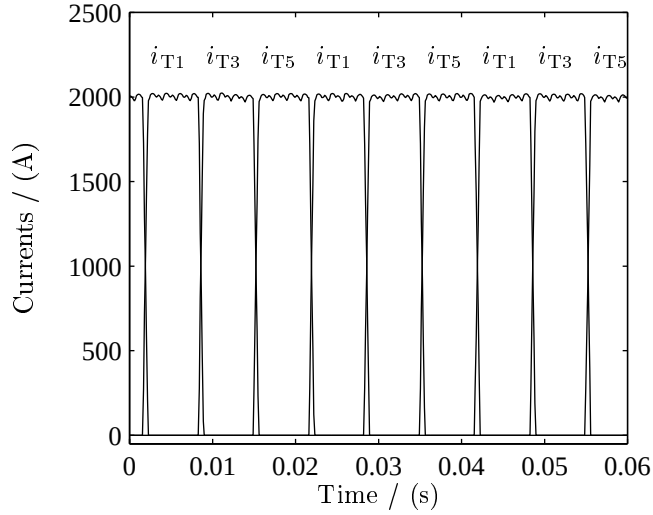

Fig. 7. Thyristor valve currents under steady state condition: simulation with *CSPG*

The control system is a modified version of the model described in [14]. The order for the DC current is set to 2000 A. The integration step size chosen is $\Delta t = 100\,\mu$s.

B. Test Results for Simulation without CSPG

In a first simulation, *CSPG* is not enabled. The thyristor valve currents i_{T1}, i_{T3} and i_{T5}, see Fig. 5, in steady state are considered. The simulation results are depicted in Fig. 6.

It can be recognized that the magnitude of the currents reveals a significant jitter around the value 2000 A. The jitter occurs because the equidistant pulse control system is not modelled with as high a precision as necessary. The simulated pulses are not equidistantly spaced. The statistical imprecision is only limited by the integration step size. For the integration step size of $100\,\mu$s and a base frequency of 50 Hz, the ignition delay angle imprecision $\Delta\alpha$ at each integration step is $0° \leq \Delta\alpha \leq 1.8°$.

The accuracy could be improved by reducing the integration step size. However, for real time performance at each integration step all calculations must be completed within a time interval which must not exceed the integration step size. Therefore, the more complex the network, the larger the integration step size must be to achieve real time performance.

C. Test Results for Simulation with CSPG

In the following the *CSPG* algorithm is activated. In Fig. 7, the results of a steady state simulation of the thyristor valve currents are given.

It can clearly be recognized that the jitter has disappeared. This is because the simulated gating instants are now equidistantly spaced. The simulation results now match the phenomena observed in the real world.

Now, the simulation of a short circuit across the DC filters of the rectifier is considered. The short circuit starts at $t = 0.1$ s. In Fig. 8, the rectifier DC current i_{DC} is shown. Prior to the short circuit, the DC current is $i_{DC} = 2000$ A. The current rises sharply directly after the beginning of the short circuit. The controller of the rectifier station then advances the ignition delay angle so that the DC current becomes again $i_{DC} = 2000$ A. The simulated firing pulse instants are then equidistantly spaced again. The magnitude of the DC current is free of jitter effects.

V. Conclusions

A novel algorithm for accurate numerical real time simulations of interactions between gate pulse generators and power electronic switches was presented. It allows to accurately simulate gating instants even though a constant integration step size is used while keeping the computational burden at a minimum.

The high precision for the simulation of the instants at

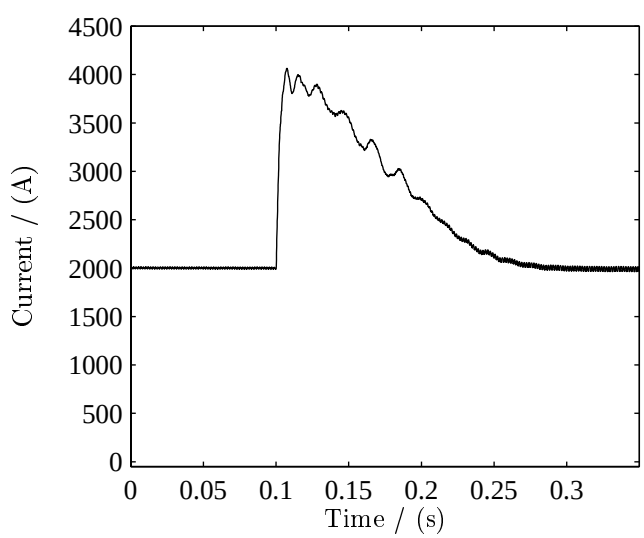

Fig. 8. Rectifier DC current under the condition of a short circuit across the DC filters: simulation with *CSPG*

which gate pulses are triggered is achieved by means of interpolation based backtracking. The resynchronization of simulation time and real time is ensured through the application of extrapolation based prediction. Case studies involving an HVDC benchmark system have demonstrated that a very high simulation precision is achieved.

The algorithm is used in the digital real time simulator ARENE. This makes ARENE a very powerful tool for real time simulations of electromagnetic transients in power electronic systems.

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