Considerations on Pulsed DC-Link Voltage Converters

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***Abstract* - This digest presents and classifies the PDCLV topologies in terms of the pulsed dc-link voltage waveform and refers to the converters by their AWCs. Also, the pulse modulation technique they are able to employ is taken into account. The essential features associated with each type of converter is presented before a comparison is established in terms of those features. Only topologies in which the bridge devices commutate under Zero-Voltage-Switching (ZVS) technique are considered. In addition, an extensive bibliography is included. Although this study is related to inverters most of these can be easily adapted to be used with AC-to-DC and AC-to-AC converters.**

I. Introduction

In recent past, significant advances in AC-to-AC, AC-to-DC, and DC-to-AC converter topologies have been reported. With the advent of gate turn-off power devices a large number of topologies has been proposed with the purpose of improving the process of power conversion through a combination of new circuit topologies, improved input and output of voltage and current waveforms, harmonic minimization, and various control strategies. Most of research initiative to date has been with DC-link. While Pulse-width modulation (PWM), which is associated with hard-switching was first reported in the mid-1970's [1], the resonant DC-link technology, which features soft-switching, appeared in 1986 [2]. Since then a number of soft-switched topologies that operate as current and voltage sources have been developed, although this technique does not have the industry preference [3]-[31]. Because of the the different principles employed as well as for the sake of generalization they will here referred as Pulsed DC-Link (PDCL) converters. The voltage source type (PDCLV) is the most used among the PDCL converters. Figure 1 presents a generalized structure for PDCLV AC-to-AC converters. In these converters the DC-link voltage is shaped by an Auxiliary Waveshaping Circuit (AWC) so that its waveform becomes null in a resonant mode to commutate the bridge switches under zero voltage. Same type of generalized representation can be used for rectifiers [Fig. 2(a)] and inverters [Fig. 2(b)]. Due to the vast number of original topologies with sometimes contradictory performance claims, a comprehensive study of major PDCLV topologies seems to be appropriate. The only reviews on these converters the authors are aware of treat them as part of a broader overview on soft-switching converters [1][3]. Also, [4] has classified the PDCLV topologies taking into account their PWM operation capability.

Differently from [4], this digest presents and classifies the PDCLV topologies in terms of the pulsed dc-link voltage waveform, (Fig. 3) but also takes into account their PWM operation capability. Depending on the pulse modulation technique they employ, there exist six different types of converters. The essential features associated with each type are presented before they are employed to compare the different topologies.. The study is limited to topologies with bridge devices commutating under Zero-Voltage-Switching (ZVS) technique and an extensive bibliography is included.

II. Topologies for Pulsed DC-Link Voltage Converters Type A

This study will consider mainly inverter topologies but it can be easily adapted for both DC-to-AC and

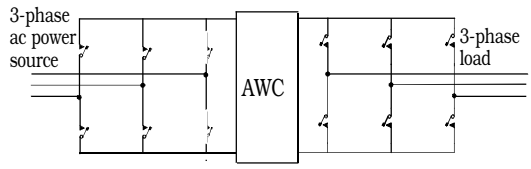
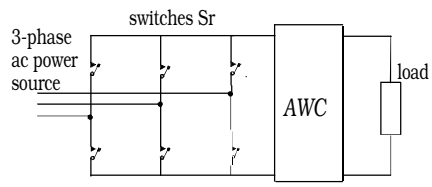
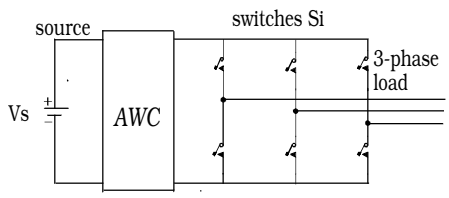


Fig. 1. Generalized structure for PDCVL AC to AC converters



(a) Rectifier



(b) Inverter

Fig. 2. Generalized structures for PDCVL AC-to-DC and DC-to-AC converters

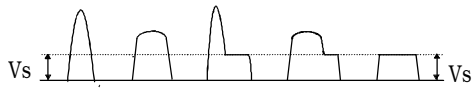


Fig. 3. Types of DC-link voltage waveforms

AC-to-AC converters. The waveforms in Fig. 3 can have either constant or adjustable width. For this reason the existing topologies originate six different types of inverters, if the technique of modulation they can employ is taken into account. In general, Pulsed DC-Link Voltage isolates the DC-link voltage from the DC source voltage during the resonant cycle in different ways. The isolation can be accomplished by an inductor L in the main path of the power flow. It can also be is accomplished by a resonant switch. Besides that, a "mixed isolation" can be employed, that is, a switch and an inductor are connected in series for isolation. In the following, all topologies will be represented by their AWCs

A. Type I: Resonant DC-Link Converter

The *Resonant DC-Link* (RDCL) *converter*, shown in Fig. 4, minimizes the switching losses and reduces harmonic problems [2]. Its voltage pulse has a constant width and its zero voltage interval width can also be considered as nearly constant (*Constant Notch Interval, CNI)*. For this reason, it basically employs Pulse Density Modulation (PDM).

This converter, represented by the AWC I in Fig. 4(a), has a high dynamic performance because enables switching frequencies of 20 kHz and above [2]. However, it suffers from substantial regular voltage peaks across the converter devices, which are 2 - 3 times the DC voltage V_s [2].

The peak voltage of the resonant peak have been confined to twice V_s by using an additional power circuit to initialize the resonant inductor current [5]. However, same results can be accomplished with a simpler circuit, represented by AWC II in Fig. 4(b) [6]. Other enhancements for the RDCL, include efficient control algorithms [7].

B. Type II: RDCL Converter with Reduced Voltage Peak

The *Resonant DC-Link with Reduced Voltage Peak* (RDCL-RPV) converter [Fig. 5] does limit the device voltage peaks to 1.2 - 1.5 times V_s. Such limits can be achieved by the Actively Clamped RDCL (ACRDCL) converter represented by AWC III [8], of which simulated results for the link voltage is shown in Fig. 6. However, active clamping produces current jumps with high di/dt at twice the resonant frequency and high stresses and losses in the clamping device [9]. Passively Clamped RDCL (PCRDCL) converters, corresponding to AWCs IV [8] to VI [9] eliminate this problem. It should be mentioned that, although the circuits corresponding to AWC V and AWC VI can be designed to reduce the peak voltage, a clamping circuit can be added to them to provide an additional protection [9].

C. Type III: PWM Resonant DC-Link Converter

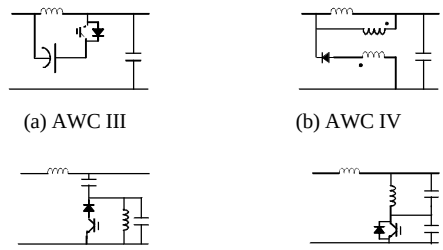
The PWM-RDCL converters are represented by AWCs VII [10][11] and VIII [11] (Fig. 7). They are able to synchronize with external PWM signals, since they can adjust the pulse width, but continue to suffer from high voltage stresses and operate with a nearly *CNI.*

D. Type IV: PWM Resonant Pulse with Reduced Voltage Peak

The ACRDCL converter can operate with PWM techniques if the resonant capacitor at the inverter input is split into individual capacitors across each switch of the bridge, as shown in Fig. 8 [12]. Other PWM versions that incorporate the principle of the actively clamped circuit to the RDCL, the PWM-ACRDCL, are indicated in Fig. 9 by AWCs IX to XI [13]-[15], which use electrolytic capacitors, and AWCs XII to XVI [10], which use resonant capacitors. They operate all with CNI. These actively clamped converters electrolytic capacitors have to regulate excessive pumping charge into the clamp capacitor due to the initial current stored in the resonant inductor to compensate losses. The PWM passively clamped (PWM-PCRDCL) converters represented by AWCs XVII and XVIII [16][17] eliminate such a problem. However, its overvoltage period introduces a limitation in the modulation technique to be used [17]. Simulated results in Fig. 10(a) and (b) show the voltage peaks in the DC link for

(a) AWC I (b) AWC II

Fig. 4. AWCs for the Resonant DC Link converter



(a) AWC III (b) AWC IV

(c) AWC V (d) AWC VI

Fig. 5. AWCs for the Resonant DC Link converter with reduced voltage peaks

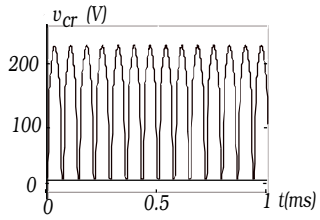


Fig. 6. Simulated results for converter with AWC III (V_s = 150 V)

AWCs IX and XVIII, respectively.

E. Type V - Quasi-Square-Wave with Resonant Transition DC-Link Converter with CNI

In these topologies the DC-link voltage is clamped to the value of the input voltage (Fig. 11). They are usually referred as Quasi-Resonant DC-Link (QRDCL) converters. Switch-isolated inverters with electrolytic capacitors are represented by AWCs XIX [18] and XX [19]. The main problem with these topologies is the difficulty to regulate the capacitor voltage for all range of operation. Other possibilities are AWCs XXI [20] and XXII [21], for this type of converter.

F. Type VI - Quasi-Square-Wave with Resonant Transition DC-Link Converter with ANI

Although inductor isolation (AWCs XXIII and XXIV) [22] and mixed isolation (AWC XXV) [23] can be found in this type of converter, most of them are switch-isolated, as shown in Fig. 12. Besides that, the existing topologies employ one or two additional switch, as indicated by AWCs from XXVI to XXX [24]-[38] and by AWCs from XXXI to XXXIII [27][29][30], respectively. Simulated results in Fig. 13 illustrate the behaviour of the voltage link for AWC XXVIII [26]. During the adjustable notch width interval (conduction of either diode D_i or switch S_i) one of the three cases in Fig. 14 may occur. Except for AWCs XXIX [27], XXXII [27], and XXXIII [30], all other topologies fall in cases (a) and (b), in which the inductor current freewheels while the notch interval holds. This deteriorates the efficiency of the converter. However, AWC XXIX is unable to operate in the regenerative mode and in AWC XXXIII there is a voltage fluctuation in the split capacitors.

It is possible to generate new converters type ANI by adding an extra switch to AWCs XIX [13] and XXII [21], for instance. Also, an extra switch in XXVI [24] and XXXI [29] allows to not have inductors in the freewheeling path during the notch interval.

III. Control, Modulation Techniques and Selection

As can be seen, a great number of topologies with different features do exist. Also, several control schemes can be employed for DC-to-AC, AC-to-DC, and AC-to-AC systems, depending on the structure used. For example, the change from motoring to regenerative mode of operation and *vice-versa*, causes large peaks in the voltage capacitor in inductor-isolated topologies. This, in turn, causes high inductor current peaks [2]. Clamping circuits and control techniques reduce these peaks [31]-[33]. In particular, the "three arcs law" optimizes the current and voltage peaks in RDCL and ACRDCL converters [32]. This technique is shown in Fig. 15 where for a resonant capacitor C_r and a resonant inductance L_r, $Z_o = \sqrt{L_r/C_r}$. In that figure, I_{Lr} is current in the resonant inductance and I_p is maximum excitation current that can be applied to the resonant link.

Input and output voltage and/or current control is possible with structures operating with either techniques PDM or PWM. Voltage and current regulators can be accomplished with delta modulation techniques. Implementation of sigma-delta modulation (ΣΔM) and modified ΣΔM [35][36][37] have been used

(a) AWC VII (b) AWC VIII

Fig. 7. AWCs for PWM Resonant DC Link converters

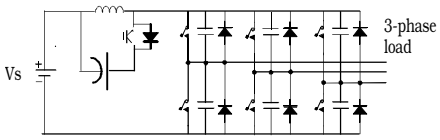
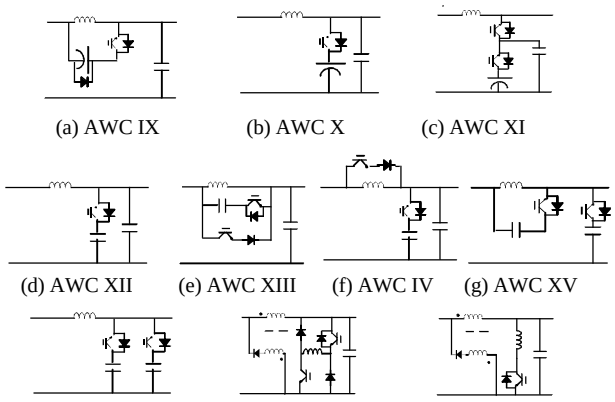


Fig. 8. Split of the resonant capacitor in individual capacitors across each switch.

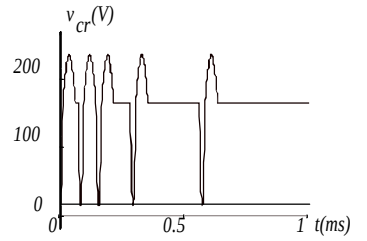


(a) AWC IX (b) AWC X (c) AWC XI

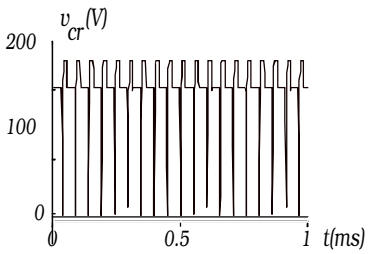
(d) AWC XII (e) AWC XIII (f) AWC IV (g) AWC XV

(h) AWC XVI (i) AWC XVII (j) AWC XVIII

Fig. 9. AWCs for PWM Voltage Clamped Resonant DC Link converters



(a) AWC IX (V_s = 150 V)



(b) AWC XV (V_s = 150 V)

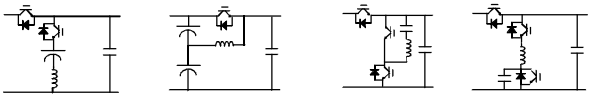
Fig. 10. Simulated results for PWM voltage clamped converters

for PDM and input unity power factor has been obtained [38].

Certainly, a better performance is obtained when converters with PWM capability are employed. In the case of an AC-to-AC system, the current reference of the source can be obtained from the balance of the active power flow between the source and load and the current reference of the inverter from the speed controller and field oriented controller. Synchronous PI current regulators has been used [34]. Also, a state-feedback control scheme has been reported in [39]. These different procedures have been succeeded with the help of PWM techniques. Carrier-Based Modulation (CBM) [14], Space Vector Modulation (SVM) [18][28], Hybrid PWM and PDM (either analog [8] or digital, [15][34]), and hybrid SVM and CBM (HSVCBM) [40] are some of these PWM techniques.

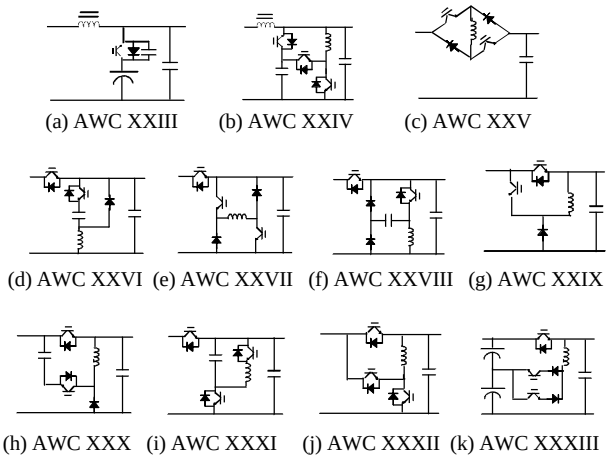
On the other hand, by considering that PDCLV topologies can operate with either CNI or ANI, special PWM patterns have been developed. It has been shown that for converters type CNI a ripple content of the load current not too far from that of the conventional schemes, can be obtained with SVM. In addition, the bridge switching losses can be reduced if the comutation circuit is activated only once per switching interval [18]. The converter type ANI, however, gives better results than the CNI type in terms of lower-order harmonics, total harmonic distortion and distortion factor of the line current and reduction in the number of commutations [27][28]. In this case, the zero voltage interval is considered as a third zero voltage vector. Simulated results are presented in Fig. 16 for the input power factor control of a rectifier that employ AWC XXX.

Another aspect that influences control is that the resonant capacitor has to have enough energy to overcome losses or has to be "assisted" to completely discharge, allowing ZVS turn-off. For converters with inductor isolation, two of the solutions found in literature are (1) an additional power circuit to initialize the resonant inductor current [5][41] and (b) a current prediction scheme [9]. For inverters with switch isolation the equivalent snubber capacitor must discharge (charge) completely from (to) the voltage source value after that switch is turned off. The discharge can be accomplished by the load current [Fig. 17(a)]. However, to operate from no-load to full-load, either an "initial inductor current" [Fig. 17(b)] or an auxiliary oscillating circuit with the capacitor pre-charged or not [Fig. 17(c)] is necessary. Except for AWCs XXVI [24] and XXX [28], which use an oscillating circuit as in Fig. 18(c), in all other QRDCL converter the initial inductor current is linearly increased, as illustrated in both Fig. 18(a) and Fig 18(b) [11]. As a consequence, this initial current has to be controlled to guarantee adequate operation from no-load to full-load. Instead, the capacitor voltage control has been introduced together with AWC XXX and is



(a) AWC XIX (b) AWC XX (c) AWC XXI (d) AWC XXII

Fig. 11. AWCs for QRDCL converters with CNI



(a) AWC XXIII (b) AWC XXIV (c) AWC XXV

(d) AWC XXVI (e) AWC XXVII (f) AWC XXVIII (g) AWC XXIX

(h) AWC XXX (i) AWC XXXI (j) AWC XXXII (k) AWC XXXIII

Fig. 12. AWCs for QRDCL converters with ANI

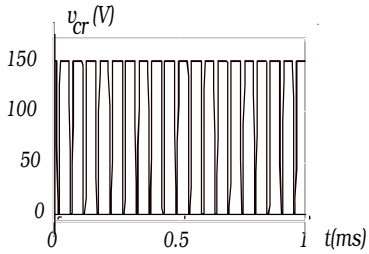
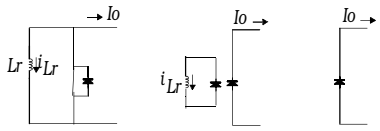


Fig. 13. Simulated results for the link voltage in AWC XXVIII (V_s = 150V)



(a) (b) (c)

Fig. 14. Different possibilities for adjusting the notch interval

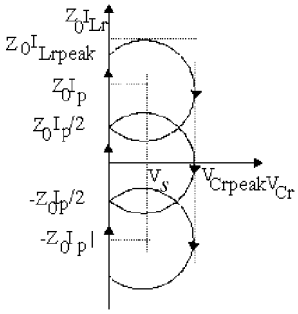


Fig. 15. "Three arcs law"

claimed to be of easier implementation than the current control [29]. Another alternative is the use of an auxiliary transformer assistance, Fig. 18(d) [4].

For the charge of the resonant capacitor a freewheeling inductor current (that could also be a current source), Fig. 19(a), or a current that increases

linearly [Fig. 19(b)] or a resonant current [Fig. 19(c)] are the main techniques employed.

Table I summarizes the features of most of the topologies discussed in this paper. Technology has been applied with a variety of devices including BJTs, GTOs, MOSFETs, IGBTs and MCTs, around the world. Efforts have been made to characterize these devices for the resonant mode of operation. It has been calculated that RDCL and ACRDCL converters switching at 3 - 4 times the frequency of hard-switched PWM systems yield approximately equivalent spectral and control characteristics [35]. Also, even for a frequncy ratio of 20:1 the the device switching losses in RDCL are actually less than unde hard switching conditions [. For soft-switched PWM systems, however, the type of soft switching technique (ZVS or ZCS) used, the type and number of switches, and the type of freewheeling during the notch interval play an important role in the total losses for the topology to be selected. Therefore, only a judicious comparative study of losses would lead to a better guideline for selection of the topology to be used.

CONCLUSION

While hard-switched will continue to dominate the high-power market in the forseeable future, pulsed dc soft-switched converters are likely to make advances. Table I summarizes typical features. This paper has classified them in terms the pulsed dc-link voltage waveform and their PWM operation capability. Principles of operation and main features have been discussed for a better understanding of each possibility. Researchers continue to make an efort to make the PWM quasi-resonant DC-link topologies an alternative to the well established RDCL and ACRDCL techniques. A comparative study on losses is under study to complete this scenario that is expected to aid the nonspecialist engineer in the preliminary stages of converters selection and analysis.

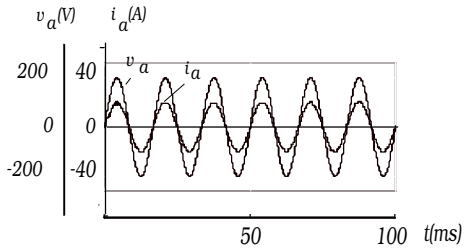


Fig. 16. Simulated results for unity power control with AWC XXX

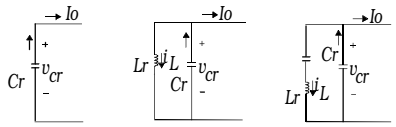


Fig. 17. Different possibilities for capacitor discharge

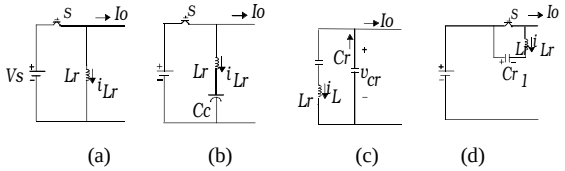


Fig. 18. Different possibilities to obtain the initial inductor current

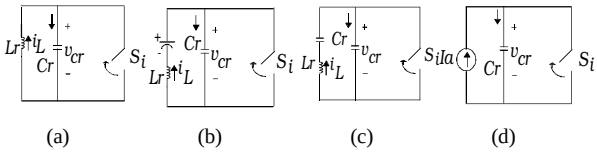


Fig. 19. Different possibilities for charging the capacitor

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TABLE I - COMPARISON OF PULSE RESONANT DC-LINK CONVERTERS

	A	B	C-pu	D-pu	E	F	G	H	I	J
I	-	1L/1C	>2.5	-	yes	-	yes	-	no	no
III	1S-1D	1L/1C	1.5 -1.8	1	yes	-	yes	1	no	no
V	1S-2D	1L/2C	1.5	>1	yes	-	yes	-	no	no
X	1S-1D	1L/1C	1.1-1.3	>1	yes	-	yes	1	no	no
XI	2S-2D	1L/1C	1.2	>1	yes	-	yes	1	no	no
XVI	2S/2D	1L/2C	1.6	1	yes	-	yes	-	no	no
XVII	2S/4D	3L/1C	1.1-1.3	1	no	-	yes	-	no	yes
XIX	2S/2D	1L/1C	1	>1	yes	-	no	1	no	no
XX	1S/1D	1L/1C	1	>1	yes	-	yes	2	yes	no
XXI	3S/2D	2L/2C	1	high	no	-	no	1	no	no
XXII	3S/3D	1L/2C	1	high	yes	-	no	-	no	no
XXVI	2S/3D	1L/2C	1	high	no	yes	no	-	no	yes
XXVII	3S/3D	1L/1C	1	>1	yes	yes	no	-	no	yes
XXVIII	2S/4D	1L/2C	1	>1	yes	yes	no	-	no	yes
XXIX	2S/2D	1L/1C	1	1	yes	no	no	-	no	yes
XXX	2S/3D	1L/2C	1	high	no	yes	no	-	no	yes
XXXII	3S/3D	1L/1C	1	1	yes	yes	no	-	no	yes
XXXIII	3S/3D	1L/1C	1	>1	yes	no	no	2	yes	yes

A - Number of switches and diodes; B - Number of resonant inductors and capacitors; C - Voltage peak across the main switch; D - Current peak in the DC switch (* = controlled by design); E - Requests linear energizing for the inductor; F = Inductor losses during the adjustable notch; G - Inductor losses during the "on" period; H - Number of electrolytic capacitors; I - Voltage fluctuation in split capacitors; J - adjustable notch.

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