A Quadruple ZVS-PWM Active-Clamping Forward Converter

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***Abstract* - This paper presents an isolated dc-dc converter without switching losses from no-load up to full-load, also featuring a voltage stress across each switching device smaller than half of the input voltage. The proposed converter is based on four ZVS-PWM active-clamping forward converters connected in series and coupled using a single high frequency transformer. This converter is suitable for high input voltage (800Vdc) and high power applications. Operation principle, theoretical analysis, design example and experimental results, taken from a 3kW laboratory prototype, are presented.**

I. INTRODUCTION

In telecommunication systems, a power supply is composed by a power factor correction PFC rectifier (ac-dc converter) and a dc-dc converter. To obtain power factor correction, the topology generally used is the boost rectifier, which presents an output voltage greater than the input voltage. For example, when a three-phase input voltage of 380Vac is utilized, the output voltage of the rectifier always will be greater than 600Vdc. Therefore, nowadays there is a demand for dc-dc converters capable of operating with high bus voltage and low voltage stress across the switching devices.

It is known that the conventional FB-ZVS-PWM converter is not suitable for high input voltage applications because the total input voltage is applied across its blocking switches [1].

Among the alternatives to overcome this drawbacks are the series connection of switches and multilevel topologies. In the series connection of switches, the static and dynamic sharing of the voltage across the switches is difficult to obtain and requires specific techniques. Multilevel topologies seem to be a more effective solution because they can solve the problem of static and dynamic sharing of the voltage and minimize the electromagnetic interference, since the dv/dt is reduced [2].

Another alternative to solve the problems of the series connection of the switches is the association of two or more converters in series reducing the voltage stress on each switching device. This method is appropriate if a perfect division of the voltage between the converters can be guaranteed at any time. This condition is attainable by coupling the converters with a single high-frequency power transformer as explained in [3, 4]. The associated converters coupled by a single transformer are controlled by the same control circuit. Hence, the pulse-width-modulator and drive circuit are identical for all the converters, allowing a good sharing of the voltage across the switches. On the other hand, they are capable of automatically balance the voltage of the input capacitors associated in series and connected to a dc bus voltage. If one of the voltages is higher, the respective capacitor will transfer energy to the other through the transformer during the on time.

In this paper the converter shown in Fig. 1 is proposed. The proposed converter was derived from the topologies proposed in references [5,6,7]. This converter is described and analyzed in the following sections.

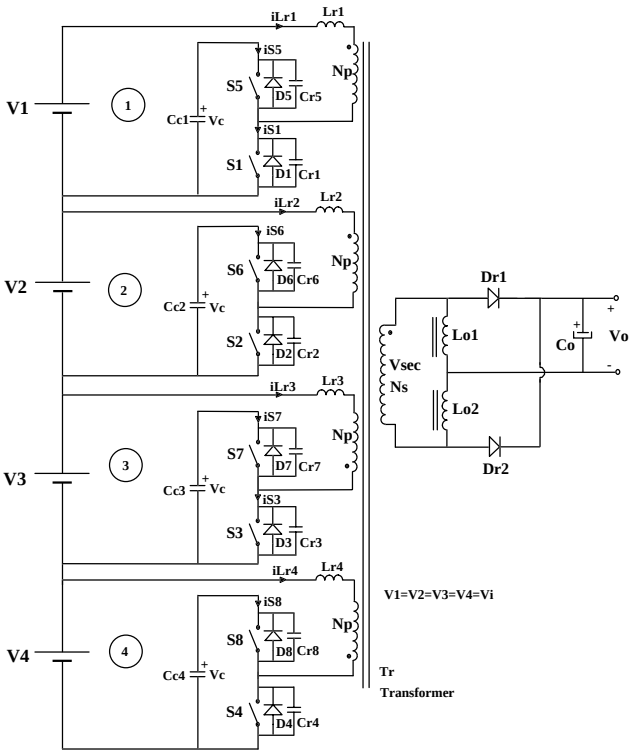

Fig. 1. The proposed converter.

II. CIRCUIT DESCRIPTION AND PRINCIPLE OF OPERATION

A. Circuit Description

The proposed converter, shown in Fig. 1, is composed by the following components: main switches S_1,..S_4, auxiliary switches S_5,..S_8, resonant inductors L_{r1},..L_{r4}, five-winding high frequency transformer T_r, input voltage sources V_1,..V_4, clamping capacitors C_{c1},..C_{c4}, commutation capacitors C_{r1},..C_{r8}, anti-parallel diodes D_1,..D_8, rectifier diodes D_{r1} and D_{r2}, output filter given by L_{o1}, L_{o2} and C_o, and load R_o.

B. Principle of Operation

In the suggested converter the two upper converters operate simultaneously during the first semi-cycle of operation and the two lower converters operate simultaneously during the subsequent half operation period. Within a semi-cycle of operation, six different stages of operation take place. Fig. 2 shows the main theoretical waveforms for one switching period. Following is a description of each stage.

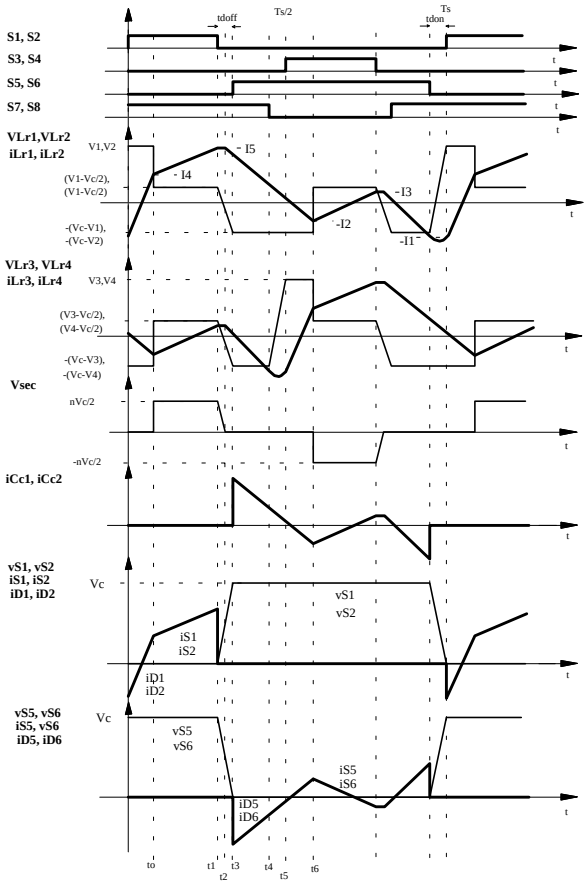

Fig. 2. Main waveforms of the converter.

First Stage (t_o, t_1): During this stage, power is transferred to the load from the input sources V_1 and V_2 through switches S_1 and S_2 and also from the clamping capacitors C_{c3} and C_{c4} which discharge through the switches S_7 and S_8. In the secondary side of the transformer, the current flows through the rectifier diode D_{r1} and inductor filter L_{o2}. The switches S_3, S_4, S_5 and S_6 are in "off" state and the voltage across them is equal to the voltage V_c across the clamping capacitors C_{c1}, C_{c2}, C_{c3} and C_{c4}.

Second Stage (t_1, t_2): At instant t_1, switches S_1 and S_2 are tuned-off simultaneously with zero voltage. Capacitors C_{r1} and C_{r2} begin to charge and the capacitors C_{r5} and C_{r6} begin to discharge, both linearly with a constant current. This stage finishes when the voltages over S_1 and S_2 are V_1 and V_2, and over S_5 and S_6 are V_c-V_1 and V_c-V_2.

Third Stage (t_2, t_3): At instant t_2, the transformer voltage is zero, and consequently, the capacitors C_{r1}, C_{r2}, C_{r5} and C_{r6} begin the resonance with L_{r1} and L_{r2}. Also, the freewheeling process of the output current I_o starts involving L_{o1}, L_{o2}, D_{r1} and D_{r2}. When the voltages across S_1 and S_2 reach V_c and across S_5 and S_6 reach zero, this stage finishes.

Fourth Stage (t_3, t_4): At instant t_3, anti-parallel diodes D_5 and D_6 are directly biased and start conducting the current through L_{r1} and L_{r2}, which decrease linearly. In the same manner, the currents through L_{r3} and L_{r4} decrease linearly. During this stage the load current I_o keeps freewheeling through the diodes D_{r1} and D_{r2}. Switches S_5 and S_6 must be gated on before diodes D_5 and D_6 are reversely biased. This stage finishes when switches S_7 and S_8 are turned off.

Fifth Stage (t_4, t_5): When switches S_7 and S_8 are turned off, the currents through L_{r3} and L_{r4} are deviated to resonant capacitors C_{r3}, C_{r4}, C_{r7} and C_{r8}. These capacitors are discharged and charged in a resonant way. During this stage the load current keeps freewheeling. This stage finishes when voltages across S_3 and S_4 are null, across S_7 and S_8 reach V_c, and diodes D_3 and D_4 start to conduct.

Sixth Stage (t_5, t_6): At the instant t_5, diodes D_3 and D_4 are directly biased and begin conducting the resonant inductor currents iL_{r3} and iL_{r4}. During this condition, the switches S_3 and S_4 must be gated on. The currents through L_{r3} and L_{r4} decrease linearly until reaching zero. At this point, diodes D_3 and D_4 are blocked, and the referred currents invert their direction, flowing through switches S_3 and S_4. During this stage there is no power transferred to the load; therefore, only a reduction in the duty cycle occurs.

III. Theoretical Analysis

A. Clamping Characteristic

The clamping voltage and input voltage ratio (V_c/V_i) can be obtained determining the average voltage across the main switch S_1 and applying loop voltage equations. Therefore,

$$\frac{V_c}{V_i} = \beta = \frac{2}{(2 - D)} \tag{1}$$

The clamping characteristic is shown in Fig. 14.

B. Output Characteristics

In the proposed converter the duty cycle reduction, is reflected in the transformer secondary voltage (Fig. 2). This case occurs due to the presence of external resonant inductors and transformer leakage inductances. During this condition, power is no transferred to the load from the input.

According to the waveforms shown in Fig. 2, and considering that the commutation time is much smaller than the switching period, the average output voltage is given by

$$V_o = V_{sec} \cdot \left(\frac{D}{2} - \frac{\Delta t_1}{T_S} \right) \tag{2}$$

$$V_{sec} = n \cdot \frac{V_C}{2} \tag{3}$$

where:
V_o : output voltage;
D: duty cycle;
V_c : clamping voltage;
T_s : switching period;
V_{sec} : transformer secondary voltage;
n: transformer turns ratio (N_s/N_p);
Δt_1 : no power transfer time interval (sixth stage).
The no power transfer interval in half period is,

$$\Delta t_1 = \frac{n \cdot I_o \cdot L_r \cdot (2 - D)}{4 \cdot V_i} \tag{4}$$

The reduction of duty cycle in the period T_s is given by

$$\Delta D = \frac{2 \cdot \Delta t_1}{T_S} \tag{5}$$

Substituting (4) into (5), yields

$$\Delta D = \frac{f_s \cdot n \cdot I_o \cdot L_r \cdot (2 - D)}{2 \cdot V_i} \quad (6)$$

Substituting (1), (3) and (4) into (2), the average output voltage is obtained as

$$V_o = n \cdot V_i \cdot \left[\frac{D}{2 \cdot (2 - D)} - \frac{f_s \cdot L_r \cdot n \cdot I_o}{4 \cdot V_i} \right] \quad (7)$$

The plot of the output voltage V_o as a function of the output current I_o, known as output characteristic, is shown in Fig. 13.

C. Commutation Analysis

This converter presents soft turn-on and turn-off commutation during its operation.

Turn-on : for analytical purposes, the commutation between main switch S_3 and auxiliary switch S_7, during the fifth stage, is considered.

Equation (8) is obtained for no load (critical) operation condition. Therefore,

$$\theta_{on} = tg^{-1}\left[\frac{-\pi \cdot (1 - D)}{2 \cdot \bar{f}} \right] + \cos^{-1}\left[\frac{-2 \cdot \bar{f} \cdot (2 - D)}{D \cdot \sqrt{\left[\pi \cdot (1 - D)\right]^2 + 4 \cdot \bar{f}^2}} \right] \quad (8)$$

$$\bar{f} = \frac{f_s}{f_o} \quad (9)$$

$$\theta_{on} = \omega_o \cdot t_{on} \quad (10)$$

where:

$\bar{f}$:switching frequency and resonance frequency ratio

θ_{on} : displacement angle of the oscillation frequency

t_{on}: discharge time interval of the commutation capacitors C_{r3} and C_{r7}, where, $C_{req}=C_{r3}+C_{r7}$.

Displacement angle θ_{on} as a function of $\bar{f}$ during the turn-on is shown in Fig. 3.

The discharge and charge time interval of the commutation capacitors C_{r3} and C_{r7} is given by

$$t_{on} = \frac{\theta_{on} \cdot \bar{f}}{2 \cdot \pi \cdot f_S} \quad (11)$$

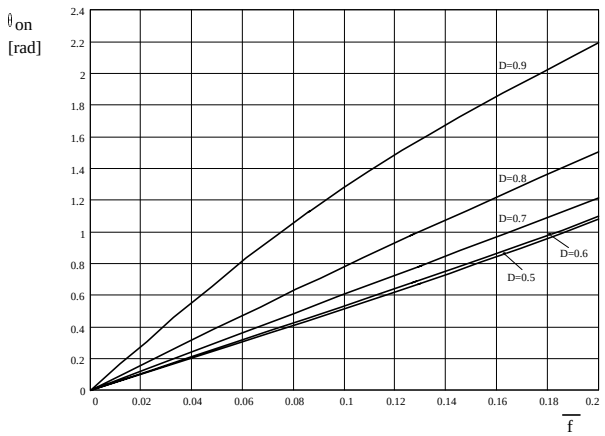

Fig. 3. Displacement angle θ_{on} as function of $\bar{f}$ during turn-on.

Turn off: In this case, the turn-off of the switches S_1 and S_5, which happens in the second and third stages is analyzed. During this commutation, capacitors C_{r1} and C_{r5} are charged and discharged.

Equation (12) is also obtained for no load (critical) operation condition. Therefore,

$$\theta_{off} = \frac{2 \cdot (2 - D) \cdot \bar{f}}{\pi \cdot D \cdot (1 - D)} + sen^{-1}\left[\frac{2 \cdot \bar{f}}{\pi \cdot (1 - D} \right] \quad (12)$$

$$\theta_{off} = \omega_o \cdot t_{off} \quad (13)$$

Displacement angle θ_{off} as a function of $\bar{f}$ during the turn-off is shown in Fig. 4.

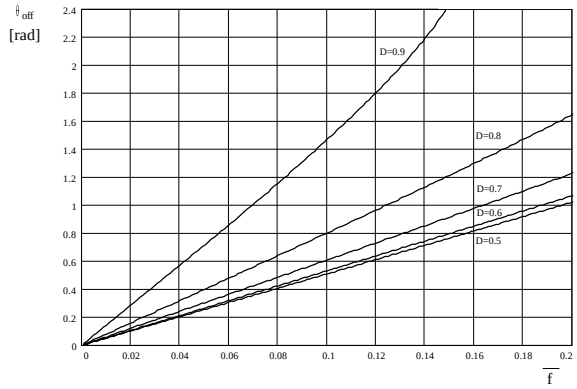

Fig. 4. Displacement angle θ_{off} as function of $\bar{f}$ during turn-off.

The charge and discharge time interval of the commutation capacitors C_{r1} and C_{r5} is given by

$$t_{off} = \frac{\theta_{off} \cdot \bar{f}}{2 \cdot \pi \cdot f_S} \quad (14)$$

IV. Simplified Design Example

A methodology and design procedure is presented in this section.

A. Input Data

Po=3000W output power 4Vi=800V input voltage; Vo=60V output voltage; Io=50A output current; fs=25kHz switching frequency.

B. Determination of passive components

Assuming ideal switches and diodes and considering:

D_{max} =0.8 maximum duty cycle

ΔD_{max} =0.18 maximum duty cycle reduction

The transformer turns ratio is calculated from (7)

$$n = \frac{N_S}{N_P} = \frac{2 \cdot (2 - D_{max})}{(D_{max} - \Delta D_{max})} \cdot \frac{V_o}{V_i} = \frac{2 \cdot (2 - 0.8)}{(0.8 - 0.18)} \cdot \frac{60}{200} = 1.16$$

The clamping voltage is calculated from (1)

$$V_C = \frac{2}{(2 - D_{max})} \cdot V_i = \frac{2}{(2 - 0.8)} \cdot 200 = 333.34V$$

1). Resonant inductor L_r: The resonant inductor is defined by the specified maximum reduction of duty cycle and is calculated from (6).

$$L_r = \frac{2 \cdot V_i \cdot \Delta D_{max}}{f_s \cdot n \cdot I_o \cdot (2 - D_{max})} = \frac{2 \cdot 200 \cdot 0.18}{25 \cdot 10^5 \cdot 1.16 \cdot 50 \cdot (2 - 0.8)} = 41.4\mu H$$

2). Clamping capacitor C_c: To determine the capacitance, it is considered that the resonance period of the clamping capacitor and resonance inductor corresponds to three times the switching period T_s. Therefore,

$$2 \cdot \pi \cdot \sqrt{L_r \cdot C_C} = 3 \cdot T_s$$

$$C_C = \frac{2.25}{\pi^2 \cdot L_r \cdot f_s^2} = \frac{2.25}{\pi^2 \cdot 41.4 \cdot 10^{-6} \cdot (25 \cdot 10^3)^2} = 8.8\mu F$$

3). Resonant capacitor C_{req}: To determine the capacitance, it is necessary to find the oscillation frequency between L_r and C_{req}. For this purpose, equation (12) and (14) are used. Assuming the

commutation time interval, during turn-off in no load situation, as 1% of T_s (400ns) and being the minimum duty cycle D_{min}=0.68, values of θ_{off} and $\bar{f}$ are:

$$\theta_{off} = 0.61\text{rad}$$
$$\bar{f} = 0.104$$

The oscillation frequency is obtained from equation (9),

$$f_o = \frac{25 \cdot 10^3}{0.104} = 240.4\text{kHz}$$

Therefore,

$$C_{req} = (C_{r1} + C_{r5}) = \frac{1}{41.4 \cdot 10^{-6} \cdot \left(2 \cdot \pi \cdot 240.4 \cdot 10^3\right)^2} = 10.59\text{nF}$$

4). Output filter: The output filter can be calculated in the same way as for a conventional full-bridge converter. This filter is designed for a maximum current ripple ΔI_{Lo1}=2.5A (10% of $I_o/2$) and a maximum voltage ripple ΔV_o=0.48 (0.8% of V_o).

$$L_{o1} = L_{o2} = \frac{V_O \cdot (1 - D_{min})}{2 \cdot f_S \cdot \Delta I_{Lo}} = \frac{60 \cdot (1 - 0.68)}{2 \cdot 25 \cdot 10^3 \cdot 2.5} = 153.6\mu\text{H}$$

$$C_o = \frac{2 \cdot \Delta I_{Lo1}}{2 \cdot \pi \cdot f_S \cdot \Delta V_O} = \frac{2 \cdot 2.5}{2 \cdot \pi \cdot 25 \cdot 10^3 \cdot 0.48} = 66.3\mu\text{F}$$

The maximum allowable series resistance for the output capacitor C_o is:

$$R_{SE} = \frac{\Delta V_o}{2 \cdot \Delta I_{Lo1}} = \frac{0.48}{2 \cdot 2.5} = 0.096\Omega$$

C. Semiconductors voltage and current stresses

1). Main and auxiliary switches: the maximum voltage across the switches is:

$$V_{S1,..S8} = \frac{2 \cdot V_i}{(2 - D_{max})} = \frac{2 \cdot 200}{(2 - 0.8)} = 333.34\text{V}$$

The average current through the main switches (S_1,..S_4) and auxiliary switches (S_5,..S_8) can be calculated by means of the normalized current values determined in [8]; for ΔD_{max}=0.18 we have:

$$\overline{I_{S1,..S4_{avg}}} = 0.0225$$

$$\overline{I_{S5,..S8_{avg}}} = 0.0075$$

Hence,

$$I_{S1,..S4_{avg}} = \frac{V_i}{f_s \cdot L_r} \cdot \overline{I_{S1,..S4_{avg}}} = \frac{200}{25 \cdot 10^3 \cdot 41.4 \cdot 10^{-6}} \cdot 0.0225 = 4.38\text{A}$$

$$I_{S5,..S8_{avg}} = \frac{V_i}{f_s \cdot L_r} \cdot \overline{I_{S5,..S8_{avg}}} = \frac{200}{25 \cdot 10^3 \cdot 41.4 \cdot 10^{-6}} \cdot 0.0075 = 1.45\text{A}$$

2). Output rectifier diodes: in the output rectifier, the diode reverse voltage is:

$$V_{Dr1,Dr2} = n \cdot \frac{V_i}{(2 - D_{max})} = 1.16 \cdot \frac{200}{(2 - 0.8)} = 193.34\text{V}$$

The interaction of the transformer leakage inductance with the rectifier capacitance during the reverse-recovery processes causes overshoots of the diode reverse voltage. The overshoots can be controlled using soft-recovery rectifiers and a clamping circuit such as shown in Fig. 7.

The diode's average current is given by

$$I_{Dr1,Dr2_{avg}} = \frac{I_o}{2} = \frac{50}{2} = 25.0\text{A}$$

V. Design Considerations

A. Parameters and Layout of the Prototype

To obtain good current distribution through the four forward converters, it is necessary to maintain symmetry in the power circuit layout, control circuit layout and same values of the components, such as: external and leakage inductances, capacitances, semiconductors, etc. With these recommendations, in the proposed converter, the difference observed between pulse widths of the switches is negligible. Therefore, no influence in the current distribution through the circuits was observed.

B. High Frequency Transformer

To obtain symmetrical leakage inductance distribution among the primary windings, multi-winding transformer design theory was applied [4,9]. Construction details of the five-winding transformer used in the prototype are shown in Fig. 5.

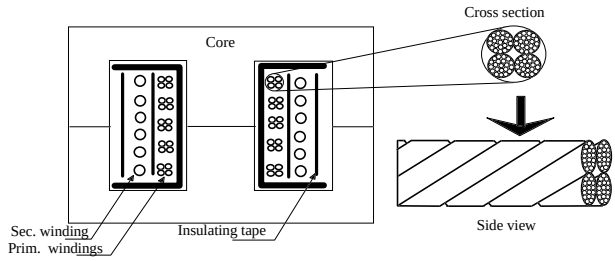

Fig. 5. Symmetrically five-winding transformer structure.

C. Coupled Resonant Inductors

To obtain equal resonant inductances values, the inductors L_{r1} and L_{r2} are coupled in the same core, as well as the inductors L_{r3} and L_{r4}. When this technique is utilized, the self-inductances of each inductor must be half of the value calculated in the simplified design example section (20.7uH), and the other half is the mutual inductance (≈20.7uH). For inductor design, the leakage transformer inductance is subtracted of the self-inductance. In the prototype, the leakage transformer inductance is around 1.35μH. The inductor construction details are shown in Fig. 6.

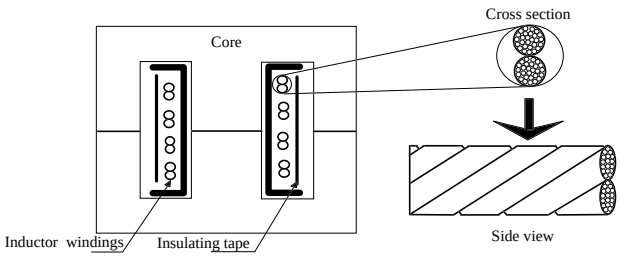

Fig. 6. Symmetrically coupled resonant inductor structure.

VI. EXPERIMENTAL RESULTS

To verify the practical aspects of the proposed converter, a prototype was built with the following components:

S_1,..S_8	IRG4PC50W - 600V, 27A, IGBT
D_{r1}, D_{r2}	HFA50PA60C - 600V, 50A ultra-fast diode
D_1,..D_8	MUR440 - 400V, 4A ultra-fast diode
D_{a1},..D_{a8}	MUR140 - 400V, 1A ultra-fast diode
C_{c1},..C_{c4}	8µF/400V - polypropylene capacitor
C_1,..C_4	3300µF, 350V - electrolytic capacitor
C_{r1},..C_{r4}	6.8nF/630V - polypropylene capacitor
C_{r5},..C_{r8}	2.7nF/630V - polypropylene capacitor
C_o	880uF/63V - electrolytic capacitor
T_r	Ferite core EE76/76 - IP12 / Thornton; N_P=14 turns, N_S= 16 turns
L_{o1}, L_{o2}	153.6µH - Ferrite core EE65/26; IP12 / Thornton; N_{Lo1}=N_{Lo2}=27 turns
L_{r1},..L_{r4}	41.4µH - Ferrite core EE55 IP12 / Thornton; N_{Lr1}=N_{Lr2}=N_{Lr3}=N_{Lr4}=10 turns.
C_{Dr1}, C_{Dr2}	0.1µF, 630V - polypropylene capacitor
R_{Dr1}, R_{Dr2}	33kΩ/ 5W - resistor
D_{Dr1}, D_{Dr2}	MUR440 - ultra-fast diode

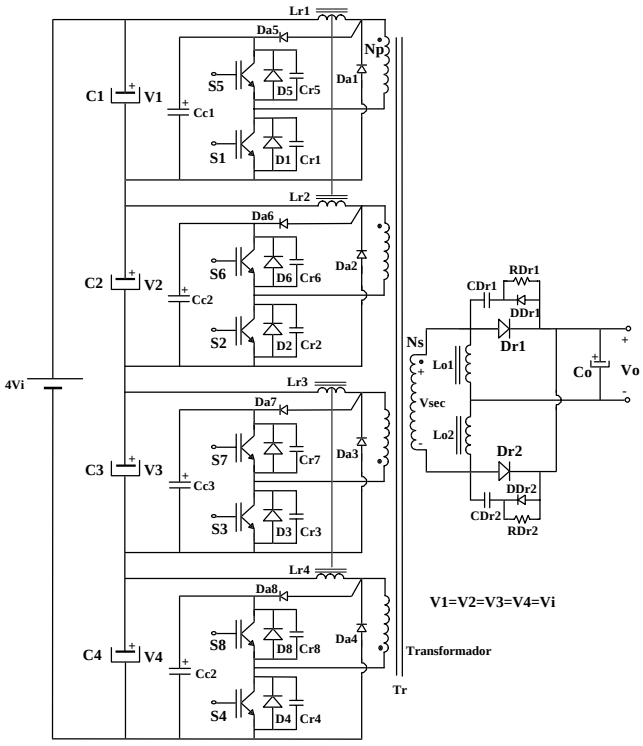

Fig. 7. Circuit diagram of the laboratory prototype.

In this section experimental waveforms obtained for an output power of P_o=3000W and P_o=62W are presented.

The waveforms obtained for P_o=3000W are shown in Figs. 8 and 9. Waveforms obtained for P_o=62W are shown in Figs. 10 and 11. These results confirm the soft commutation of the converter.

The current distribution through the composed circuits is shown in Fig. 12. The output characteristic, the clamping characteristic and the efficiency of the converter are shown in Figs. 13, 14 and 15 respectively. These experimental waveforms confirm the theoretically predicted results.

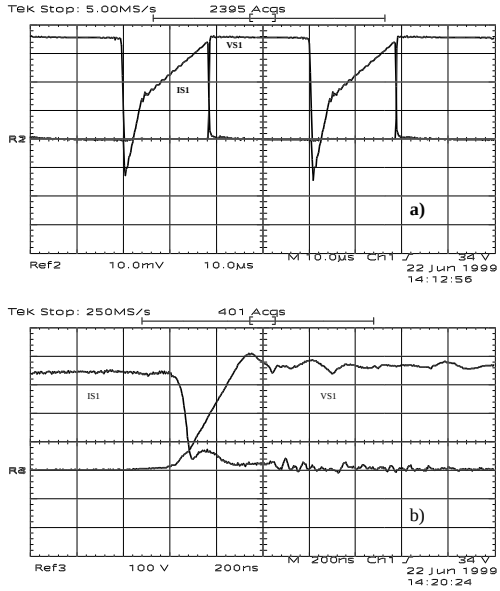

Fig. 8. a) Voltage and current in main switch S_1. (100V/div.; 5A/div.; 10us/div.)
b) Turn-off detail of the main switch S_1. (100V/div.; 5A/div.; 200ns/div.)

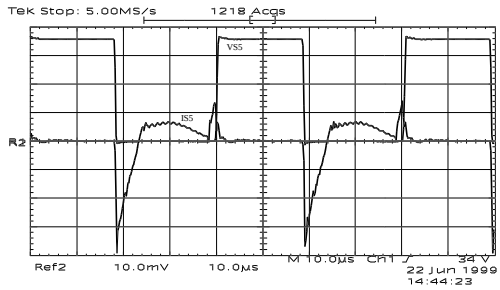

Fig. 9. Voltage and current in auxiliary switch S_5. (100V/div.; 5A/div.; 10us/div.)

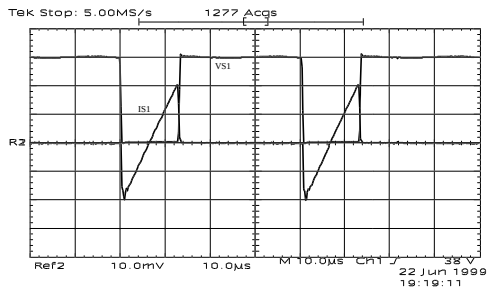

Fig. 10. Voltage and current in main switch S_1. (100V/div.; 5A/div.; 10us/div.)

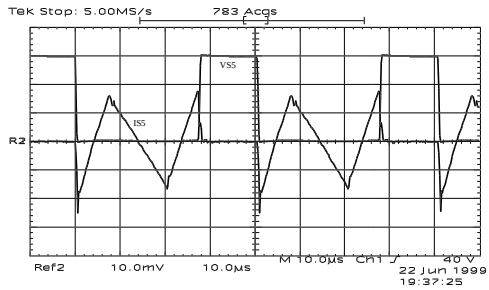

Fig. 11. Voltage and current in auxiliary switch S_5. (100V/div.; 5A/div.; 10us/div.)

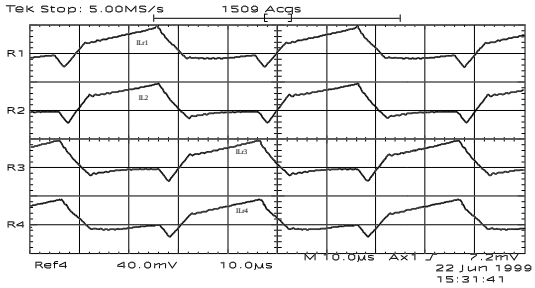

Fig. 12. Current through the inductors L_{r1}, L_{r2}, L_{r3} and L_{r4}. (20A/div.; 10us/div)

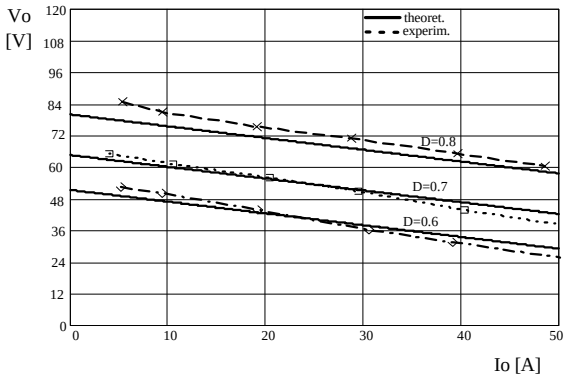

Fig. 13. Output characteristic of the converter.

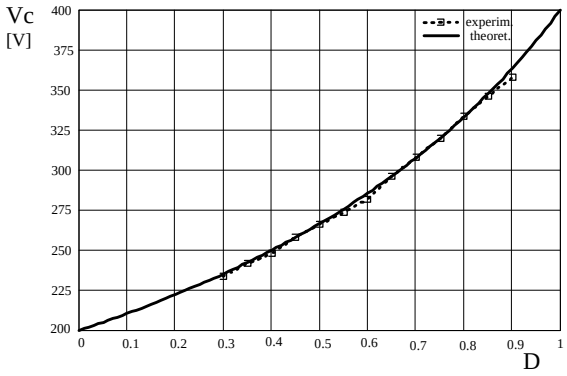

Fig. 14. Clamping characteristic of the converter.

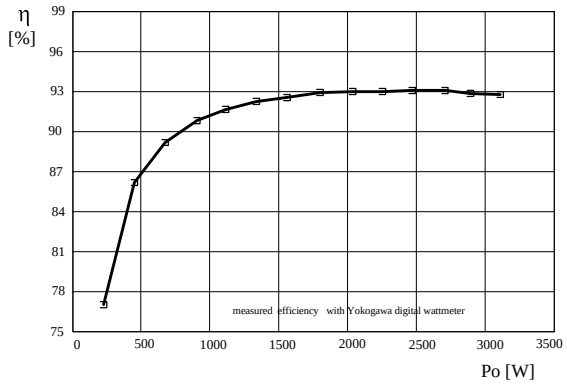

Fig. 15. Measured efficiency of the converter.

VII. CONCLUSIONS

A dc-dc converter for high input bus voltage application based in four single ZVS-PWM active-clamping forward converters was proposed in the paper. Analysis of the clamping characteristic, output characteristic, commutation characteristic, simplified design example, design considerations and experimental results are presented.

Experimental results show that the converter presents the following features:

- Soft commutation of all the controlled switches for any load current.
- The power flow from the input to the output is controlled with only four switches, S_1, S_2, S_3 and S_4. In this way, conduction losses of the converter are low. Besides, the current flowing through the auxiliary switches S_5, S_6, S_7 and S_8 is very low.
- Voltage overshoots across the switches caused by the transformer leakage inductance are eliminated by the use of active clamping circuits.
- Good distribution of the current through the composed circuits is observed.
- Good sharing of the voltage across the input capacitor is observed.
- Efficiency of the converter is around of 93%.

VIII. REFERENCES

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