A Three-Phase Series-Parallel Compensated Line-Interactive UPS System with Sinusoidal Input Current and Sinusoidal Output Voltage

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Abstract - This paper deals with a three phase line-interactive uninterruptible power supply system with active series-parallel power-line conditioning capability, which has sinusoidal output voltage regulation capability and unit power factor.

In this system two active power filter topologies are applied. The first one is a series active power filter, which can compensate supply voltage harmonics and voltage unbalances as well. The other is a parallel active power filter, which has the following main goals: reactive power compensation, load current harmonics suppression, and battery bank charging during normal power supply conditions. During input power failure, the parallel filter maintains uninterruptible power for critical loads, delivering power from the battery bank without power interruption, ensuring sinusoidal output voltages with constant rms voltage value and low Total Harmonic Distortion (THD). Therefore the proposed line-interactive UPS has low THD sinusoidal input currents with unit power factor. The control algorithm and mathematical models of the proposed three-phase line-interactive UPS system are described, and digital simulations are presented to verify the good dynamic responses of the versatile scheme.

I. INTRODUCTION

Uninterruptible Power Supplies (UPS's) have been largely used to improve power source quality as well as to protect critical loads such as computers, industrial control systems, communication systems, medical equipment, etc, against power outages by providing clean and uninterrupted power under power supply disturbances or interruptions. Under normal or abnormal line conditions, the purpose of the ideal UPS system is to act as a sinusoidal output voltage with constant RMS value and low THD to either linear or non-linear loads. Another important characteristic of the ideal UPS system is to provide seamless transition when a failure occur and low THD sinusoidal input current with unit power factor.

Depending on the configuration adopted, UPS systems are usually classified as OFF-LINE, ON-LINE or Line-Interactive, as shown in Fig. 1. The advantages and drawbacks of each scheme have been related in other papers [1], [2].

A line-interactive UPS with active power-line conditioning capability has been proposed [3], in which a parallel active power filter was used to eliminate any current harmonics injected from non-linear loads into the supply system during the normal line condition. The regulation and elimination of the voltage harmonics from the power line voltage were not considered, and in backup mode, the output voltage is not purely sinusoidal and with high THD.

Series-parallel UPS systems with universal filtering capabilities have been proposed as a single-phase mode [1] and as a three-phase mode [2]. In both topologies the series converter was used to control the input line current and the parallel converter was used to control the output voltage either in standby or backup mode.

This paper presents a three-phase line-interactive UPS with active series-parallel power-line conditioning capability, which has sinusoidal output voltage regulation capability in standby or backup mode and high input power factor with low input current and output voltage THD.

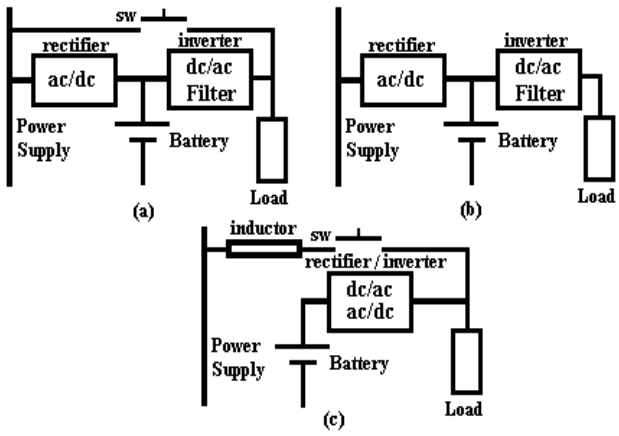

Fig. 1. UPS Topologies. (a) OFF-LINE UPS; (b) ON-LINE UPS; (c) Line-Interactive UPS.

The main advantage of the proposed line-interactive UPS topology, as compared to on-line topology (Fig. 1b), which uses two PWM power converters working at full rating power, is the smaller power rating of the series active power filter, increasing the efficiency of the system and reducing its cost. Besides this, under normal line conditions, the power rating of the parallel converter is smaller than the nominal power rating of the load because it works to eliminate any current harmonic produced by the non-linear load. Therefore the efficiency and the Maximum Time Between Fail (MTBF) of the structure is increased.

Despite the fact that the proposed line-interactive UPS topology owns two PWM power converters, one in series and the other in parallel to the load, it has advantages as compared to the line-interactive UPS topology shown in Fig. 1c. This makes it impossible to control input line current and the output voltage simultaneously, and thus decreasing the quality of the energy delivered to the load.

II. Proposed topology

The proposed line-interactive UPS system topology is shown in Fig. 2. Similar series-parallel topologies have been used in other applications such as Unified Power Quality Conditioners (UPQC) [4] and Unified Power-Flow Control (UPFC) [5], which aims at the integration of series and parallel active filters.

In this paper a battery bank is placed in the DC bus and a fast static switch is incorporated to the circuit to provide a fast disconnection between the UPS and the power supply when an occasional interruption of the incoming power occurs.

Two PWM converters, coupled with a common DC link are used to carry out the series active filter and parallel active filter functions.

The series active filter is implemented to compensate voltage harmonics and voltage unbalances as well, providing a regulated output voltage and harmonic-free to the critical loads. The parallel active filter placed in parallel to the load has the following main goals: reactive power compensation, load current harmonics suppression, and battery bank charging during normal power supply. Moreover, this parallel filter, during a power supply interruption, maintains uninterruptible power for critical loads, delivering power from the battery bank without power interruption, and ensuring sinusoidal output voltages with constant rms voltage value and low THD. Thus, when incoming power loss occur, the parallel PWM inverter provides a phase-synchronized voltage to the critical loads. Therefore, in case the power supply returns to normal conditions, the static switch transfers the load from parallel PWM converter to the phase-synchronized series PWM converter with seamless transition.

III. Series active filter controller

Traditionally, the series active filters have been applied for isolating harmonic currents with small power ratings, combined with a parallel passive filter [6], [7].

In the proposed UPS system, the series active filter is applied to compensate input voltage unbalances and voltage harmonics. This can improve the power quality offered for other harmonic sensitive loads. As shown in Fig. 2, the series PWM converter is connected by three single-phase transformers to perform the series connections and it behaves as a controlled non-sinusoidal voltage source.

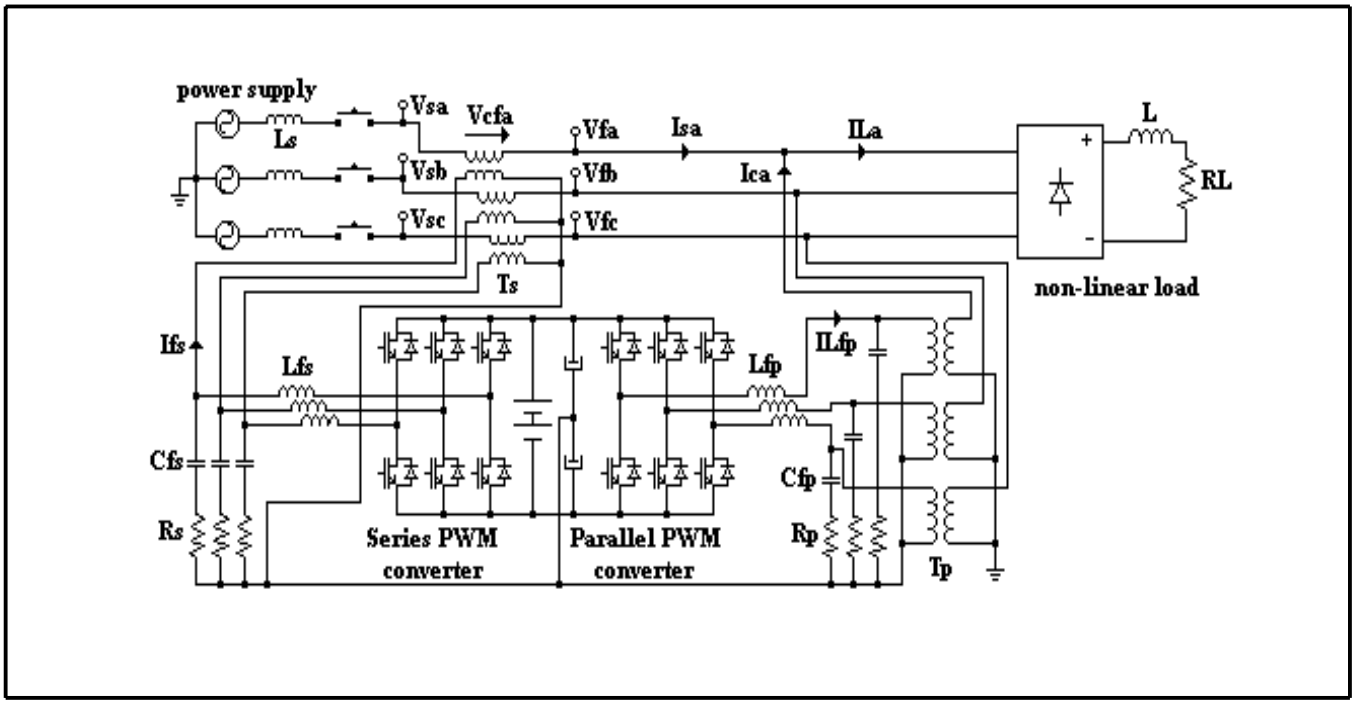

Fig. 2. Proposed line-interactive UPS system topology.

A. Control algorithm for voltage compensation

The block diagram of the SRF and AC Output Voltage Controllers for voltage compensation is shown in Fig. 3. For voltage compensation, the control algorithm should be developed to provide the compensating reference voltages (V^*ca, V^*cb, V^*cc) for the series active filter.

The three phase source voltages (Vsa, Vsb, Vsc), are transformed from three-phase into a two-phase stationary reference frame $(dq)^s$ quantities (vd^s , vq^s). Then, these quantities are transformed from two-phase stationary reference frame $(dq)^s$ into a two-phase synchronous rotating $(dq)^e$ reference frame (SRF), based on the transformation (1), where $\theta = \omega t$, is the time variant angle that represents the angular position of the reference frame [6]. The inverse transformation matrix from two-phase synchronous reference frame to two-phase stationary reference frame is given by (2).

$$\begin{bmatrix} vd^e \\ vq^e \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} vd^s \\ vq^s \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} vd^s \\ vq^s \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} vd^e \\ vq^e \end{bmatrix} \quad (2)$$

The voltage at the fundamental frequency ω is now a DC value and all the harmonics are transformed to non-DC quantities and can be filtered using a HPF, implemented by the filtering block as shown in Fig. 3. Thus, the AC components of the synchronous reference frame vdh^e, vqh^e are transformed into the stationary reference frame $(dq)^s$ and all the harmonic components of the input ac voltage (Vca, Vcb, Vcc) are yielded. The SRF method should be implemented using a phase-locked loop (PLL) circuit generating a synchronous reference externally.

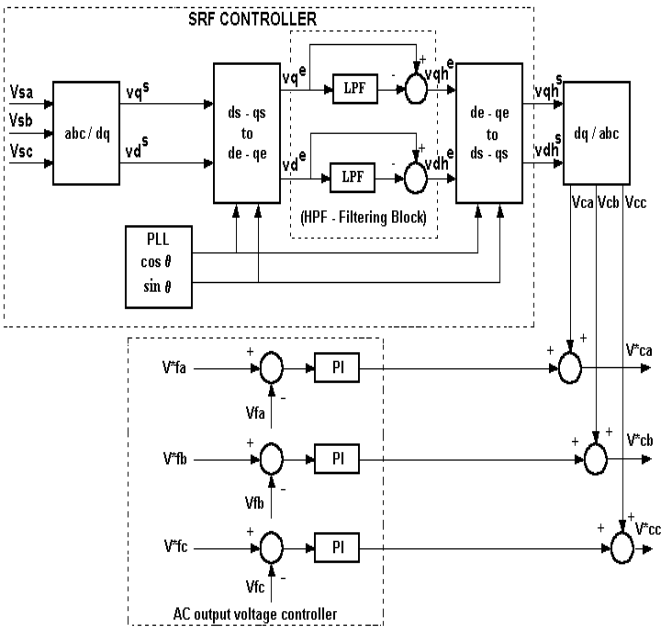

Fig. 3. Block diagram of the SRF and AC output voltage controllers.

Equations (3) and (4) show the matrices that provide the linear transformation of a three-phase system into a two-phase stationary reference frame system (abc/dq) and its inverse (dq/abc) respectively. The f variable denotes the current and/or voltage quantities.

$$\begin{bmatrix} fd \\ fq \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} fa \\ fb \\ fc \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} fa \\ fb \\ fc \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} fd \\ fq \end{bmatrix} \quad (4)$$

In order to provide a regulated input voltage Vfa, Vfb and Vfc (Fig. 2) at a desired value, an AC output voltage controller, as shown in Fig. 3, has been implemented. The output signal of the PI controller is added to the reference voltage harmonic Vca, Vcb, and Vcc compensating signals to generate the new reference signals V*ca, V*cb and V*cc.

Fig. 4 shows the simplified control block diagram for voltage compensation considering the reference voltages obtained from SRF controller.

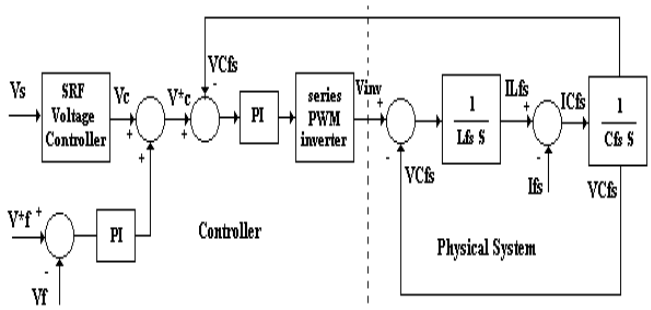

Fig. 4. Block diagram of the control scheme for voltage compensation.

IV. Parallel Active Filter Controller

During normal power flow, the main goals of the parallel PWM converter proposed in this paper are: functioning as a parallel active filter to compensate the load current harmonics that would be injected from critical non-linear loads into the power supply; charging the battery bank. Depending on the application and the load characteristics, the algorithm strategy applied to the active power filter, can perform reactive power compensation.

Upon a power supply interruption a fast static switch is opened and the parallel PWM converter immediately deliveries power from the battery bank to the critical load. As in ON-LINE UPS systems, there is no power interruption to the critical load.

In this line-interactive UPS the parallel PWM converter behaves as a controlled non-sinusoidal current source.

A. Control algorithm for current compensation

The block diagram of the current compensation control scheme is shown in Fig. 5. As well as control algorithm for voltage compensation, the synchronous reference frame (SRF) method is used, and all the harmonic components of the load currents (Ica, Icb, and Icc) are yielded.

Thus, the reference harmonic currents (I*ca, I*cb, I*cc) are derived from the SRF compensator. At a fundamental frequency there will be a displacement factor between the input compensated current and the output compensated voltage introduced by the capacitor Cfp (Fig. 2) of the LC output filter. To overcome this unsuitable behavior of the parallel active filter, the measured load current ILa, ILb and ILc should be added to the capacitor reference current ICfpa, ICfpb and ICfpc respectively. In this case the synchronous rotating reference frame current of the 'q' axis (iq^e) should not be filtered. Then, the HPF of the 'q' axis should be eliminated in the SRF controller as shown in Fig. 5. To overcome additional sensor costs, the capacitors reference current are obtained directly from the reference output voltages (V*fa, V*fb and V*fc) in the control algorithm.

The cut-off frequency of the third orders low pass filter used in SRF controller is 30Hz. If the cut-off frequency is chosen lower, the closed loop system stability margin is improved but the transient response becomes slower.

V. DC LINK VOLTAGE CONTROL (battery bank voltage)

The DC bus voltage PI controller regulates the DC bus voltage to its reference voltage Vdc^* (Fig. 5). A reference current is provided by the PI controller to generate the real power transfer to regulate DC link voltage, and for inverter loss compensations. As shown in Figure 5, the PI controller output is added to the axis "d" harmonic current compensation (Idh^e). The smaller the unbalances and harmonic contents of the input voltage and the losses of the two PWM converters, the smaller the energy balance needed to regulate the DC bus voltage.

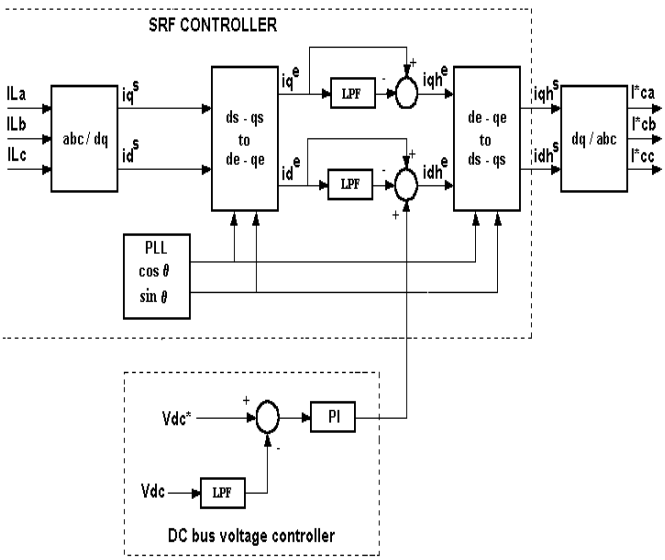

Fig. 5. Block diagram of the SRF and DC bus voltage controllers.

Fig. 6 shows the simplified control block diagram for current compensation considering the reference current obtained from SRF controller.

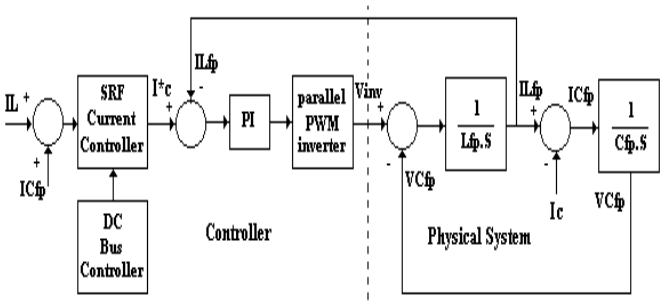

Fig. 6. Block diagram of the control scheme for current compensation.

VI. INVERTER MODE

When power supply is out, the parallel PWM converter delivers power from battery bank to critical loads. Fig. 7a shows the simplified single-phase equivalent model of the VSI-PWM converter operating as a voltage source (voltage-mode control). In this model the low-pass filter (Lfp-Cfp) introduces a delay time in the compensation of the measure output voltage signal occasioning output voltage distortion mainly when the PWM inverter is supplying non-linear loads [8].

In this work the PWM converter operates as a VSI with current-mode control. Thus it behaves as a high quality sinusoidal controlled current source for the output voltage control. Fig. 7b shows the simplified single-phase equivalent model of the voltage source inverter operating in current-mode control. The PWM voltage source inverter is combined with the filter inductor and it can be regarded as a current source (ILfp).

The control block diagram for the inverter mode is shown in Fig. 8. As the capacitor current (ICfp), load current (IL) and inductor current (ILfp) are involved in control loop, the output voltage will become less distorted.

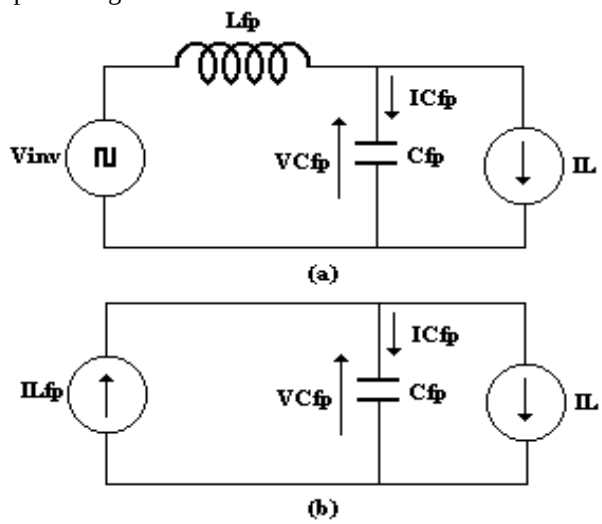

Fig. 7. Simplified single-phase equivalent model of the voltage source inverter.

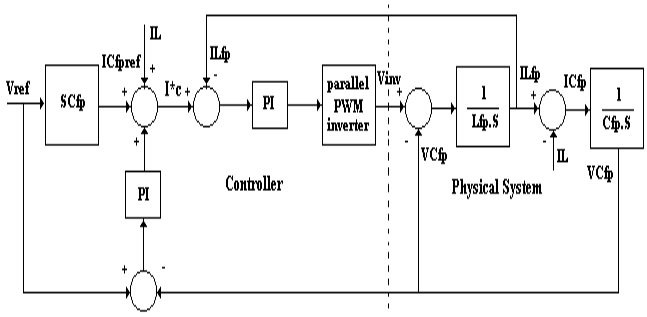

Fig. 8. Control block diagram for the inverter mode.

VII. Current and Voltage Regulators

As the series and parallel PWM inverter control loops are composed of three independent PI controllers, the reference harmonic currents (I*ca, I*cb, I*cc) and reference harmonic voltages (V*ca, V*cb, V*cc) are compared with their actual currents and voltages respectively. Thus, the resulting error (*ei*) is processed through a PI controller and the output error (*eo*) is compared with a triangular reference waveform, which has constant frequency and amplitude. The generic current and voltage regulator is shown in Fig. 9 considering only a phase.

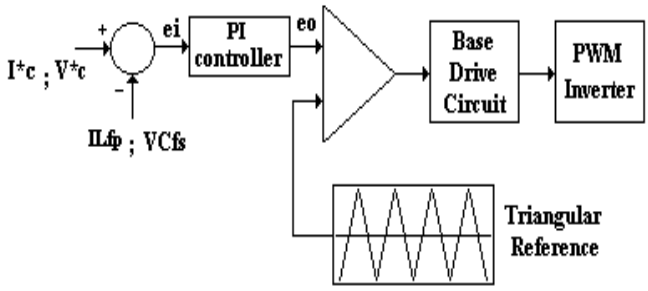

Fig. 9. Generic voltage and current regulators.

In both current and voltage regulators the error *eo* should be forced to remain between the maximum and the minimum amplitude of the triangular reference.

In order to avoid multiswitching and disturb the operation of the switches, the maximum slope of the error *eo* should be lower than the slope of the triangular reference waveform [9]. Then, an adequate design procedure considering the PI controller gains (Kp and Ki) and values of the inductor and capacitors filters is required.

VIII. Mathematical Simulations

The line-interactive UPS system was simulated considering a ±15% fundamental input voltage source unbalance under non-sinusoidal voltage conditions with fifth and seventh harmonics contents. The UPS system feeds a 21 KVA non-linear load represented by a there-phase diode rectifier bridge as shown in Fig. 2.

Firstly the proposed UPS system was simulated considering that the system works as a series-parallel compensated UPS with universal filtering capabilities. After that, the transition modes from standby to backup and from backup to standby mode were presented to show the dynamic behavior of the proposed scheme.

The passive element values and characteristics of the load and power system used in mathematical simulations are shown below as follows:

- *Parallel Active Power Filter:*

Cfp=180uF; Lfp=0.50mH; Rp=1Ω; Turns ratio of the Parallel Transformer: 1:1; PWM switching frequency: 20KHz

- *Series Active Power Filter:*

Cfs=280uF; Lfs=0.5mH; Rs=0.5Ω; Turns ratio of the Series Transformer: 1:1; PWM switching frequency: 20KHz.

- *Power System*

Ls = 25uH (1.3%); Input voltages: 15% unbalances; Nominal line-to-line input voltage: 220 Volts.

- *Non-linear Load (Diode Rectifier Bridge)*

L= 5mH; RL= 4 Ohm.

- *DC bus voltage*: Vdc = 500 Volts.

A . Standby mode simulations

1) Series Active Power Filter

The series active power filter was used to compensate the fifth and seventh harmonics contents of the input voltages and input voltage unbalances as well. Fig. 10 shows uncompensated three phases voltages (Fig. 10a) and the compensated three phases output voltages (Fig. 10b). It is noted that the three phase output voltages of the series active filter become balanced and harmonic-free with a regulated 127 volts RMS. Fig. 11 shows phase ‘a’ uncompensated input voltage (Vsa), compensation voltage (Vcfa) which follows its reference compensation voltage (V*ca) generated from the SRF controller and compensated output voltage (Vfa), respectively.

2) Parallel Active Power Filter

The parallel active filter acts as current power-line harmonic suppression, and the input current becomes sinusoidal and harmonic-free with a unit power factor (Fig. 14). In Fig. 12a the phase ‘a’ uncompensated load current (ILa) is shown. The harmonic compensation current (Ica) and its harmonic reference current (I*ca) generated from the SRF controller are shown in Fig. 12b. The compensated input current (Isa) is shown in Fig.12c. The harmonic compensation current and its harmonic reference current are shown with details in Fig. 13. As can be noted, there are saturation problems of the current regulator during the high *di/dt* of the uncompensated supply current due to rectifier commutations periods. This problem generates current spikes in compensated supply current as shown in Fig. 12c. The saturation of the current regulator can be partially overcome by increasing the inverter DC bus voltage magnitude that increases the UPS system cost.

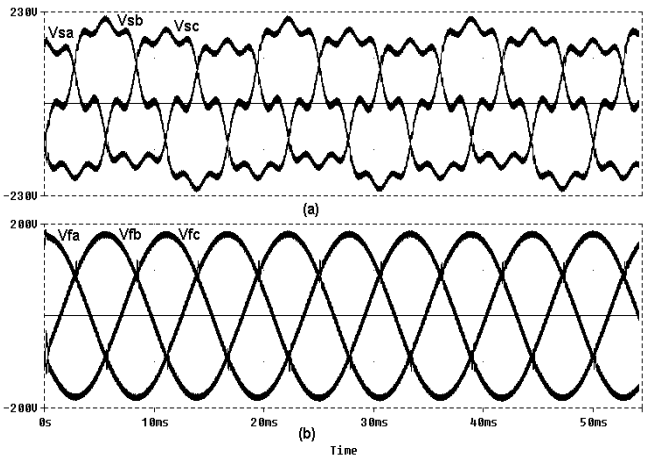

Fig. 10. (a) Three-phase uncompensated input voltages; (b) There-phase compensated output voltages.

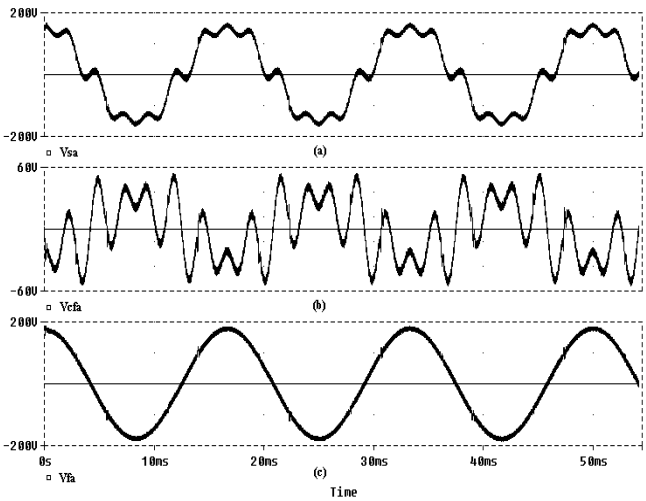

Fig. 11. (a) Phase 'a' uncompensated input voltage; (b) Phase 'a' compensation voltage; (c) Phase 'a' compensated output voltage.

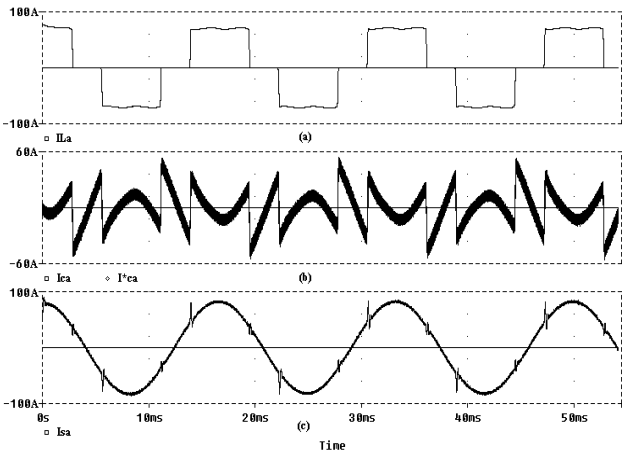

Fig. 12. (a) Phase 'a' uncompensated current; (b) Phase 'a' harmonic compensation current and harmonic reference current; (c) Phase 'a' compensated input current.

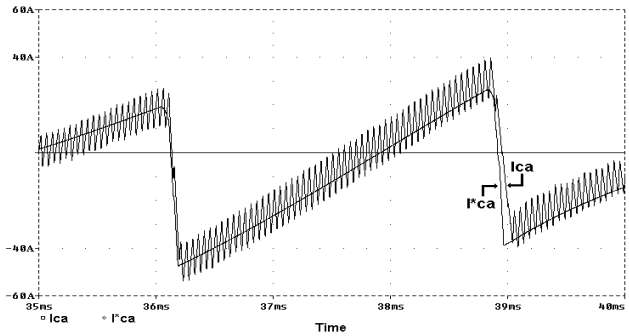

Fig. 13. Detail of the harmonic compensation current (Ica) and reference harmonic compensation current (I*ca).

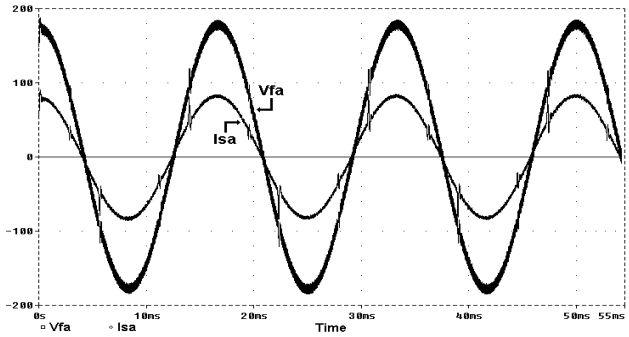

Fig. 14. Phase 'a' compensated output voltage (Vfa); Phase 'a' compensated input current (Isa).

Figs. 15a and 15b show phase 'a' supply current spectrum before and after harmonic compensation respectively. Before harmonic compensation the THD of the supply current was 29.63% and after the harmonic compensation from the parallel active power filter it was reduced to 4.13% which complies with the IEEE 519 harmonic standards. The harmonic spectrum of input and output voltage of the phase 'a' is shown in Fig. 16a and 16b respectively. The THD of the input voltage without voltage compensation was firstly 20.93% and after the harmonic compensation it was reduced to 0,76%. The THD values were considered up to the 50th harmonics for all the currents and voltages.

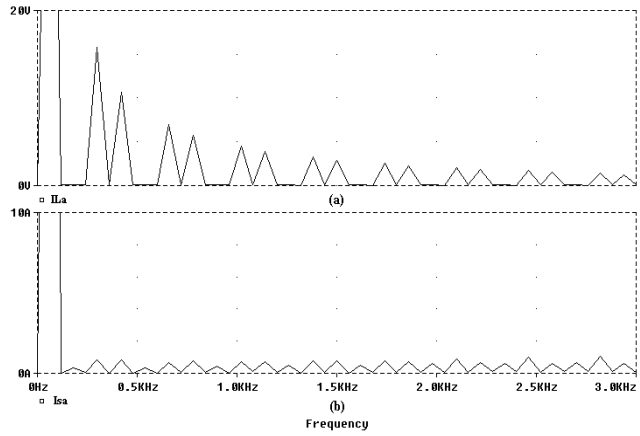

Fig. 15. Phase 'a' Harmonic Amplitude Spectrum: (a) uncompensated input current; (b) compensated input current.

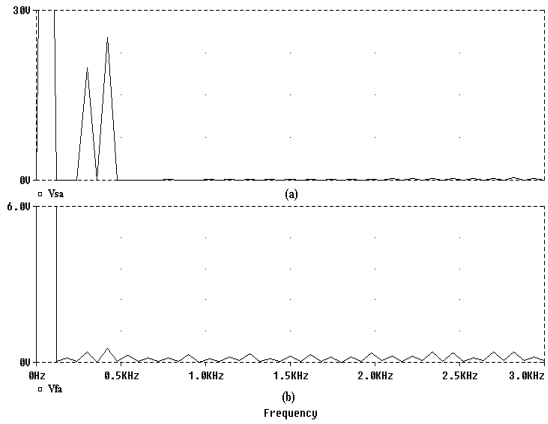

Fig. 16. Phase 'a' Harmonic Amplitude Spectrum: (a) uncompensated input voltage; (b) compensated output voltage.

B . Backup mode simulations

In Fig. 17 the transition modes from the standby mode to backup mode (18.33ms) and vice versa (35ms) are shown. The uncompensated load current is shown in Figure 17a. In Fig. 17b the harmonic compensation current (Ica) is shown. Note from the Fig. 17b that the parallel active filter is providing compensation harmonic current to the load when the UPS is operating in the standby mode until 18.33ms. After 18.33ms it assumes the total necessary current to provide power flow to the load. Seamless transitions from the standby mode to backup mode (18.33ms) and vice versa (35ms) are obtained as can be observed in the Fig. 17a (load current) and Fig. 17d (output voltage). The switching frequencies of the PWM converters are 20KHz. The detail of the transition modes is shown in Fig. 18a.

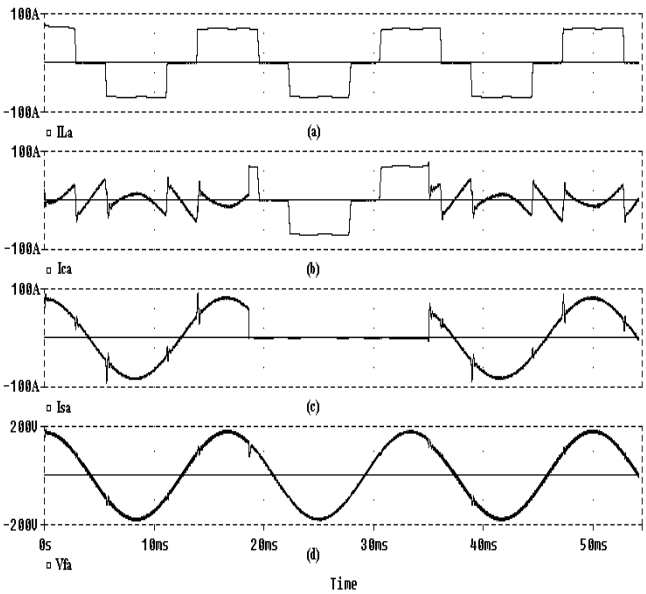

Fig. 17. (a) phase 'a' uncompensated current; (b) phase 'a' harmonic compensation current/output parallel active filter current; (c) phase 'a' compensated input current; (d) compensated output voltage.

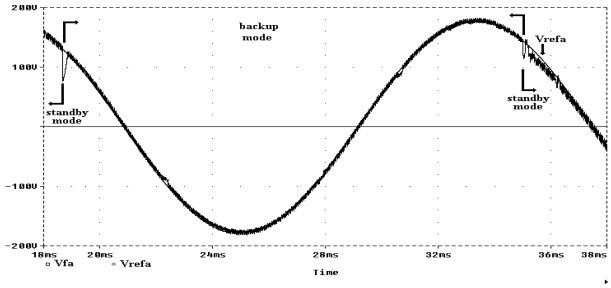

Fig. 18. Detail of the Phase 'a' transition modes – Output inverter voltage (Vfa) and output reference voltage Vrefa.

IX. Conclusions

This paper proposed a three-phase line-interactive uninterruptible power supply system with active series-parallel power-line conditioning capability, which has sinusoidal output voltage regulation capability and high input power factor.

The advantage of the proposed line-interactive UPS topology, as compared to on-line topology, which uses two PWM power converters working at full rating power, is the smallest power rating of the series active power filter which increases the efficiency of the system and reduces its cost.

The control algorithm and mathematical models were described and digital simulations were presented to verify the behavior of the proposed three-phase line-interactive UPS system. In standby mode, the results of the simulation show that UPS system works with low input current THD, low output voltage THD, regulated output voltage and unit power factor. In backup mode, the UPS system operates with regulated and low THD output voltage. The line-interactive UPS provided seamless transitions from the standby mode to backup mode and vice versa. This proposed UPS system is a good choice to be used at rating power higher than 20 KVA.

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