Power Factor Correction with Interleaved ZCS Boost Converters in Critical Conduction Mode

Carlos M. de O. Stein, José R. Pinheiro and Hélio L. Hey
UFSM - CT - DELC
97105-900 - Santa Maria - RS - Brazil
E-mail: cmstein@ieee.org, renes@pequim.ctlab.ufsm.br, hey@pequim.ctlab.ufsm.br

***Abstract* – A power-factor-correction (PFC) circuit based on the interleaved boost converters in critical conduction mode (C-DCM) with a zero current switching (ZCS) technique is investigated. The main switches turn-on occurs naturally in ZCS, due to the operation in C-DCM. In addition, the C-DCM also reduces the reverse recovery losses of the boost diodes. The use of the auxiliary commutation circuits provides ZCS at the main switches turn-off and they are only activated during the main switches commutations. By using the interleaved converters technique, the input current ripple is minimized. The control circuit of the converters has been implemented using a single Erasable Programmable Logic Device (EPLD) EPM7128SLC84-15 from Altera Corporation. The experimental results obtained using a 1.2 kW prototype operating from an AC input voltage source of 120 Vrms are presented.**

I. Introduction

In order to satisfy international standards such as IEC-1000-3-2, several active power factor correction (PFC) techniques have been developed. The PFC technique reduces the disturbances in utility systems caused by non-linear loads, especially current harmonics. Among the different alternatives, the boost converter used as front-end single-phase PFC circuit operating in continuous conduction mode (CCM) became the most popular approach [1,2]. The favorable aspects of this configuration are : set-up voltage conversion ratio, simple topology, high efficiency and continuous input current. However, the operation of the boost converter in CCM can present some drawbacks such as a high reverse recovery losses of the boost diode and the commutation losses. This results in higher EMI and reduces the efficiency of the converter [3]. Some papers has proposed the use the soft-switching techniques as a solution to overcome such drawbacks [8-10]. An another alternative to minimize the mentioned drawbacks, it is the use of interleaved boost converters operating in the discontinuous conduction mode (DCM) or critical conduction mode (C-DCM) [3-5]. The use of the interleaved technique allows the reduction of the conduction losses in the switches, maintaining a good quality of the input current. Moreover, the turn-on of the switches occur naturally under zero current (ZCS). However, the turn-off losses of the switches are not minimized, which happen under maximum current condition.

To improve the performance of the interleaved boost converters in C-DCM, this works investigate the use of the auxiliary commutation circuits which provides ZCS at the turn-off of the switches. With the use of these ZCS auxiliary commutation circuits is possible to improve the efficiency.

The operation of the ZCS auxiliary commutation circuits applied to interleaved boost converters is analyzed in Section II. In Section III, a design example is presented. Section IV shows the control circuit strategy which is implemented using the EPLD technology. The experimental results obtained from a 1.2 kW prototype operating with input AC voltage of 120 Vrms and an output DC voltage of 300 V are presented in Section V. The last Section summarizes the conclusions drawn from this investigation.

II. Principles of Operation

A. Interleaved ZCS Boost Converters

Figure 1 shows the proposed PFC interleaved ZCS boost converters. Each one of the boost cells presents an auxiliary commutation circuit composed by a resonant capacitor C_{R1} (C_{R2}), a resonant inductor L_{R1} (L_{R2}), and a bi-directional auxiliary switch S_{A1}-D_{A1} (S_{A2}-D_{A2}). Since the converters operate in a critical conduction mode (C-DCM), the turn-on of the main switches happens naturally in ZCS. The function of the auxiliary commutation circuit is to provide favorable conditions for the turn-off of the main switches under ZCS. The main characteristics of this topology are as follows:

- Commutation under ZCS at turn-on and under ZCS and ZVS at turn-off for the main and auxiliary switches;
- Commutation under ZCS and ZVS at turn-on and under ZCS at turn-off for the boost diodes;
- The auxiliary circuits are placed out of the main power path, and they are activated during the switching transitions of the main switches only;
- The input current ripple is reduced, when compared with an only boost converter operating in critical conduction mode;

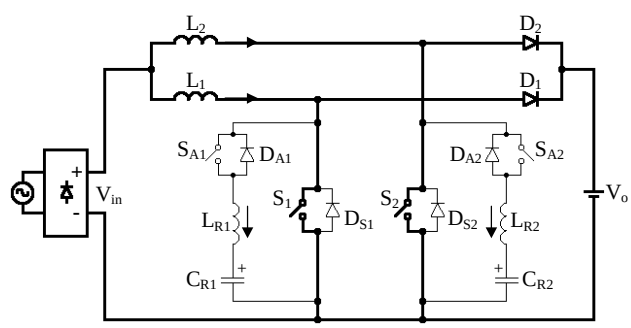

Fig. 1. Interleaved ZCS boost converters.

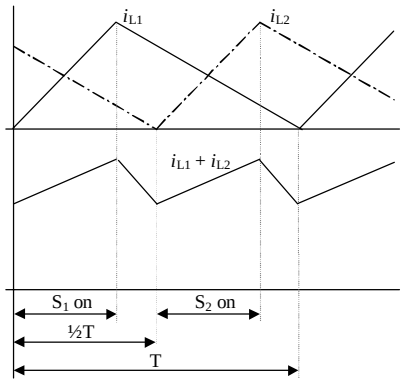

Fig. 2. Ideal waveforms of the inductors currents.

- The boost diodes reverse recovery losses are minimized;
- Operation in critical conduction mode (C-DCM).

Figure 2 shows the ideal waveforms of the currents in the inductors L_1 and L_2 operating in C-DCM. The input current waveform of the interleaved boost converters is given by the sum of $i_{L1}(t)$ and $i_{L2}(t)$, which is similar to the input current waveform of the boost converter operating in CCM. The minimum input current ripple is obtained by shifting the boost main switches gate signal by half switching period.

B. Variable Frequency Operation

In Fig. 3 a detail of the current in one of the boost inductors is represented. In this figure t_{on} is the main switch on-time, t_{off} is the conduction time of the boost diode and T is the switching period. The boost inductor currents should reach zero at the end of each period. Therefore:

$$\left|\Delta i_{t_{on}}\right| = \left|\Delta i_{t_{off}}\right| \qquad (1)$$

The input voltage is defined as:

$$V_{in}(t) = V_p \sin(\omega t) \qquad (2)$$

Then:

$$\frac{V_p \sin(\omega t)\cdot t_{on}}{L_1} = \frac{(V_o - V_p \sin(\omega t))t_{off}}{L_1} \qquad (3)$$

The switching frequency variation for the boost converter operation in C-DCM, can be obtained from expression (3) as follows:

$$f_S(t) = \frac{1 - a\sin(\omega t)}{t_{on}} \qquad (4)$$

where a is the ratio of the peak input voltage to DC output voltage and is given by:

$$a = \frac{V_p}{V_o} \qquad (5)$$

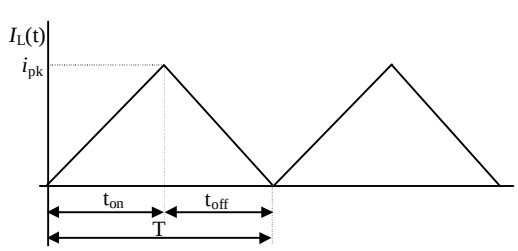

Fig. 3. Current in one of the boost inductors.

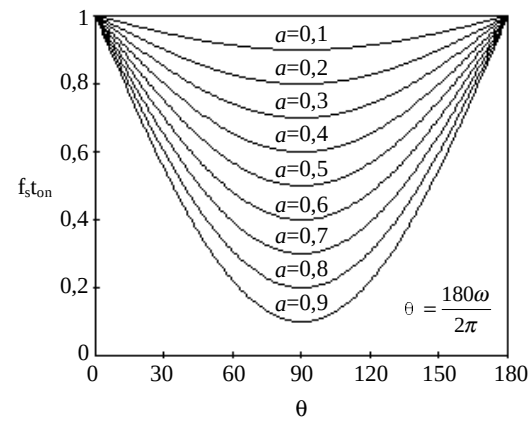

Fig. 4. Variation of the switching frequency.

In Fig. 4 is shown the switching frequency variation as function of the input voltage angle for different values of a.

C. Auxiliary Commutation Circuit

Taking into account that the boost converters operate without interactions among them, the operation principle of the interleaved ZCS boost converters is analyzed considering only one of the boost converters. In this analysis the output filter capacitor is assumed as a constant voltage source V_o during a switching period. Figure 5 shows the operating stages of the simplified ZCS boost converter during a switching cycle, and they are described as follows:

Stage 1. (t_0, t_1): During this stage the main switch S_1 is on and the input current $i_{L1}(t)$ flows through it increasing linearly. This stage is responsible by the power transference control. The resonant capacitor voltage $v_{CR1}(t)$ is clamped at $-V_{C0}$, where

$$V_{C0} = V_o - I_{in} Z_1 \qquad (6)$$

and

$$Z_1 = \sqrt{\frac{L_{R1}}{C_{R1}}} \qquad (7)$$

Stage 2. (t_1, t_2): At t_1, the auxiliary switch S_{A1} is turned on under ZCS. The current $i_{LR1}(t)$ increases due to the resonance between L_{R1} and C_{R1}. The current $i_{LR1}(t)$ evolves in a resonant way until it reaches $i_{L1}(t)$. The current $i_{LR1}(t)$ and the voltage $v_{CR1}(t)$ can be expressed as follows:

$$i_{L_{R1}}(t) = \frac{V_{C0}}{Z_1}\sin(\omega_1 t) \qquad (8)$$

$$v_{C_{R1}}(t) = -V_{C0}\cos(\omega_1 t) + V_o \qquad (9)$$

where

$$\omega_1 = \frac{1}{\sqrt{L_{R1} C_{R1}}} \qquad (10)$$

The duration of this resonant stage is equal to

$$\Delta_{t_2} = \frac{1}{\omega_1}\sin^{-1}\left(\frac{Z_1 I_{in}}{V_{C0}}\right) \qquad (11)$$

Stage 3. (t_2, t_3): This stage begins when the diode D_{S1} turns on, starting to drive the difference among the value of the current $i_{LR1}(t)$, in the inductor L_{R1}, and of the input current $i_{L1}(t)$. During this stage the main switch S_1 can be turned off under ZCS and ZVS. When $i_{LR1}(t)$ reaches the input current again, the diode D_{S1} turns off. The current $i_{LR1}(t)$ and the voltage $v_{CR1}(t)$ can be expressed as follows:

$$i_{L_{R1}}(t) = \frac{-V_{C2}}{Z_1}\sin(\omega_1 t) + I_{in}\cos(\omega_1 t) \quad (12)$$

$$v_{C_{R1}}(t) = V_{C2}\cos(\omega_1 t) + Z_1 I_{in}\sin(\omega_1 t) \quad (13)$$

where
$$V_{C2} = -\sqrt{V_{C0}^{\ 2} - (I_{in}Z_1)^2} \quad (14)$$

The duration of this resonant stage is equal to

$$\Delta_{t_3} = \frac{1}{\omega_1}\sin^{-1}\left(\frac{2Z_1 I_{in}\sqrt{V_o^{\ 2} - 2V_o Z_1 I_{in}}}{(V_o - Z_1 I_{in})^2}\right) \quad (15)$$

Stage 4. (t_3, t_4): During this stage the capacitor C_{R1} is linearly charged up to output voltage V_o by the input current. At this time the boost diode D_1 turns on. During this stage the voltage $v_{CR1}(t)$ is given by

$$v_{C_{R1}}(t) = V_{C3} + \frac{I_{in}}{C_{R1}}t \quad (16)$$

where
$$V_{C3} = -V_{C2} = \sqrt{V_{C0}^{\ 2} - (I_{in}Z_1)^2} \quad (17)$$

The duration of this resonant stage is equal to

$$\Delta_{t_4} = C_{R1}\frac{V_o - \sqrt{V_o^{\ 2} - 2V_o Z_1 I_{in}}}{I_{in}} \quad (18)$$

Stage 5. (t_4, t_5): The current $i_{LR1}(t)$ decreases due to the resonance between L_{R1} and C_{R1}. The current $i_{D1}(t)$ evolves in a resonant way until it reaches $i_{L1}(t)$. During this stage the current $i_{LR1}(t)$ and the voltage $v_{CR1}(t)$ can be expressed as follows:

$$i_{L_{R1}}(t) = I_{in}\cos(\omega_1 t) \quad (19)$$

$$v_{C_{R1}}(t) = Z_1 I_{in}\sin(\omega_1 t) + V_o \quad (20)$$

The duration of this resonant stage is equal to

$$\Delta_{t_5} = \frac{\pi}{2\omega_1} \quad (21)$$

Stage 6. (t_5, t_6): This stage begins when the diode D_{A1} turns on. During this stage the auxiliary switch S_{A1} can be turned off under ZCS and ZVS. When $i_{LR1}(t)$ reaches zero again, the diode D_{A1} turns off. The current $i_{LR1}(t)$ and the voltage $v_{CR1}(t)$ can be expressed as follows:

$$i_{L_{R1}}(t) = \frac{-(V_{C5} - V_o)}{Z_1}\sin(\omega_1 t) \quad (22)$$

$$v_{C_{R1}}(t) = (V_{C5} - V_o)\cos(\omega_1 t) + V_o \quad (23)$$

where
$$V_{C5} = V_o + I_{in}Z_1 \quad (24)$$

The duration of this resonant stage is equal to

$$\Delta_{t_6} = \frac{\pi}{\omega_1} \quad (25)$$

Stage 7. (t_6, t_7): The active switches S_1 and S_{A1} are off, and the input current flows through the boost diode D_1 decreasing linearly .

Stage 8. (t_7, t_0): At t_7, when the input current $i_{L1}(t)$ reaches zero, the main switch S_1 is turned on under ZCS. The capacitor C_{R1} and the inductor L_{R1} form a half-cycle resonance through the main switch S_1 and the diode D_{A1}, which reverses the polarity of the voltage $v_{CR1}(t)$. When $i_{LR1}(t)$ reaches zero again, the diode D_{A1} turns off, beginning another switching cycle. During this stage the resonant inductor current $i_{LR1}(t)$ and the resonant capacitor voltage $v_{CR1}(t)$ can be expressed as follows:

$$i_{L_{R1}}(t) = \frac{-V_{C0}}{Z_1}\sin(\omega_1 t) \quad (26)$$

$$v_{C_{R1}}(t) = V_{C0}\cos(\omega_1 t) \quad (27)$$

The duration of this resonant stage is equal to

$$\Delta_{t_8} = \frac{\pi}{\omega_1} \quad (28)$$

Figure 6 shows the theoretical waveforms of the converter operation. In Fig. 7 are represented the state plane of the converter for the maximum and the minimum input current.

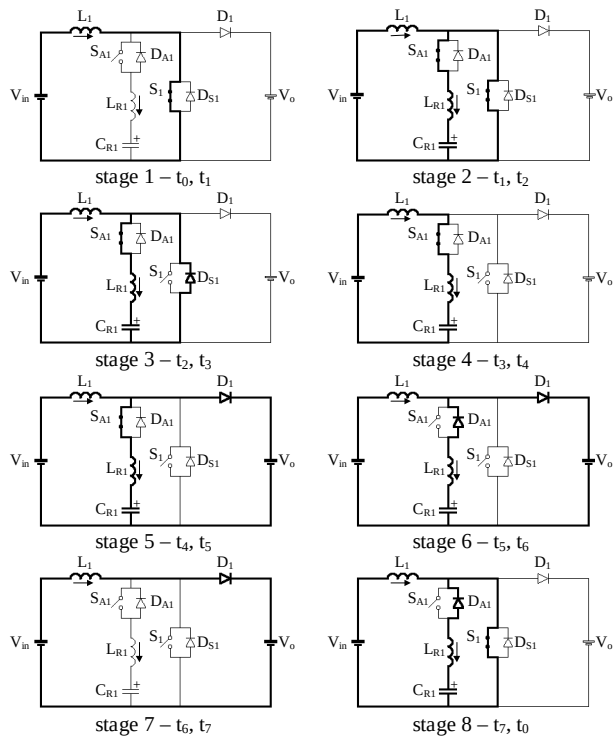

Fig. 5. Operation stages of one of the boost converters.

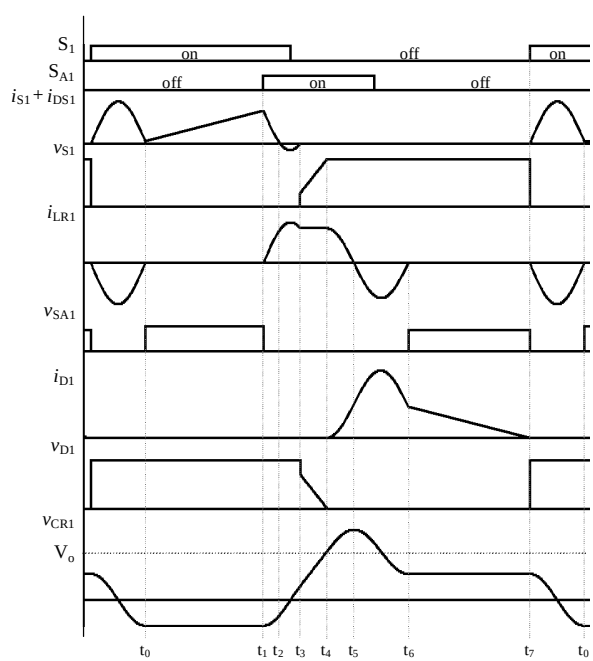

Fig. 6. Theoretical waveforms.

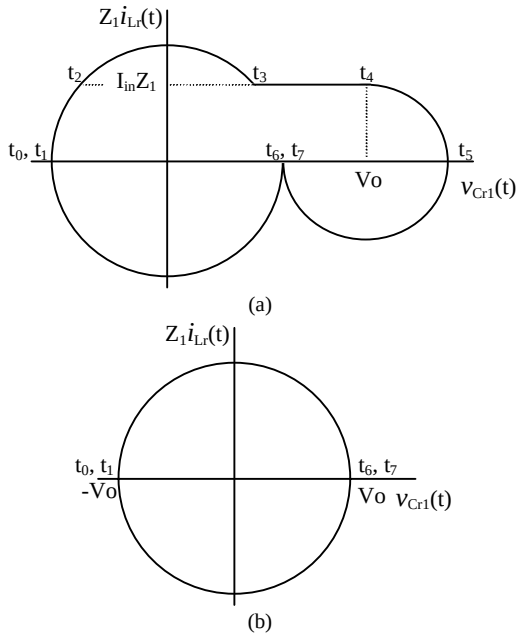

Fig. 7. State plane of one of the boost converters.
(a) for maximum input current;
(b) for minimum input current.

III. Design Guidelines and Example

In this section, it is presented a design procedure and an example to determine the component values of the proposed interleaved boost converters.

a) The input specifications consists of :

Output Power	P_o = 1200 W
Output Voltage	V_o = 300 V
Input Voltage	V_{in} = 120 Vrms
Input Frequency	f_{in} = 60 Hz
Minimum Switching Frequency	$f_{S\,min}$ = 40 kHz

b) Voltage ratio: from the input specifications it is possible to obtain the voltage ratio, which is given by:

$$a = \frac{V_p}{V_o} = \frac{120\sqrt{2}}{300} = 0.5657 \qquad (29)$$

c) Time of conduction of the main switch: from the input specifications and the equation (29):

$$t_{on} = \frac{1-a}{f_{S\,min}} = \frac{1-0.5657}{40000} = 10.8\,\mu s \qquad (30)$$

d) Maximum switching frequency:

$$f_{S\,max} \approx \frac{1}{t_{on}} = 93\,\text{kHz} \qquad (31)$$

e) The boost inductances L_1 and L_2:

$$L_1 = L_2 = \frac{V_p^{\,2} t_{on}}{2P_o} = 129.6\,\mu\text{H} \qquad (32)$$

f) Peak current in the boost inductances L_1 and L_2:

$$I_{pk} = \frac{V_p t_{on}}{L_1} = 14.14\,\text{A} \qquad (33)$$

g) Characteristic impedance of the auxiliary commutation circuit: to ensure the main switches turn-off under ZCS, the current peak in the auxiliary inductor during the stage 3 it should be larger than the maximum current in the boost inductor. Defining α as the parameterized value of the maximum input boost current, this α parameter should be larger than 1. Choosing $\alpha = 1.1$:

$$Z_1 = \frac{V_o}{I_{pk}(1+\alpha)} = 10.1\,\Omega \qquad (34)$$

h) The resonant inductances L_{R1} and L_{R2}: choosing C_{R1} and C_{R2} equal to 56 nF (commercial value) the resonant inductances value are obtained as follows:

$$L_{R1} = L_{R2} = Z_1^{\,2} C_{R1} = 5.7\,\mu H \qquad (35)$$

IV. Control Circuit Strategy

The block diagram of control circuit for the interleaved ZCS boost converters presented in this paper is shown in Fig. 8. Concerning Fig. 1, the boost cell formed by L_1, S_1, D_1 and its auxiliary commutation circuit is considered to be the master boost converter. The other boost cell is considered to be the slave boost converter. The operation of the master boost converter in C-DCM is as follows: the switch S_1 is turned on whenever the current value in the inductor L_1 reaches zero. The current value of L_1 is monitored using a LA 55-P current sensor, from LEM Inc. The current sensor signal is compared with zero and the output signal comparator is used as input for the circuit of generation of the gate signals, which was implemented using a Erasable Programmable Logic Device (EPLD) EPM7128SLC84-15 from Altera Corporation. The emergence of Application Specific Integrated Circuit - ASIC has drawn much attention due to its shorter design cycle, lower cost and higher density. The simplicity and programmability of the EPLD make it a good choice for prototyping digital systems.

Figure 9 shows the input and output signals of the control circuit represented in Fig. 8. The conduction time interval of the switches are constant and fixed. For the main switches this interval is defined as Δt_S and for the auxiliary switches this interval is defined as Δt_A. During the time interval Δt_C both switches S_1 and S_{A1} or S_2 and S_{A2} are on.

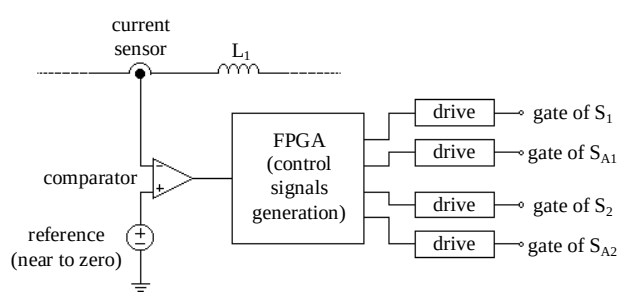

Fig. 8. Block diagram of control circuit.

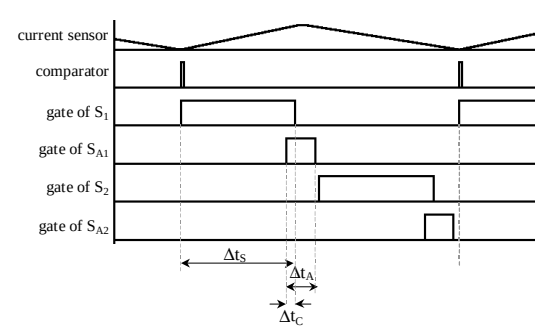

Fig. 9. Control circuit waveforms.

The delay time between main switches gate signals is defined as the half of the switching period. To determine this delay, it was used a similar procedure to that utilized in [4].

V. Experimental Results

To verify the operation and the performance of the interleaved ZCS boost converters presented in this paper, a prototype has been implemented. The power stage circuit is shown in Fig. 10 and the components and parameters used are summarized in Table 1. The active switches were implemented with a HGTP7N60C3D (600 V, 7 A) UFS (Ultra Fast Switches) series IGBTs from Harris Semiconductor, which present built-in an anti-parallel hyperfast diode. The boost diodes used were a hyperfast diode RHRP870 (700 V, 8 A) from Harris Semiconductor. The measured efficiency was 97.5%.

Figure 11 shows the experimental waveforms obtained for a close point to the peak of input voltage. As can be seen in Fig. 11.a, the main switches turn-on happens naturally in ZCS. Due to the presence of the auxiliary commutation circuit, the turn-off of the main switches occurs simultaneously in ZCS and ZVS. The maximum voltage on this device is equal to the output voltage of the converter. Figure 11.b shows that the auxiliary switch S_{A1} turns-on in ZCS and turns-off simultaneously in ZCS and ZVS. Figure 11.c shows that the boost diode D_1 turns-on in ZCS and ZVS and turns-off in ZCS. In Fig. 11.d are represented the current in the resonant inductor L_{R2} and the voltage in the resonant capacitor C_{R2}. In Fig. 11.e are represented the currents in the two main switches, S_1 and S_2. In Fig. 11.f are represented the currents in the two main inductors, L_1 and L_2. In this figure can be verified the delay of half operation period among the command of these devices. This delay is the responsible by minimization of the input current ripple.

TABLE 1
UTILIZED COMPONENTS AND PARAMETERS IN THE PROTOTYPE

Component	Parameter
V_{in} (input voltage)	120 Vrms
V_o (output voltage)	300 V
Input Frequency	60 Hz
L_1 and L_2	129 µH
L_{R1} and L_{R2}	5.3 µH
C_{R1} and C_{R2}	56 nF, polypropylene capacitors
C_f (output filter)	680 µF, eletrolythic capacitor
S_1-D_{S1} and S_2-D_{S2}	HGTP7N60C3D
S_{A1}-D_{A1} and S_{A2}-D_{A2}	HGTP7N60C3D
D_1 and D_2	RHRP870

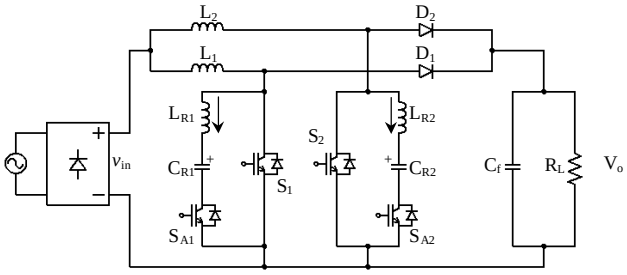

Fig. 10. Breadboarded interleaved ZCS boost converter.

In Fig. 12. are represented the input voltage and current. This figures shows that the waveform of the current is very similar to the one of the input voltage. The input current distortion is due to low resolution of the equipment used for the waveforms acquisition.

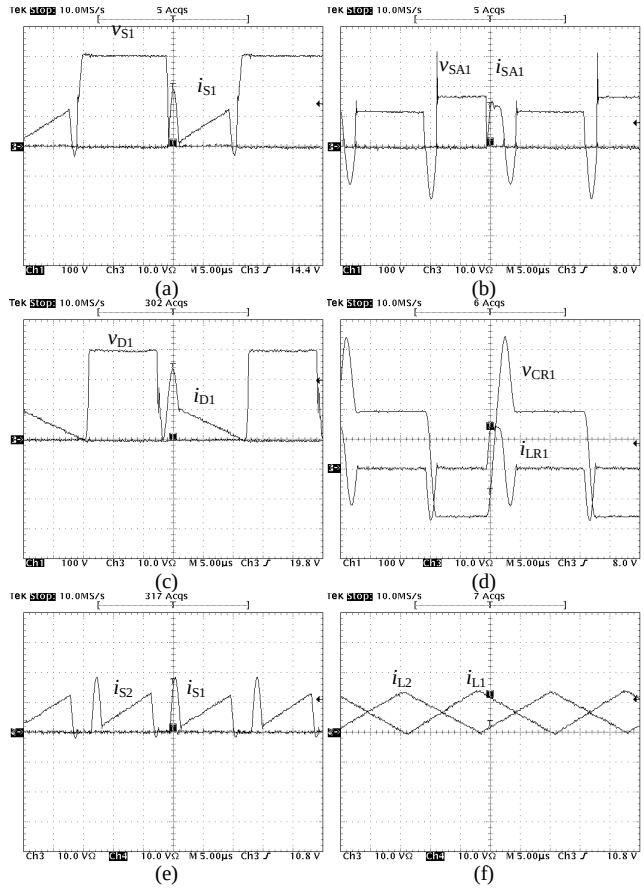

Fig. 11. Experimental waveforms.
(a) Main switch S_1; (b) Auxiliary switch S_{A1}; (c) Boost diode D_1; (d) Capacitor voltage $v_{CR1}(t)$ and inductor current $i_{LR1}(t)$; (e) Main switches currents; (f) Main inductors currents.
(scales: 100 V/div.; 10A/div.; 5µs/div.).

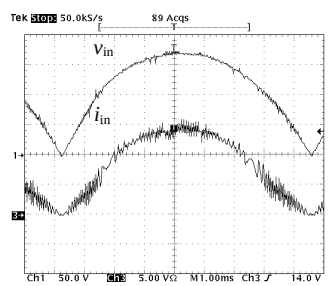

Fig. 12. Experimental waveforms of the input voltage and current.
(scales: 50 V/div.; 5A/div.; 1ms/div.).

VI. Conclusions

In this paper was investigated the use of a zero current switching (ZCS) soft commutation technique for application in boost converters, operating in critical conduction mode. The main switches turn-on occurs naturally in ZCS, due to the operation in C-DCM. In addition, the C-DCM also reduces the reverse recovery

losses of the boost diodes.

The use of the auxiliary commutation circuit providing ZCS at the turn-off of the main switches and an improvement of the efficiency is achieved. The experimental results was obtained using a 1.2 kW prototype operating from an AC input voltage source of 120 Vrms. The measured efficiency was 97.5%.

The auxiliary commutation circuit is placed out the power path and therefore, there is no voltage stresses on power semiconductor devices.

The minimization of the input current ripple is obtained by use of the interleaved boost converters.

The control circuit was implemented using a single EPLD EPM7128SLC84-15 from Altera Corporation. Owing to the highly integrated facility of the designed Control IC, the complexity can be greatly reduced.

VII. References

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