A NEW HPF-ZCS-PWM BOOST RECTIFIER

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Abstract: **This paper presents a new high-power-factor (HPF) pulse-width modulated (PWM) Boost rectifier, based on a novel soft-commutation cell, featuring zero-current-switching (ZCS) of the active switches. Two active switches (main and auxiliary transistors), two diodes, two small resonant inductors and one resonant capacitor compose this commutation cell, recommended to operate with insulated-gate bipolar transistors (IGBTs) as the power switches.**

This new ZCS-PWM commutation cell provides a zero-current (ZC) turn-on and a zero-current-zero-voltage (ZCZV) turn-off to the transistors, besides a zero-voltage (ZV) turn-on to the diodes.

Based on this new commutation cell, a new family of ZCS-PWM dc-to-dc converters is generated, offering conditions to obtain isolated converters, as example: derived Buck-Boost, Sepic and Zeta converters.

The new HPF-ZCS-PWM Boost rectifier is presented, and its input current shaping is achieved using the average current mode control, obtaining a structure with high efficiency at wide load range, reduced total harmonic distortion (THD) and, consequently, power factor (PF) near the unity.

Also, it is presented the principle of operation, the theoretical analysis and a design procedure for the new HPF-ZCS-PWM Boost rectifier, as well as a design example and experimental results from a test unit rated at 1.6kW, 400V output voltage, 220V_{rms} input voltage, and 20kHz switching frequency. The measured efficiency and power-factor were 96.4% and 0.999 respectively, with an input current total harmonic distortion (THD) equal to 3.42% for an input voltage with THD equal to 1.61%, at rated load.

I - INTRODUCTION

At the moment, the switching-mode power supplies are one of the most important loads connected to the ac system. These power supplies are based on dc-to-dc converters, which control the power transferred from the input source to the load. Reduced volume, high efficiency and high power factor are some of the basic demands that the switching-mode power supplies must attend, especially when harmonic standards, such as IEC 1000-3-2, must be satisfied.

It is possible to reduce the size of the capacitive and magnetic components increasing the switching frequency of the converter, reducing consequently the total size and volume of the structure. However, this process increases the total switching losses at the semiconductors devices, causing a significant reduction in the structure's efficiency. Moreover, high switching frequencies propitiate an increase in the electromagnetic interference (EMI) emission.

Due to the development of the soft-commutation techniques, which limit the switching losses, the efficiency of the converters has been improved, providing conditions to increase the switching frequency and reduce the EMI.

In compliance with this context, zero-voltage-switching (ZVS) and zero-voltage-transition (ZVT) techniques have been proposed in several papers [1 - 5]. However, the choice of the soft-commutation technique to be used must take into account the static and dynamic characteristics of the semiconductor devices used as power switches.

The ZVS and ZVT techniques are naturally recommended for metal-oxide-semiconductor field-effect transistors (MOSFETs). However, in high power applications (above 1kW), insulated-gate bipolar transistors (IGBTs) are preferred as power switches, because they present lower conduction losses than MOSFETs. On the other hand, the turn-off losses compose the major part of the total switching losses in IGBTs. This fact makes the zero-current-switching (ZCS) or the zero-current-transition (ZCT) technique the most effective one for IGBTs [6 - 8].

In addition to the reduced volume and the high efficiency, the switching-mode power supplies must also present high power-factor. Most of the switching-mode power supplies drain non-sinusoidal currents from the ac system and, consequently, the power-factor of these structures are generally very low. This problem can be avoided using an appropriated control mode for the active switches, featuring a sinusoidal shape at the input current waveform.

Based on these facts, this paper presents a new ZCS-PWM commutation cell, derived from the commutation cell analyzed in [8]. This new ZCS-PWM commutation cell provides a zero-current (ZC) turn-on and a zero-current-zero-voltage (ZCZV) turn-off to the active switches, besides a zero-voltage (ZV) turn-on to the diodes.

A new family of ZCS-PWM converters is generated based on this new commutation cell, offering conditions to obtain isolated converters, as example: derived Buck-Boost, Sepic and Zeta converters.

The new HPF-ZCS-PWM Boost rectifier, using average-current mode control to achieve high input power-factor, is taken as example to explain the operation of the proposed commutation cell, obtaining a structure with high efficiency at wide load range and power factor near the unity.

The principle of operation, the theoretical analysis, a design procedure and experimental results from a test unit of the new Boost rectifier, rated at 1.6kW, 400V output voltage, 220V_{rms} input voltage, and operating at 20kHz, are also presented.

II – THE NEW FAMILY OF ZCS-PWM CONVERTERS

Figure 1 shows the new ZCS-PWM soft-commutation cell proposed.

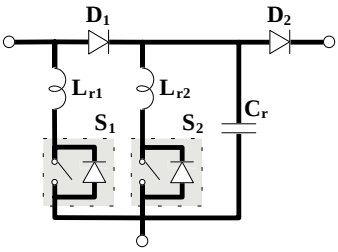


Fig. 1 - The new ZCS-PWM commutation cell.

According to figure 1, two transistors (S_1, main switch, and S_2, auxiliary switch), two diodes (D_1 and D_2), one resonant capacitor (C_r) and two small resonant inductors (L_{r_1} and L_{r_2}) compose this commutation-cell

The main switch is the major responsible for the power transferred to the load. The function of the auxiliary switch is to provide conditions for soft-commutation under constant frequency at the main switch.

Figure 2 shows the new family of dc-to-dc converters, based on the new ZCS-PWM commutation cell.

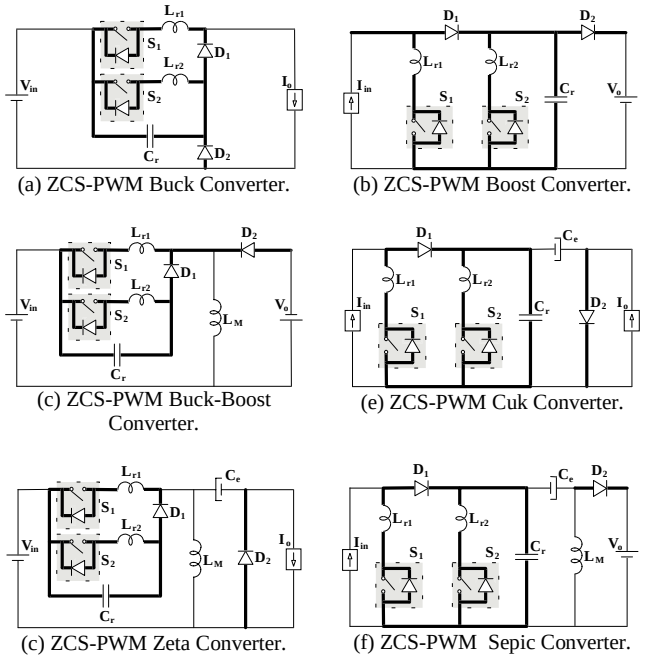


Fig. 2 – A new family of dc-to-dc converters, generated from the new ZCS-PWM commutation cell.

According to figure 2, the Buck-Boost, Sepic and Zeta structures can be naturally isolated through their accumulation inductors (L_m). This fact is not possible with the ZCS-PWM commutation cell proposed in [8].

III – A NEW HPF-ZCS-PWM BOOST RECTIFIER AND ITS PRINCIPLE OF OPERATION

Figure 3 shows the new HPF-ZCS-PWM Boost rectifier proposed.

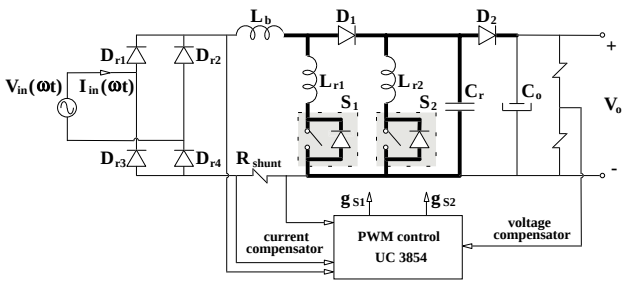


Fig. 3 – The new HPF-ZCS-PWM Boost rectifier.

In order to simplify the analysis, some conditions will be assumed, as follows:

- all components are ideal;
- the switching frequency (f_s) of the switches is much higher than the ac system frequency (f_{line}), which allows us to consider the input voltage practically constant, during one switching period (T_s);
- according to the last condition, one can admit that the converter is supplied by a constant current-source equal to the absolute value of the input current ($|I_{in}(\omega T_i)|$), during a generic switching period ($T_i = T_s$);
- the output voltage (V_o) of the rectifier is constant.

In compliance with the simplifying conditions, figure 4.a shows the nine topological stages for the new HPF-ZCS-PWM Boost rectifier and figure 4.b shows the main theoretical waveforms, for the simplified HPF-ZCS-PWM Boost rectifier, during a generic switching period.

The topological stages of this structure are described as follows:

Stage 1: In the beginning of this stage, the currents through L_{r_1} (i_{Lr1}) and L_{r_2} (i_{Lr2}) are nulls, the voltage across C_r (v_{Cr}) is equal to the output voltage (V_o) and the input current ($|I_{in}(\omega T_i)|$) flows through D_1 and D_2. This stage starts when S_1 is turned on, at $\omega t = \omega t_0$, in zero-current (ZCS) due to the presence of L_{r_1}. The current i_{Lr1} evolves linearly, starting from zero, until it reaches the value $|I_{in}(\omega T_i)|$, at $\omega t = \omega t_1$. At this moment, D_1 and D_2 turn off because the currents through them become nulls. Thus, the second stage starts.

Stage 2: The input current $|I_{in}(\omega T_i)|$ remains constant and flowing through S_1 and the final conditions of the first stage are sustained during this stage. The end of this stage happens when S_2 is turned on, at $\omega t = \omega t_2$. The control of this time interval allows us to control the power transferred to the load.

Stage 3: The turn-on of S_2, in the beginning of this stage, occurs in zero-current (ZCS) due to the presence of L_{r_2}. Now, the resonance between L_{r_2} and C_r occurs. D_1 and D_2 remain turned off and the input current $|I_{in}(\omega T_i)|$ stays flowing through S_1. This stage finishes when v_{Cr} reaches zero, at $\omega t = \omega t_3$.

Stage 4: The beginning of this stage happens when the diode D_1 turns on in zero-voltage (ZVS), due to the annulment of v_{Cr} at $\omega t = \omega t_3$. In this way, the resonance occurs among L_{r_1}, L_{r_2} and C_r. The end of this stage occurs at $\omega t = \omega t_4$, when i_{Lr1} becomes null.

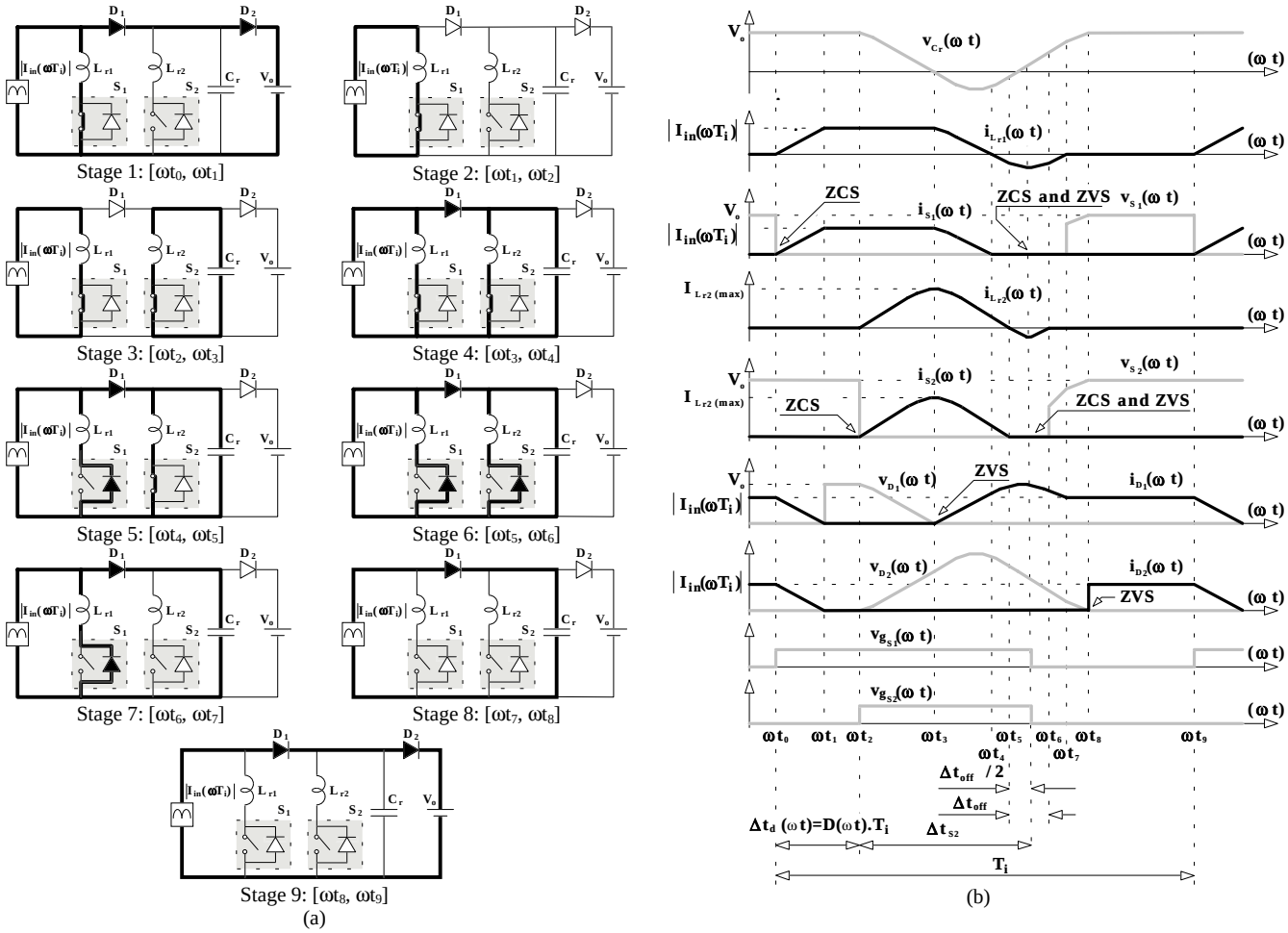


Fig. 4 – (a) Topological stages for the new simplified HPF-ZCS-PWM Boost rectifier,
(b) Theoretical waveforms, for the simplified HPF-ZCS-PWM Boost rectifier; during a generic switching period (T_i).

Stage 5: This stage starts when the current i_{Lr1} flows through the anti-parallel diode of S_1. Therefore, the current and the voltage across S_1 are nulls during this stage. The current i_{Lr2} stays flowing through S_2, in a resonant way. At $\omega t = \omega t_5$, i_{Lr2} reaches zero and the sixth stage begins.

Stage 6: The anti-parallel diode of S_2 starts to conduct due to the inversion of i_{Lr2}. Thus, during this stage, S_1 and S_2 are turned off, simultaneously, in zero-current and zero-voltage (ZCZVS). This stage finishes at $\omega t = \omega t_6$, when i_{Lr2} returns to zero, and the anti-parallel diode of S_2 turns off.

Stage 7: During this stage, i_{Lr1} stays evolving in a resonant way until it becomes null, at $\omega t = \omega t_7$. At this moment, the anti-parallel diode of S_1 turns off, finishing the resonance and starting the eighth stage.

Stage 8: In this stage, C_r is charged linearly by the input current $|I_{in}(\omega T_i)|$. At $\omega t = \omega t_8$, v_{Cr} reaches V_o and the diode D_2 turns on in zero-voltage (ZVS), starting the ninth stage.

Stage 9: The major part of the power is transferred to the load in this stage. Here, only D_1 and D_2 are on, and the energy flows directly to the load. This stage finishes at $\omega t = \omega t_9$, when S_1 is turned on in zero-current (ZCS), starting a new operation period.

Based on the analysis of the topological stages, it can be seen that the switching losses are eliminated. In this way, the operation of the converter in high frequency will be possible, which allows a structure reduction (volume and size) and a consequent increase in the power density.

IV – Conditions to Obtain Zero-Current-Switching

In order to obtain zero-current-switching, the following constraints must be assisted for the stages happen as described before:

$$\beta = \frac{L_{r2}}{L_{r1}} < 1 \qquad (1)$$

and,

$$\alpha_{max} < \beta \qquad (2)$$

where:

$$\alpha(\omega t) = \frac{|I_{in}(\omega t)|}{V_o} \cdot \sqrt{\frac{L_{r2}}{C_r}} \qquad (3)$$

$$\alpha_{max} = \frac{I_{pk}}{V_o} \cdot \sqrt{\frac{L_{r2}}{C_r}} \qquad (4)$$

$$I_{pk} = \frac{\sqrt{2}.P_o}{\eta\%.V_{in(rms)_{min}}}.100 \qquad (5)$$

I_{pk} = peak value of input current;
P_o = nominal value of output power;
$\eta\%$ = minimum value of efficiency adopted, in percentage;
$V_{in(rms)_{min}}$ = minimum rms value of input voltage.

The time interval available to turn off the switches simultaneously is given by (6).

$$\Delta t_{off} = \Delta t_6 = \frac{2}{\omega_{01}} \cdot \left[\frac{\pi - a\cos(-\beta)}{\sqrt{1+\beta}} \right] \qquad (6)$$

where:

$$\omega_{01} = \frac{1}{\sqrt{L_{r2} \cdot C_r}} \qquad (7)$$

Thus, the time interval used to control S_2 is obtained using (8), as follows:

$$\Delta t_{S2} = \frac{1}{\omega_{01}} \cdot \left[\frac{4.\pi - (\sqrt{1+\beta}).\pi - 2.a\cos(-\beta)}{2.\sqrt{1+\beta}} \right] - \frac{\Delta t_{off}}{2} \qquad (8)$$

So,

$$\Delta t_{S2} = \frac{1}{\omega_{01}} \cdot \left[\frac{\pi}{2} + \frac{\pi}{\sqrt{1+\beta}} \right] \qquad (9)$$

It should be noted, based on (9), that the time interval used to control S_2 just depends on the resonant parameters used. It means that this time interval is constant during the ac system period, and over load variation.

V – THE THEORETICAL OUTPUT CHARACTERISTICS

The voltage conversion ratio (q) of the new Boost rectifier is given by (10).

$$q(\alpha_{rms}, \beta, f_s / f_{01}, D_{rms}) = \frac{V_o}{V_{in(rms)}} \qquad (10)$$

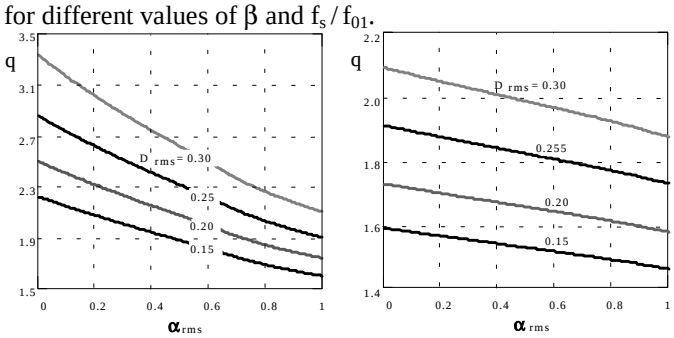
where:

$$\alpha_{rms} = \frac{I_{rms}}{V_o} \cdot \sqrt{\frac{L_{r2}}{C_r}} \qquad (11)$$

$$f_{01} = \frac{\omega_{01}}{2.\pi} \qquad (12)$$

and, D_{rms} = effective duty cycle of control.

From the analysis, figure 5 shows the voltage conversion ratio for the new Boost rectifier, obtained as a function of α, for different values of β and f_s / f_{01}.



(c) $\beta = 0.4$, $f_s / f_{01} = 0.40$ (d) $\beta = 0.8$, $f_s / f_{01} = 0.25$

Fig. 5 – Theoretical output characteristics for the new HPF-ZCS-PWM Boost rectifier.

VI – DESIGN PROCEDURE AND EXAMPLE

Following, the design procedure of the new HPF-ZCS-PWM Boost rectifier is presented, employing as an example the input and output data listed bellow:

$V_{in(rms)}$ = 220V ± 15%, V_o = 400V, P_o = 1.6kW,
f_{line} = 60Hz, f_s = 20kHz and η% = 95%.

The peak value of the input current is obtained using (5). This value will be used in (4) to obtain the resonant parameters.

Values for the parameters α_{max} and β are adopted in order to assist the constraints of operation. Also it is necessary to adopt a value for the relation f_s/f_{01}.

Taking the following parameters:

$$\beta = 0.8 \text{ , } \alpha_{max} = 0.7 \text{ and } \frac{f_s}{f_{01}} = 0.25 \text{ ,}$$

the resonant inductors and the resonant capacitor can be obtained using (1), (4), (7) and (12), as follows:

L_{r1} = 56.78μH , L_{r2} = 43.45μH and C_r = 94nF.

The Boost input inductor (L_b) is specified assuming that the ripple of the input current must not exceed 15% of its peak value. The output capacitor (C_o) is obtained for a maximum accepted output voltage ripple of 2% of its nominal value. Thus:

L_b = 2.4mH and C_o = 680μF.

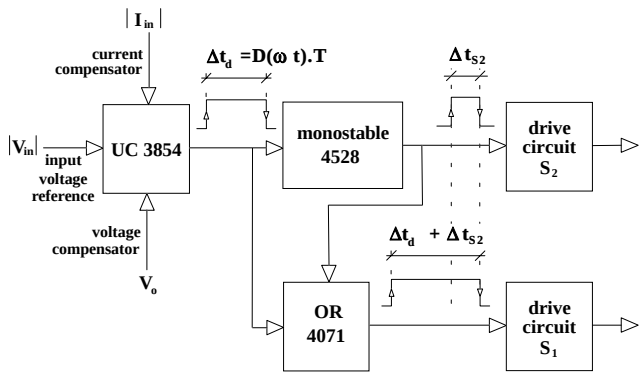
The time interval used to control the auxiliary switch is given by (10). So:

$$\Delta t_{S2} = 7.95\mu s \text{ .}$$

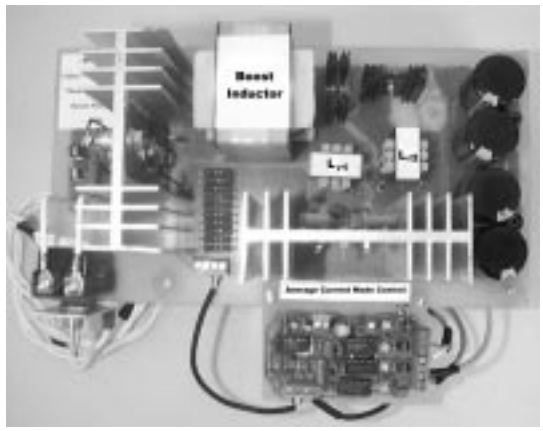
The proposed structure is controlled using the UC3854, especially designed for average-current mode control technique. Its external parameters are obtained following the recommendations presented in [9].

VI – EXPERIMENTAL RESULTS

Figure 6.a shows the blocks diagram of the control logic circuit implemented, in order to obtain the signals used to control the main and auxiliary switches, and figure 6.b shows a photograph of the test unit implemented.



(a)



(b)

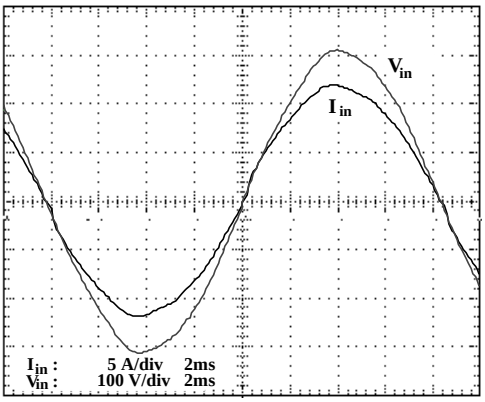
Fig. 6 – (a) The control logic diagram, and (b) Test unit of the new HPF-ZCS-PWM Boost rectifier.

The experimental input current of the rectifier is shown in figure 7.a, at the nominal input voltage and full load. Figures 7.b and 7.c show the frequency spectrums of the input current and the input voltage, respectively, from the results presented in figure 7.a.

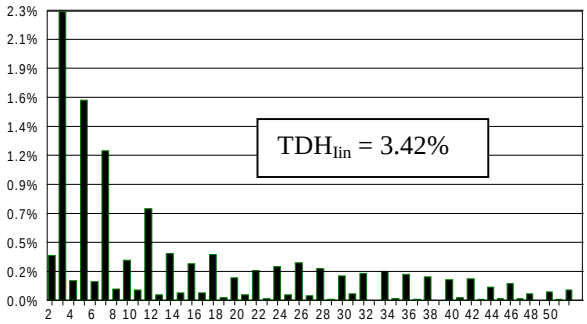
From figure 7.a, one can verify that the phase displacement between input current and input voltage is practically null.

Based on figure 7.b, it can be seen that the harmonic distortion of the input current is quite small. The total harmonic distortion of the input current, for nominal load, is 3.42%, for a total harmonic distortion in the input voltage equal to 1.61%.

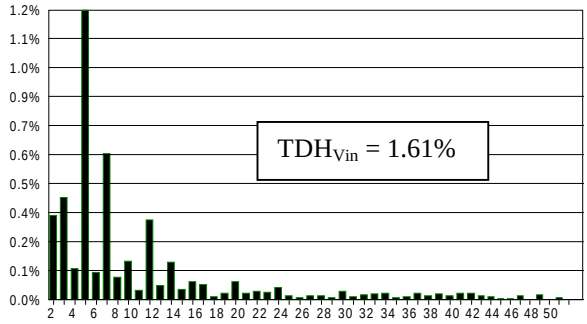
In this way, the measured power-factor of the structure is 0.999, for nominal load.



(a)



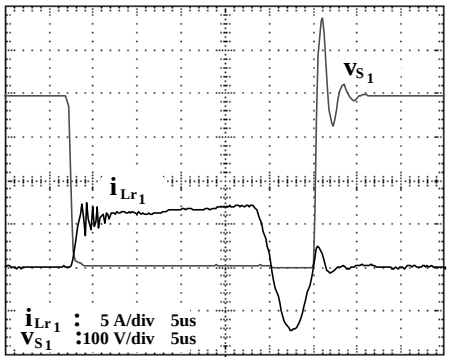
(b)



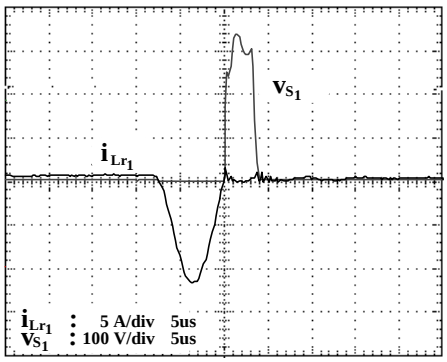
(c)

Fig. 7 – (a) Input voltage (V_{in}) and current (I_{in}), (b) frequency spectrum of input current, (c) frequency spectrum of input voltage; at full load.

Figure 8 shows the commutation details for the main and auxiliary switches (S_1 and S_2). These results were obtained near $V_{in}(\omega t) = 0$ and also near $V_{in}(\omega t) = V_{pk}$, where: $V_{in}(\omega t)$ is the instantaneous value of input voltage, and V_{pk} is the peak value of input voltage.



(a)



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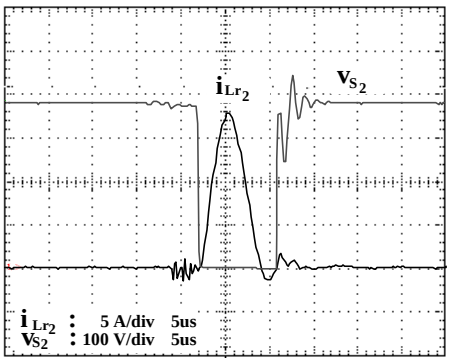
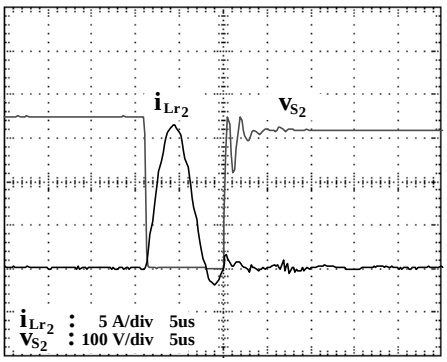


(c)



(d)

Fig. 8 – Commutation details for the main switch: (a) near $V_{in}(\omega t) = V_{pk}$, (b) near $V_{in}(\omega t) = 0$, and commutation details for the auxiliary switch: (c) near $V_{in}(\omega t) = V_{pk}$, (d) near $V_{in}(\omega t) = 0$; at full load.

According to the results showed in figure 8, it can be seen that the main (S_1) and the auxiliary (S_2) switches perform ZC commutations in their turn-on processes and ZCZV commutations in their turn-off processes. In this way, the soft-commutations performed are preserved during the ac system period.

The commutation details for the Boost diode (D_2) are shown in figure 9.

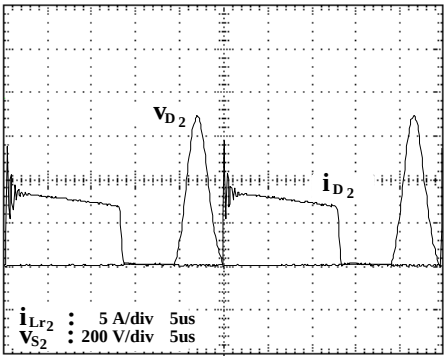


Fig. 9 – Commutation details for D_2.

In the conventional ZCS technique, the Boost diode has to sustain voltage twice the output voltage (in this case, > 800V). However, in this new ZCS operation proposed, the maximum value of the blocking voltage stress on diode D_2 is determined by parameters α and β. In this design example, it is near 700V, as shown in figure 9. On the other hand, the voltage stresses indirectly increases the conduction losses in several high voltage ultra fast diodes, which present high forward voltages. So, for better performance in practical applications we suggest the device BYP100-Siemens (1000V, low forward voltage – $V_{F(typ)}$ = 1.75V (100°C) and 55ns ultra fast soft recovery) as diode D_2.

The measured efficiency of the new HPF-ZCS-PWM Boost rectifier proposed, as a function of the output power, is shown in figure 10, in comparison to the efficiency of the conventional hard-switching HPF-PWM Boost rectifier, both operating at $220V_{rms}$ nominal input voltage, and at the same data specifications.

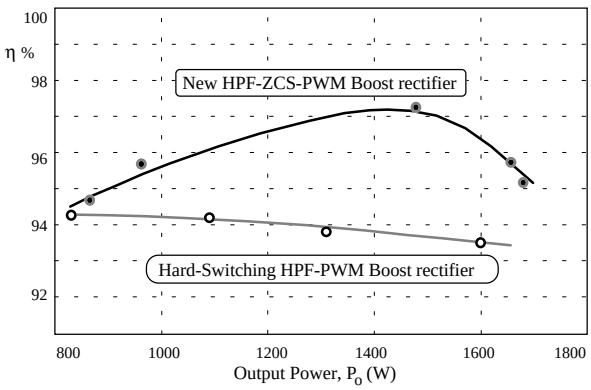


Fig. 10 – Experimental efficiency for the new HPF-ZCS-PWM Boost rectifier and for the hard-switching HPF-PWM Boost rectifier.

For the conventional PWM Boost rectifier, the major power dissipation comes from the switching losses (about 52W). On the other hand, for the new HPF-ZCS-PWM Boost rectifier, the additional power losses involved in the auxiliary components are only about 12W, which is less than 0.8% of the nominal output power.

The measured efficiency from the new HPF-ZCS-PWM Boost rectifier is equal to 96.4% and, from the conventional hard-switching HPF-PWM Boost rectifier, it is equal to 93.5%, at rated load.

Finally, the commutation energy for this ZCS-PWM cell proposed should be designed to attend the worst operating point (nominal load and low rms input voltage), and it keeps constant in this converter since V_o (output voltage) is considered regulated. So, the efficiency for light load will not be high in this case. However, this drawback is present in almost all ZCS cells proposed in the literature, and the efficiency at full load is usually more a concern than at light load.

VIII. Conclusions

This paper presented a new HPF-ZCS-PWM Boost rectifier. The new rectifier proposed presents an input current with low total harmonic distortion and reduced phase displacement in relation to the input voltage. Thus, this structure presents a power-factor near the unity, and it is in agreement with IEC 1000-3-2 standards, emulating a practically resistive load.

The commutations of the main and the auxiliary switches occurred in zero-current (ZCS) in their turn-on processes, and in zero-current-zero-voltage (ZCZVS) in their turn-off processes, as expected, providing conditions to obtain high efficiency and a reduced EMI emission.

Therefore, this new ZCS-PWM technique significantly improves the circuit's efficiency, providing a great reduction in the size of the heat sinks used, and it is suitable for IGBTs applications.

Acknowledgments

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