A Novel Non-Isolated Single Phase UPS based on Boost Converters

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***Abstract* – This paper presents a single phase non-isolated uninterruptible power supply topology that overcomes some drawbacks of the previous reported ones. Among the desired features of the proposed UPS topology are: small number of semiconductors, low battery voltage, flexibility for the selection of the input and output voltages, common neutral between the incoming ac line and the load. The proposed UPS is composed of three bi-directional boost converters, where both the incoming ac line and the load are connected in differential mode across the output terminals of these boost converters. A current limiter is introduced to improve robustness and reliability of the proposed UPS. In this paper, analysis and experimental results for both the line operating mode and backup mode are presented. In addition, the current limiter operation is experimentally verified under several load transient conditions.**

I. Introduction

Uninterruptible power supplies have been used in a wide variety of application to protect critical loads against disturbances (sags, swells, outages) coming from the utility supplied voltage. Among the UPS, single phase non-isolated UPS have been deployed to protect loads of a fraction to few kW, due their reduced size and small cost compared with the isolated counterparts. Usually, single phase non-isolated UPS are required to operate with unity input power factor, for two reasons. First, to take advantage of the current supplying capabilities of the available single phase line. Second, to satisfy the limits imposed by the regulatory agencies on the current harmonics drawn by equipment connected to the utility grid. On the other hand, it is desired to operate with low battery storage voltage since the cost increases and the reliability decreases with the number of batteries connected in series.

Many non isolated single phase topologies have been reported in the literature [1-5]. The majored of them are based on PWM rectifier and inverters either in half-bridge configuration [2,4] or in full-bridge configuration [1,5]. Regarding the number of components count, the UPS based on half-bridge rectifiers and inverters are more attractive then the full-bridge ones. On the other hand, high battery voltage is required in both the full-bridge and half-bridge based topologies. The battery voltage must be larger than the peak value of the incoming ac line voltage in the full bridge based topologies [1,5], and it reaches twice this value in the half-bridge counterparts, which is not acceptable in the majority of applications. Aiming to mitigate the high battery voltage of the half bridge based topologies, a bi-directional chopper can be introduced between the battery and the dc bus [2]. However, half bridge configurations usually suffer from unbalance in the voltage across the dc bus capacitors [2]. This unbalance becomes critical during the start-up of loads with transformers or diode rectifiers followed by large electrolytic capacitors. The dc bus unbalance is addressed in [4], which mitigate it at the price of adding a larger number of diodes and switches.

This paper presents a UPS topology that does not suffer from the unbalance in the dc link capacitors and does provide flexibility for the selection of the battery, the input and the output voltages, with a reduced number of switches. The proposed UPS topology is shown in Fig. 1. It is comprised of a boost rectifier and a boost inverter [6,10,11]. The input boost rectifier and output boost inverter have a common leg, which reduces the number of components count. In addition, the neutral conductor is common between the incoming ac line and the load. As a result, this eliminates the requirement of an isolation transformer.

This paper is organised as follows: In Section II a description of the proposed UPS in both the line operating mode and backup mode are presented. In Section III, the proposed UPS is analyzed. In Section IV the UPS controller is described and a current limiter is introduced. Experimental results are presented in Section V and in Section VI, conclusions based on the results obtained are drawn.

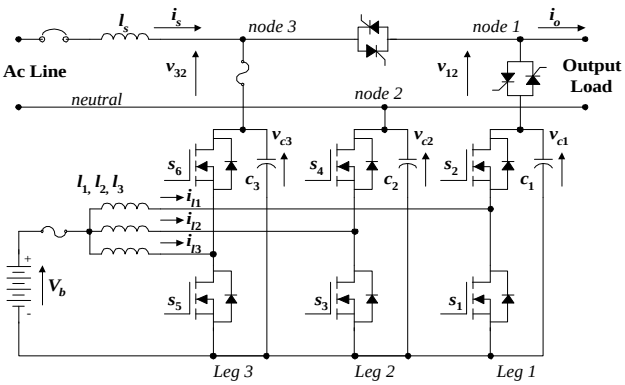

Fig. 1 Power circuit diagram of the proposed UPS.

II. Principle of Operation

In this Section the principle of operation of the proposed UPS is described. Two modes of operation, which depend on the status of the incoming ac line, are considered. The first is called line operating mode, and it occurs when the incoming ac line is within the acceptable input voltage range. The second is called backup mode, it occurs when the incoming ac line fails.

A. Line Operating Mode

During the line operating mode power is transferred

from the incoming ac line to the battery and output load. Both boost rectifier (legs 3 and 2) and inverter (legs 1 and 2) are active. All legs are operated in continuous conduction mode of the currents i_{l1}, i_{l2} and i_{l3} and their output voltages v_{c1}, v_{c2} and v_{c3} are controlled so that they have a dc component and a fundamental ac component at the line frequency. The dc components must have equal magnitude. In this way there is no dc components in the differential voltages across the load, $v_{12,}$ and line v_{32}. In addition, the amplitude of the dc component must be selected to ensure that the voltages v_{c1}, v_{c2} and v_{c3} are always greater than the battery voltage, V_b. This constrain is required to allow the proper operation of the boost converters. It is suggested in this paper to keep the amplitude of the fundamental component of the voltage v_{c2} at a constant value, since the leg 2 is common to the input boost rectifier and to the output boost inverter. On the other hand, the voltages v_{c1}, v_{c3} are shaped to provide the required output voltage and input current respectively.

B. Backup Mode

During the backup mode the output boost inverter transfers power from the battery to the output. Regarding the operation of the input rectifier, the leg 3 can be either inactive or it can controlled to ensure that the line current i_s is equal to zero.

In the next section, a detailed analysis of the UPS in both the line operating mode and the backup mode is presented.

III. CIRCUIT ANALYSIS

In order to simplify the analysis the following assumptions are made:

(i) All components are considered ideal, without losses;

(ii) The switches of the bi-directional boost converters are controlled in a complementary way. As a result, the boost converters operate in continuous conduction mode of currents i_{l1}, i_{l2}, i_{l3};

(iii) The variables in the circuit are averaged over one switching period, therefore the high frequency ripples are neglected;

(iv) The voltage across inductors l_1, l_2, l_3, l_s and the current through the capacitors c_1, c_2 e c_3 are neglected.

Under the above assumptions the incoming ac line voltage can be defined as:

$$v_{32}(t) = V_s\sqrt{2}\cdot\sin(\omega t) \tag{1}$$

where V_s is the rms value to the incoming ac line voltage.

Similarly, the output ac voltage is defined by:

$$v_{12}(t) = V_o\sqrt{2}\cdot\sin(\omega t) \tag{2}$$

where V_o is the rms value to the output ac voltage.

The relationships between voltages at the input and output of the UPS, Fig. 1, can be found from the Kirchhoff's voltage law, that is:

$$v_{32}(t) = \bar{v}_{c3}(t) - \bar{v}_{c2}(t) \tag{3}$$

$$v_{12}(t) = \bar{v}_{c1}(t) - \bar{v}_{c2}(t) \tag{4}$$

The bar indicates that the associated quantity is an average value over one switching period.

By following the description of Section II, the voltages $\bar{v}_{c1}, \bar{v}_{c2}$ and $\bar{v}_{c3}$ at the output of the boost converters can be expressed as:

$$\bar{v}_{c1}(t) = V_{dc} + V_{c1_1}\sin(\omega t) \tag{5}$$

$$\bar{v}_{c2}(t) = V_{dc} + V_{c2_1}\sin(\omega t + \pi) \tag{6}$$

$$\bar{v}_{c3}(t) = V_{dc} + V_{c3_1}\sin(\omega t) \tag{7}$$

where V_{dc} is the dc bias voltage and V_{c1_1}, V_{c2_1} and V_{c3_1} are the amplitude of the fundamental components of the voltages v_{c1}, v_{c2} and v_{c3} . The angular position of the output voltage is defined as ωt. Where the frequency ω is assumed to be the same as the one of the incoming ac line.

The dc bias voltage can be computed as a function of the input voltage V_s, the output voltage V_o, the battery voltage V_b and the minimal duty cycle D_{min} , as:

$$V_{dc} = \frac{V_o\sqrt{2}}{2} + \frac{V_b}{1-D_{\min}} \qquad \text{if } V_o > V_s \tag{8}$$

$$V_{dc} = V_s\sqrt{2} - \frac{V_o\sqrt{2}}{2} + \frac{V_b}{1-D_{\min}} \qquad \text{if } V_o < V_s \tag{9}$$

Furthermore, by considering the operation of the boots converter the instantaneous average output voltage of each boost leg, can be also expressed as:

$$\frac{\bar{v}_{c1}}{V_b} = \frac{1}{1-\bar{d}_1}\ , \quad \frac{\bar{v}_{c2}}{V_b} = \frac{1}{1-\bar{d}_2}\ , \quad \frac{\bar{v}_{c3}}{V_b} = \frac{1}{1-\bar{d}_3} \tag{10-12}$$

where $\bar{d}_1, \bar{d}_2$ and $\bar{d}_3$ are the instantaneous average duty cycle of the boost legs 1, 2 and 3 respectively .

Finally, to obtain the instantaneous average inductor currents $\bar{i}_{l1}$, $\bar{i}_{l2}$, $\bar{i}_{l3}$ and the average battery current $\bar{i}_b$, is necessary to apply the Kirchhoff's current law to the nodes 1, 2 and 3 (Fig. 1). By using the equation that govern the operation of the boost converter in continuous conduction mode, it is possible to find that:

$$\bar{i}_{l1}(t) = \frac{\bar{i}_o}{1-\bar{d}_1}\ , \quad \bar{i}_{l2}(t) = \frac{\bar{i}_s - \bar{i}_o}{1-\bar{d}_2}\ , \quad \bar{i}_{l3}(t) = \frac{-\bar{i}_s}{1-\bar{d}_3} \tag{13-15}$$

$$\bar{i}_b = \bar{i}_{l1} + \bar{i}_{l2} + \bar{i}_{l3}\,. \tag{16}$$

The above equations can be used to obtain the main quantities (currents, voltages and duty cycle) at different operating conditions. As an example, let us consider a UPS with the parameters of Table I. With these it is possible to compute v_{c1}, v_{c2} and v_{c3} using (5) to (7). Then, the duty cycles can be found using (10) to (12). Finally, the currents i_{l1}, i_{l2} and i_{l3} are obtained from (13) to (15). Figures 2 to 6 illustrate the results of this procedure.

TABLE I

UPS PARAMETERS	
Nominal Input voltage V_s	110V
Output voltage V_o	120V
Nominal Battery voltage V_b	48V
Line frequency ω	377 rad/s
Output power P_o	170W
Battery charge power P_b	30W

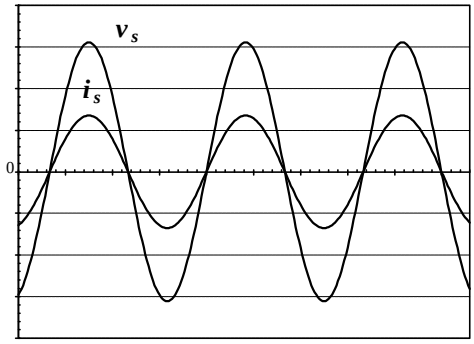

Fig. 2 UPS input voltage and current during the line operating mode Vertical scales: 50V/div. and 2A/div. Horizontal scale 5ms/div.

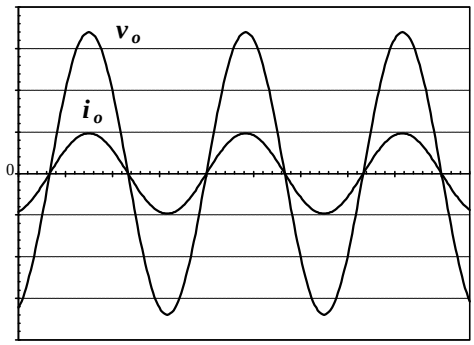

Fig. 3 UPS output voltage and current during the line operating mode. Vertical scales: 50V/div. and 2A/div. Horizontal scale 5ms/div.

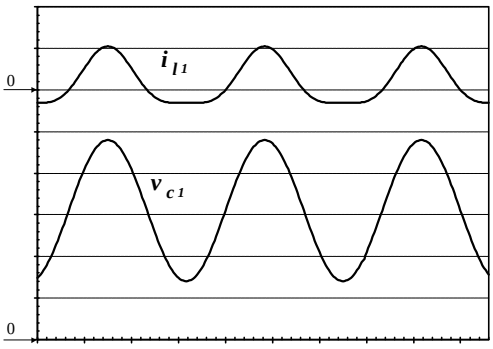

Fig. 4 Boost input current i_{l1} and output voltage v_{c1} during the line operating mode. Vertical scales: 50V/div. and 10A/div. Horizontal scale 5ms/div.

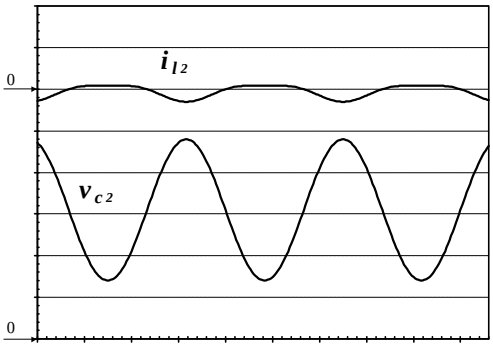

Fig. 5 Boost input current i_{l2} and output voltage v_{c2} during the line operating mode. Vertical scales: 50V/div. and 10A/div. Horizontal scale 5ms/div.

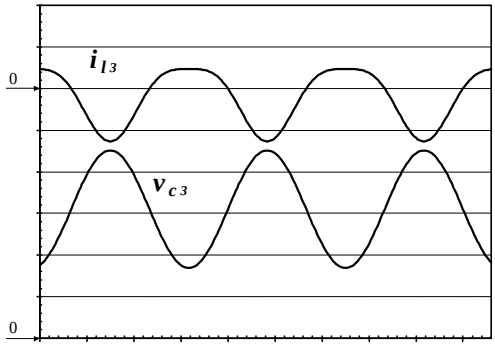

Fig. 6 Boost input current i_{l3} and output voltage v_{c3} during the line operating mode. Vertical scales: 50V/div. and 10A/div. Horizontal scale 5ms/div.

IV. Controller Description

Sliding mode control [8,9] is strong candidate for the control of the proposed UPS. This is mainly because sliding mode control usually results in very robust control systems and in many cases the average dynamic behavior of the system is insensitive to parameters uncertainties and external disturbances.

Sliding mode control has been reported for the control of both the boost PWM inverter and rectifier [7,10,11]. However, some important issues such as, current limiting during start-up and short-circuit conditions still remain unresolved.

In this section the implemented sliding mode controller is discussed and the proposed current limiter is presented.

In order to simplify the analyses and the design, each leg of the proposed UPS is separately controlled. Therefore, three SISO design problems are considered instead of a MIMO counterpart. The following sub-sections describe the implemented controllers.

A. Control of the legs 1 and 2

The control objective here is to shape the boost output voltages v_{c1} and v_{c2} into a offset sinusoidal voltage waveforms while keeping the currents through the inductors l_1 and l_2 within acceptable limits. A sliding mode surface is defined as:

$$S(x) = K_1 x_1 + K_2 x_2 = 0 \tag{17}$$

where K_1 and K_2 are the gain associated with the boost input current error x_1 and the boost output voltage error x_2 respectively.

The block diagram of the implemented sliding mode controller is shown in Fig. 7.

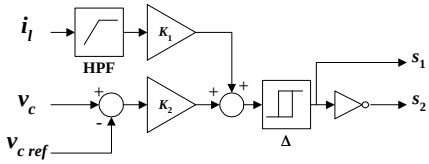

Fig. 7. Leg 1 and leg 2 sliding mode controller.

For the design, first the power components are obtained from the input and output specifications, switching frequency range and maximum ripple criteria. Then, the controller gains K_1 and K_2 are selected to guarantee the sliding mode existence condition, stability, as well as to

ensure a fast dynamic response [8].

Taking into account that it is difficult to synthesize the current reference, a first order high pass filter (HPF) has been used to generate the boost input current error x_1 [9]. The implemented high pass filter has the following transfer function:

$$\mathrm{HPF} = \frac{s+z}{s+p} \tag{18}$$

As a result, the system order is increased by one. Therefore, when in sliding mode, the boost converter still behaves as a third order system.

B. Controller of the leg 3

The control objective of the third leg is to shape the input current into a sinusoidal waveform in phase of the incoming ac line voltage. It is necessary to use two high pass filters to generate boost input current error x_1 and capacitor voltage error x_2.

The sliding mode surface in this case is defined as:

$$S(x) = K_1 x_1 + K_2 x_2 + K_3 x_3 = 0 \tag{19}$$

where K_3 is the gain associated with the ac input line current error x_3.

The block diagram of the implemented controller is shown in Fig. 8.

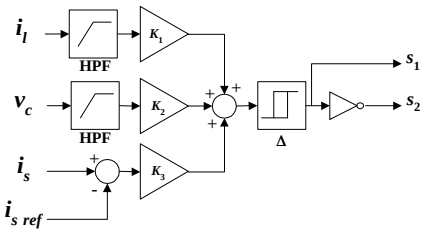

Fig. 8. Leg 3 sliding mode controller block diagram.

C. Current limiting

In UPS applications it is desirable to limit the current in the semiconductor devices during transients caused by start-up and short-circuits across the load. The start-up of the proposed UPS is critical. This is because it consists of boost rectifier and boost inverter, which can produce destructive currents through the semiconductor before the state trajectories reach the sliding surface. The sliding mode surface can be modified to the purpose of current limiting.

The procedure to reach to the current limiter is as follows: First, add the factor $K_a i_l$ to the original switching function (17). Then introduce a saturation non-linearity (SNL) in the circuit. The maximum and minimum limits of the SNL, $+i_{l\lim}$ and $-i_{l\lim}$, define the maximum and minimum values of the boost input inductor current. The output of the SNL is called $i_{l\mathrm{ref}}$ and is given by:

$$i_{l\mathrm{ref}} = \begin{cases} i_{l\lim} & \text{if} \quad (S(x)+K_a i_l) \ge i_{l\lim} \\ S(x)+K_a i_l & \text{if} \quad -i_{l\lim} < (S(x)+K_a i_l) < i_{l\lim} \\ -i_{l\lim} & \text{if} \quad (S(x)+K_a i_l) \le -i_{l\lim} \end{cases} . \tag{21}$$

The last step is to subtract the factor $K_a i_l$ which results in a new sliding surface $S_1(x)$, that is:

$$S_1(x) = i_{l\mathrm{ref}} - K_a i_l = 0 \tag{22}$$

Therefore, if the trajectories of the system are kept on the surface $S_1(x)$=0, while $i_{l\mathrm{ref}}$ is limited in acceptable values, then the current i_l will be also limited. Note that if the saturation limits are not reached the original switching function remains unaffected by the current limiter operation. This is because the factor $K_a i_l$ is add to and subtract from the original equation (17). The block diagram of the sliding mode controller with the current limiting capability is shown in Fig. 9.

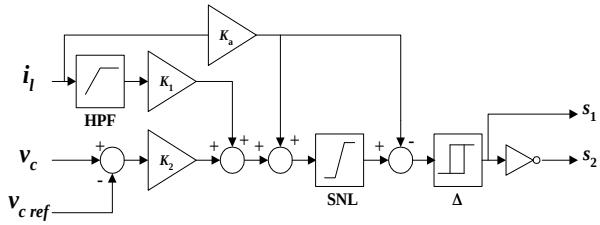

Fig. 9. Leg 1 and leg 2 sliding mode controller with the current limiter.

V. EXPERIMENTAL RESULTS

In order to validate the analysis carried out in the previous sections and to demonstrate the performance of the proposed UPS a prototype has been implemented. Experimental results for the line operating mode and backup mode are presented. The power and control circuit parameters used in the setup are shown in Table II and the nominal operating conditions are given in Table III.

A. Line Operating Mode:

The input current and the output voltage of the proposed UPS have low total harmonic distortion. This can be seen in the Fig. 10 which shows the incoming ac line voltage v_s and the input current i_s, as well as in Fig. 11 which shows the output voltage v_o and the output current i_o operating with nominal output (P_o=178W) and battery charge power(P_b=32W).

The voltages across the boost output capacitors have ac and dc components. The ac components have phase and amplitude that result in the desirable output voltage and input current. From Fig. 12 and 13 it is seen that v_{c1}, v_{c2} and v_{c3} have identical 155V dc bias and these voltages are always greater than the battery voltage. In addiction, the capacitor voltage v_{c3} is smaller than the voltage v_{c2}. This is because the incoming ac line voltage (V_s=110V) is smaller than the output voltage (V_o=120V).

Good agreement have been found between the experimental and the analytical results. This can be concluded by comparing the experimental results of Fig. 10-16 with the analytical results of Section III, Fig. 2-6. The main difference is attributed to the high frequency ripples that are neglected in the analysis.

B. Backup Mode:

The ac output voltage v_o during the backup mode is the same as observed in the line operating mode. This is because the boost output voltages v_{c1} and v_{c2} are controlled to follow their references independently of the ac incoming line voltage condition, as illustrated in Fig. 12. The correspondent output voltage is shown in the Fig. 11. The

only difference is found in the third leg which was been disable during the backup mode.

The operation of the proposed current limiter has been verify under several load transients conditions It has been found that the current limiter improves the robustness and reliability of the UPS. Fig.15 shows a transient from normal operation to overload. In this result the current limiting reference was bounded to 12 A. Indeed, it is seen that the inductor current is limited to be smaller than 12A. Fig. 18 shows the output voltage and current during a short-circuit across the load. The output voltage drops to zero and the output current is limited. On the other hand, Fig. 19 shows a transient in the load caused by a transformer start-up. Even under this condition the output voltage do not suffer variation by the asymmetrical shape of the transformer start-up current.

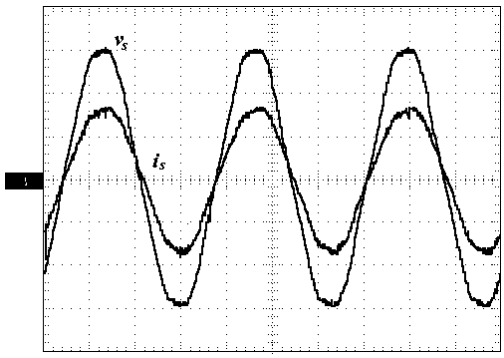

Fig. 10. UPS input voltage and current. Operating conditions as given in Table III. Vertical scales: 50V/div. and 2A/div. Horizontal scale 5ms/div.

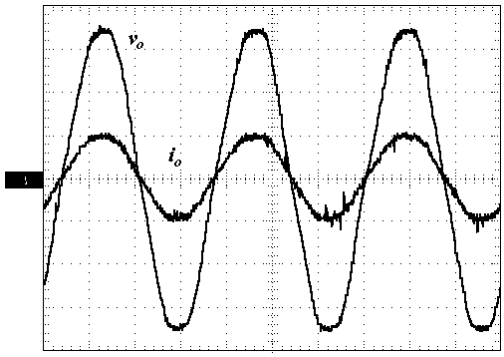

Fig. 11. UPS output voltage and current. Operating conditions as given in Table III. Vertical scales: 50V/div. and 2A/div. Horizontal scale 5ms/div.

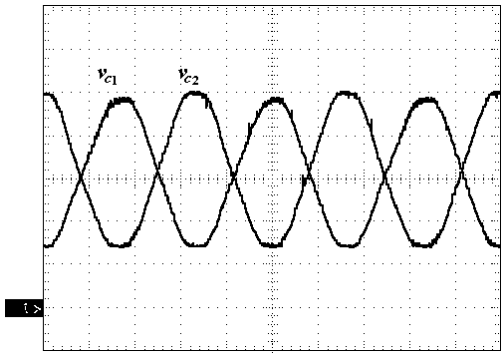

Fig. 12. Boost output voltages v_{c1} and v_{c2} during the line operating mode. Operating conditions as given in Table III. Vertical scale: 50V/div. Horizontal scale 5ms/div.

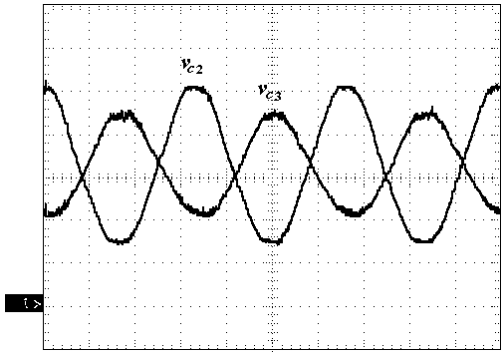

Fig. 13. Boost output voltages v_{c2} and v_{c3} during the line operating mode. Vertical scale: 50V/div. Horizontal scale 5ms/div.

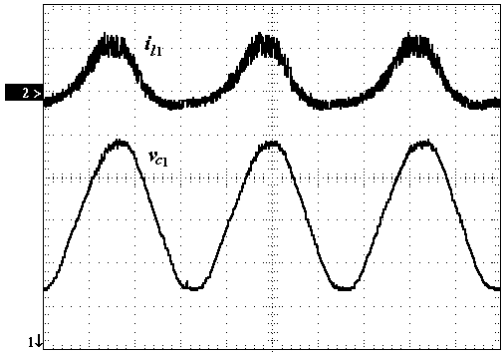

Fig. 14 Boost input current i_{l1} and output voltage v_{c1} during the line operating mode. Vertical scales: 50V/div. and 10A/div. Horizontal scale 5ms/div.

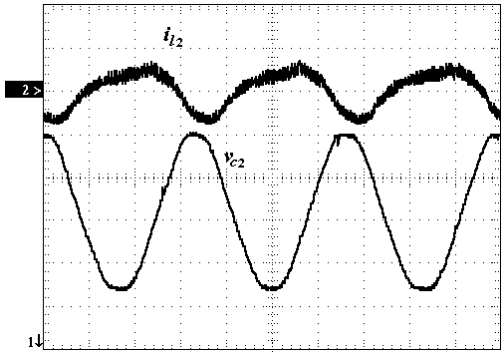

Fig. 15. Boost input current i_{l2} and output voltage v_{c2} during the line operating mode. Vertical scales: 50V/div. and 10A/div. Horizontal scale 5ms/div.

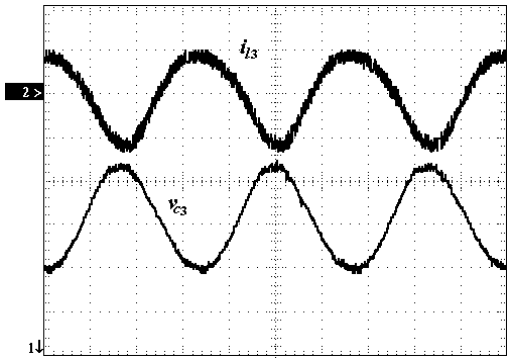

Fig. 16 Boost input current i_{l3} and output voltage v_{c3} during the line operating mode. Vertical scales: 50V/div. and 10A/div. Horizontal scale 5ms/div.

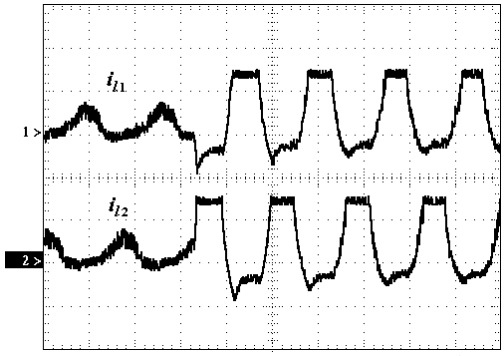

Fig. 17. Boost input currents i_{l1} and i_{l2} during the transient from normal operation to overload. Vertical scale: 10A/div. Horizontal scale 10ms/div.

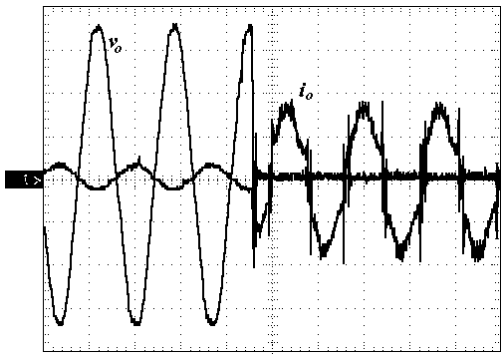

Fig. 18. UPS output voltage v_o and current i_o during a short-circuit in the load. Vertical scales: 50V/div. and 5A/div. Horizontal scale 10ms/div.

TABLE II
IMPLEMENTED UPS POWER AND CONTROL CIRCUIT PARAMETERS

THE UPS POWER PARAMETERS	
l_s	Input Filter 2.5mH
l_1,l_2,l_3	Boost Inductors 480μH
c_1,c_2,c_3	Polypropylene Capacitors 16μF/250Vac
s_1,s_2,s_3,s_4,s_5,s_6	Power MOSFET´s IRFP264
CONTROL CIRCUIT PARAMETERS LEG 1 AND LEG 2	
K_1	Inductor current error gain = 0.24
K_2	Capacitor voltage error gain = 0.08
K_a	Current limiting gain = 4.5
Δ	Sliding mode hysteresis = 0.3
z	HPF zero=0 rad/s
p	HPF pole=1000 rad/s
CONTROL CIRCUIT PARAMETERS LEG 3	
K_1	Inductor current error gain = 0.26
K_2	Capacitor voltage error gain = 0.01
K_3	Input current error gain = 1.5

TABLE III
NOMINAL UPS OPERATING CONDITIONS

LINE OPERATING MODE		**BACKUP MODE**	
Input Power	250W	Battery Input Power	200W
Output Power	178W	Output power	178W
Battery charge power	32W	--------	---
Battery Voltage	48Vdc	Battery Voltage	48Vdc
Output Voltage	120Vrms	Output Voltage	120Vr
Ac LineVoltage	110Vrms	--------	---

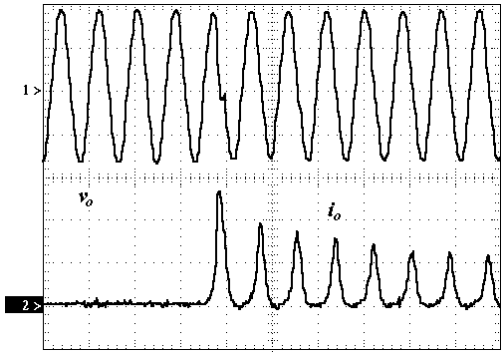

Fig. 19. UPS output voltage v_o and current i_o during a load transient caused by the start-up of a transformer. Vertical scales: 100V/div. and 2A/div. Horizontal scale 20ms/div.

VI. CONCLUSIONS

This paper presents a novel non isolated single phase UPS suitable for low power applications. The main attributes of the proposed topology are: (i) common neutral between the input and the output, (ii) flexibility for the selection of the battery voltage, (iii) it does not suffer of capacitors voltage unbalance, (iv) the proposed current limiter improves robustness and reliability. Analytical and experimental results have been presented to demonstrate the performance and to verify the feasibility of the proposed UPS.

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