Effects of the Internal Layout on the Performance of IGBT Power Modules

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***Abstract* – In this paper the issue of current sharing and gate interactions in IGBT power modules is addressed and the behavior is investigated by using a PEEC (Partial Element Equivalent Circuit) based simulation software, InCa™, for modeling and parameter extraction. The behavior of power modules in a power converter is evaluated considering the high frequency parasitic effects. A comparison between two different power modules is carried out and the importance of the internal layout of both power and control sections is point out.**

I. Introduction

IGBTs have become devices of first choice in many high frequency high power converter applications. In such applications high voltage and high current ratings are mandatory. The high current capability of the modules is obtained by paralleling multiple dies inside the module in a better fashion than with discrete devices. Particularly, designers look for an optimum internal layout of the connections to reduce the parasitic effects. However, only the power collector-emitter path has been taken into account thus far, because the minimization of stray inductance in the commutation circuit allows to utilize current capabilities of the latest chip generations as well as to optimally use the blocking voltage of the power semiconductor. The routing of all the connections inside the module is an issue, which becomes critical at high operating frequency. This paper addresses the behavior of an IGBT power module in a power converter, considering the high frequency parasitic effects such as skin and proximity effects, and the mutual coupling between the power and control sections, looking at the gate circuit behavior. Finally, a comparison between two different layouts is carried out in order to evaluate the effects of the internal layout of a power module.

II. IGBT Module Construction Technology.

The present technology used in the power module construction is based on DBC (Direct Bonded Copper) and wire-bond techniques. The silicon IGBT chips are soldered on copper, which forms the IGBT collector terminal. The DBC technique is used to connect the copper layer to the insulating ceramic that in turn is attached to a copper base plate, as shown in Fig. 1. The method is advantageous for thermal management. The connections of the emitter and of the diode anode are realized using wire-bonds. The external connections are soldered on copper bars and exit the package through the plastic case [1].

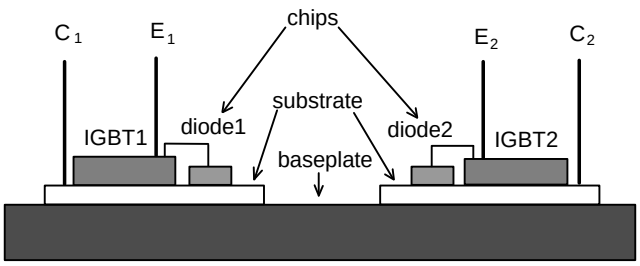

Fig. 1 - Power module cross section.

III. Limitations of the Module Technology.

The present structure of a power module minimizes the inductance of the collector and of the anti-parallel diode cathode connections due to direct soldering to the copper layer and to the DBC, but the wire-bonds limit its performance. They represent a weakness of the module from both a mechanical and electrical points of view [5]. Soldering is an issue and requires considerable manufacturing care. Wire-bonds high frequency behavior affects the operation of the chips in terms of current sharing inside the same chip due to the proximity effect, leading to unexpected thermal behavior and failure. Up to now designers have been taking care of the power routing but not to the gate behavior and its routing. The mutual coupling between the power and control sections could cause failure of the device, so a proper layout for the entire power module is needed .

In Fig. 2 and Fig. 3 are reported the internal layouts of two latest generation power modules.

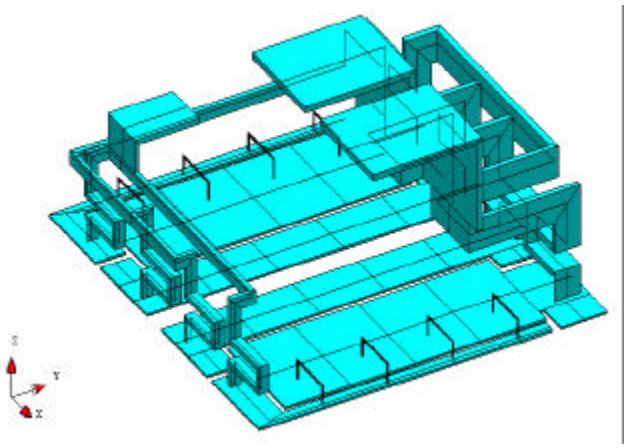

Fig. 2 - Internal layout of Module 1.

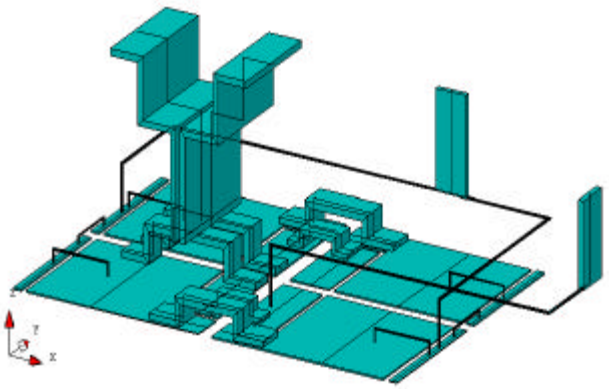

Fig. 3 - Internal layout of Module 2.

Albeit the power connections, mainly in Module 2, are optimized to obtain low inductance value, the control sections do not seem to be designed properly as they show long leads and non symmetric distribution.

Looking at a single die structure, different topologies have been found, as reported in Fig. 4 and Fig. 6. In the former there are twelve wire-bonds to connect the IGBT emitter to the external connection bar, uniformly spaced on the silicon chip, and six wire-bonds to connect the anti-parallel diode anode to the emitter external connection. The other structure uses only twelve wire-bonds for the same connections, as shown in Fig. 6. The interaction between IGBT and diode wire-bonds is expected to be different as can be evaluated from Fig. 5 and Fig. 7, which show a detailed view of such wire-bonds. Wire-bonds represent a weakness of conventional power modules in terms of mechanical and electrical issues.

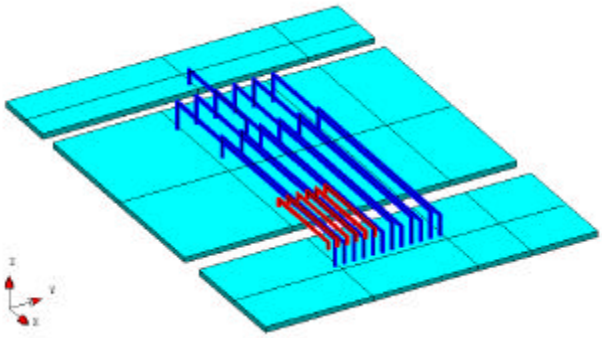

Fig. 4 - Wire-bond distribution in IGBT chip, including the anti-parallel diode connection, in Module 1.

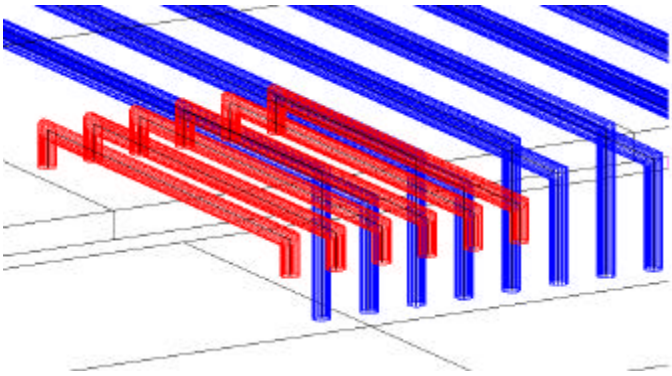

Fig. 5 - Anti-parallel diode wire-bond distribution in Module 1.

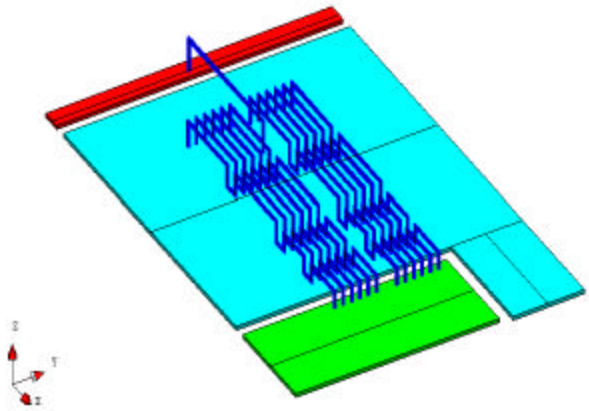

Fig. 6 - Wire-bond distribution in IGBT chip, including the anti-parallel diode connection, in Module 2.

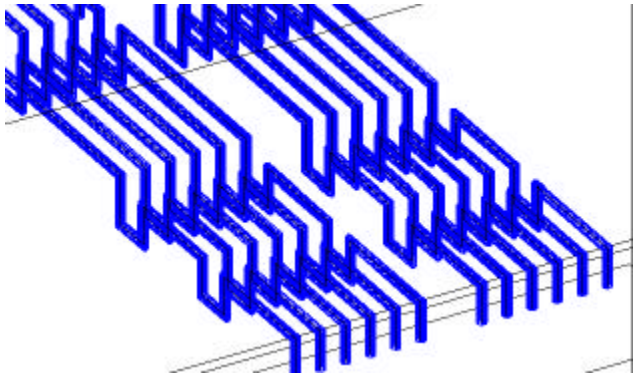

Fig. 7 - Anti-parallel diode wire-bond distribution in Module 2.

In fact, the electro-thermal behavior is strongly influenced by the current distribution inside the module and chips due to connection stray inductances, which will force the semiconductor inside the module to operate under different conditions.

IV. Analysis of the Behavior of a Power Module.

Current sharing inside the module can be analyzed in terms of sharing between multiple dies as well as inside a single chip. Position of the dies and location of the connection to the outside influence the sharing between the dies, while the position of the wire-bonds can influence current distribution within each die. This is a matter of concern in high frequency applications. Location of the dies in the module and their external connection should be symmetric to have equal current sharing. New IGBT module packages have optimized collector and emitter connections to minimize the parasitic inductance with the aim of reducing the over-voltage during switching transient avoiding voltage stress on the device.

In practice, the layout of the gate circuit is also critical. The lack of symmetry in the gate circuit can lead to unwanted gate oscillations and the inductance of the gate circuit can be critical while driving the IGBT in a hard fashion for fast switching. Particularly when an active gate drive technique is used the minimum parasitic effects are required in order to have the same operating condition for

all the chips in the module, avoiding current hogging and thermal stress. Reducing the gate parasitic inductance makes useless the presence of the integrated gate resistor present in some modern modules, leaving the gate driver designer more flexibility in the gate drive resistor selection according to the specific application.

V. Methodology and Simulation Results.

Modeling of two new generation low-inductance modules by different manufacturers has been performed in order to predict their electrical behavior, not only in terms of collector-emitter connection but also looking at the interaction with the gate control section. Parameter extraction of the parasitic inductance in multi-chip wire-bond IGBT modules has been done using INCA™ software, using the PEEC (Partial Element Equivalent Circuit) method [2]. The extracted parasitic parameters are used to build an electro-thermal model of the IGBT chips for a circuit simulator. The obtained equivalent circuits are shown in Fig. 8 and Fig. 10. In such models all the connection equivalent inductances, both self and mutual, have been modeled and the wire-bond inductances are represented in a box. The equivalent series resistances have been evaluated as well, but they are not reported in the schematics.

The parameters L_c and L_e model the power leads from the inner bar to the external power connectors; they determine the inductance value of the module as reported in manufacturer data sheets. L_g and L_{ek} are the equivalent inductance of the gate and Kelvin emitter respectively; they influence the gate performance. Since the inductance values depend on the layout, it is mandatory to consider the presence of a ground plane underneath the module simulating the grounded heat sink connection with the base plate. In Fig. 10 is represented the modeled free-wheeling diode connections with the IGBT chip. It is important to note the different wire-bond arrangements. Module 1 has separate wire-bonds for IGBT and diode chips which can influence each other, whereas Module 2 presents shared wire-bonds. Both modules have a symmetric die location on the base plate, as shown in Figs. 11 and 12, but present a non symmetric power and control lead connections.

Parameter extraction has been performed at different operating frequency to take into account the high frequency phenomena, such as skin and proximity effects, in the range from 1 kHz to 300 kHz. Some significant parameters are listed in Tab. I and Tab. II. The obtained models are implemented in SABER circuit simulator using MAST language. They are inserted in the test circuit reported in Fig. 13.

The behavior of the two considered modules has been evaluated using the same set up, looking at the effect of wire-bonds as well as of the external connection. Simulation results of the emitter wire-bond currents during a switching transient are shown in Figs. 14 and 15. As can be seen, there is 75 to 100% current difference in wire-bonds during switching transients, yielding to a different operating point for the IGBT chips. Of course this happens regardless of the internal layout, but it is related to the wire-bond technologies. The effect of the layout on the performance of a power module can be seen in current sharing between dies. Turn-on and turn-off behavior have to be analyzed separately. The current imbalance between the dies gets worse at turn-on as the gate resistance is reduced. This is to be expected since the reverse recovery current increases as the gate resistance is reduced. Also, at larger gate resistances the current rise is controlled more by the device than by the parasitics in the power circuit. At turn-off the current imbalance reduces as the gate resistance is reduced.

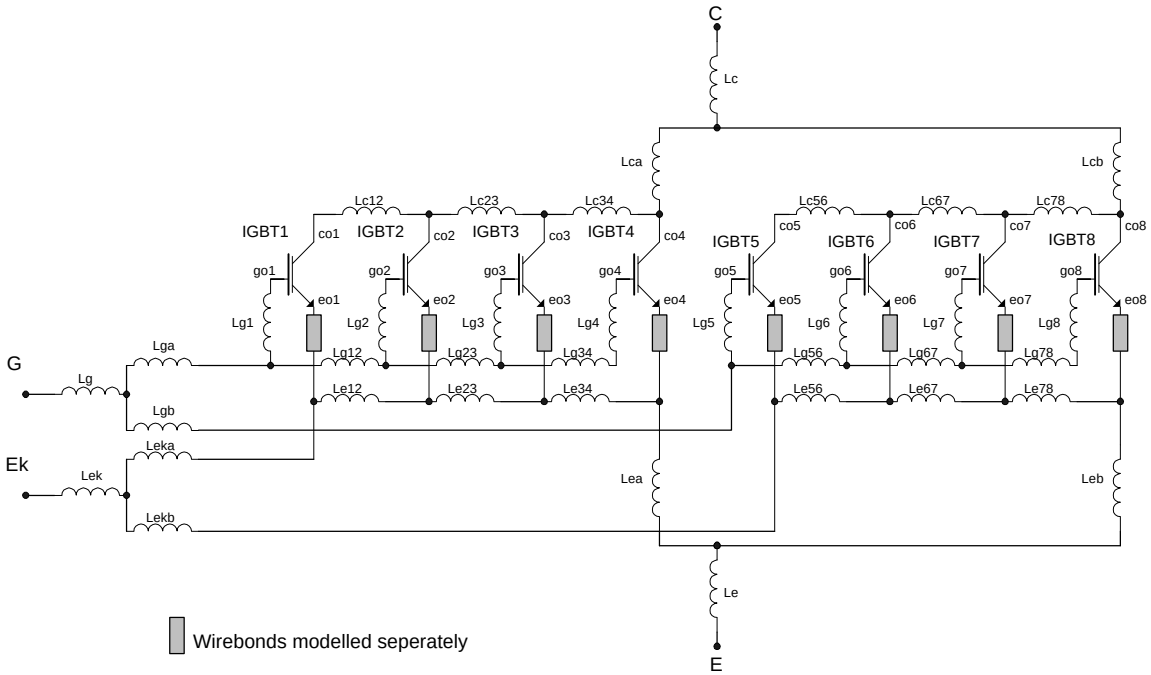

Fig. 8 – Module 1 equivalent circuit.

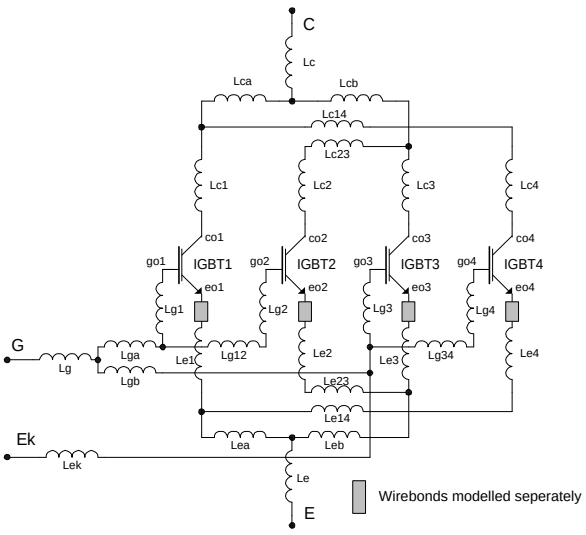

Fig. 9 – Module 2 equivalent circuit.

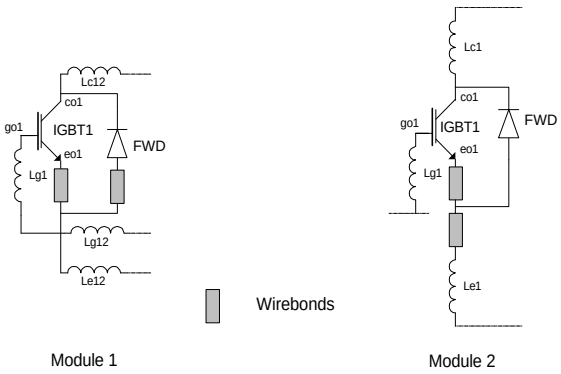

Fig. 10 - Internal connection between IGBT and anti-parallel diode.

Fig. 11 - Picture of Module 1 internal layout.

As the current error builds up over time, a quicker turn-off seems to reduce the build-up of this error and hence the current imbalance in the parallel dies. However, the current imbalance at turn-on is more critical than at turn-off because the imbalance at turn-on can be sustained during on-state, whereas the turn-off leads to a state where there is no current flow in the device.

As the mutual inductance between the gate section is removed, there is an improved current sharing in the dies at turn-on. This indicates that the gate interaction with the power section plays a significant role in the current sharing during the switching transient. Further, as all mutual inductance interactions are removed from the IGBT model, the net turn-on di/dt is reduced indicating the larger equivalent inductance seen by the IGBT dies. This confirms the "flux canceling" behavior of state-of-art IGBT modules. Also, the current imbalance in this case is similar to the case where only the gate mutual components are removed from the IGBT model. This indicates that the gate circuit mutual coupling plays a more important role than the power circuit mutual components in the model.

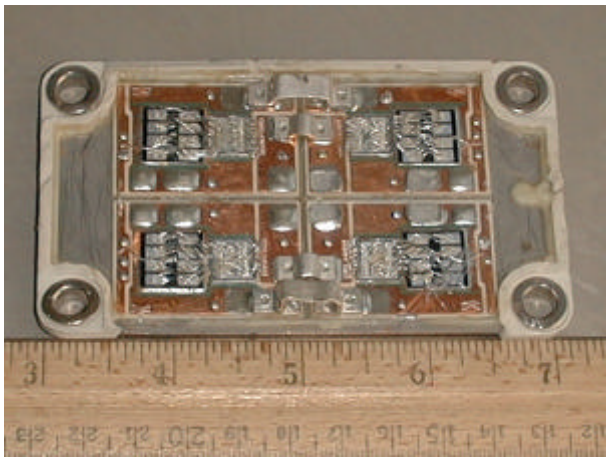

Fig. 12 - Picture of Module 2 internal layout.

Table I – Significant extracted parameters.

Value @ 10 kHz	Module 1	Module 2
Collector power leads resistance [mΩ]	C: 0.0397 C1: 0.448 C2: 0.277	C: 0.0462 C1: 0.0798 C2: 0.0798 C14: 0.111 C23: 0.111
Collector power leads self inductance [nH]	C: 9.09 C1: 42.9 C2: 18.6	C: 9.69 C1: 4.64 C2: 4.64 C14: 6.58 C23: 6.58
Emitter power leads self inductance [nH]	E: 9.08 E1: 19.1 E2: 19.1	E: 9.69 E1: 4.31 E2: 4.31 E14: 2.91 E23: 2.91
Collector-Emitter power leads mutual inductance [nH]	2.48	4.95
Collector-Gate mutual inductance [pH]	47.6	819
Wire-bond self inductance [nH]	17.9	11.1
Wire-bond mutual inductance (adjacent) [nH]	5.56	4.67
Wire-bond mutual inductance (maximum distance in the same chip) [nH]	0.461	0.198
IGBT-Diode Wire-bond mutual inductance [nH]	1.21	0.178

Table II – Frequency dependence of significant parameters.

Value/Frequency	1 kHz	10 kHz	300 kHz
Collector-emitter power leads resistance [mΩ]	0.214	0.266	0.610
Collector-emitter power leads inductance [nH]	28.1	27.2	25.7
Collector-gate mutual inductance [nH]	1.19	1.18	1.09
Wire-bond self inductance [nH]	22.8	22.6	22.5
Wire-bond mutual inductance (adjacent) [nH]	10.4	10.3	10.1
Wire-bond mutual inductance (maximum distance in the same chip) [nH]	3.25	3.22	3.21

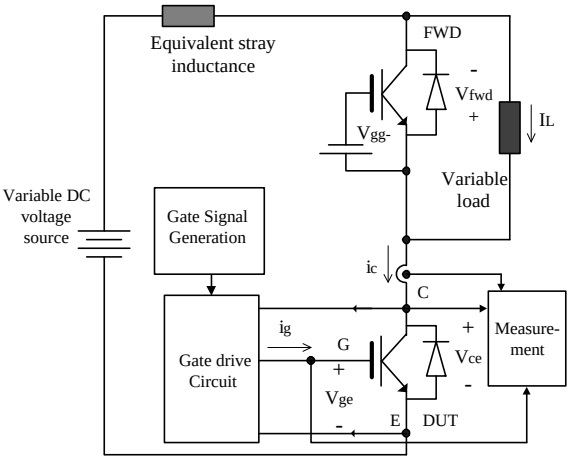

Fig. 13 - Schematic of the simulation set up.

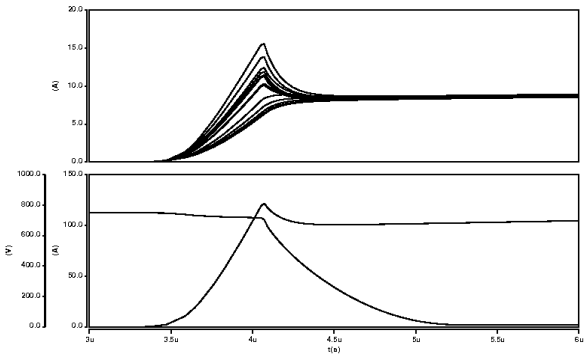

Fig. 14 - Zoomed in turn-on transient current distribution.

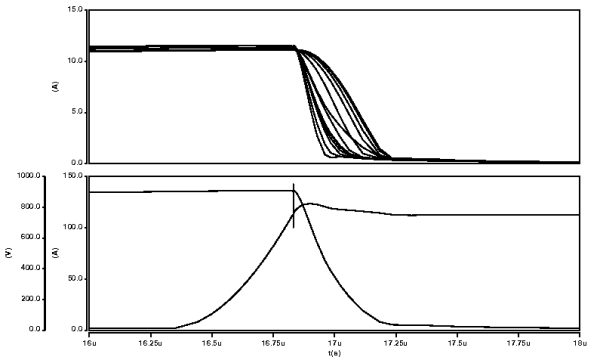

Fig. 15 - Zoomed in turn-off transient current distribution.

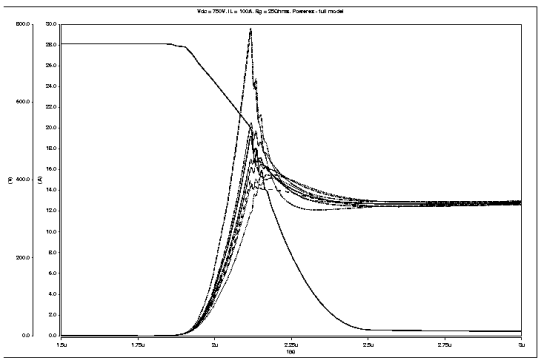

Fig. 16 - Module 1 (full model): turn-on waveforms Vce, Ic
Vdc = 750V, IL = 100A, Rg = 25 Ω.

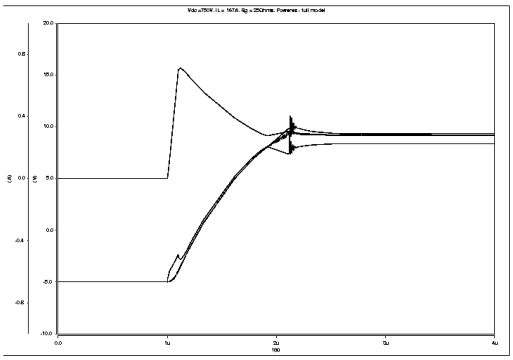

Fig. 17 – Module 1 (full model): turn-on waveforms Vge, Ig
Vdc = 750V, IL = 100A, Rg = 25 Ω.

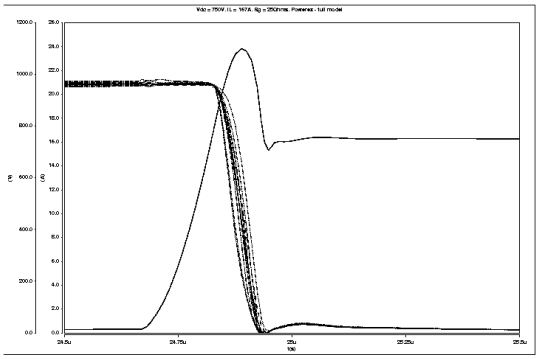

Fig. 18 – Module 1 (full model): turn-off Vce, Ic - Vdc = 750V, IL = 165A, Rg = 25 Ω.

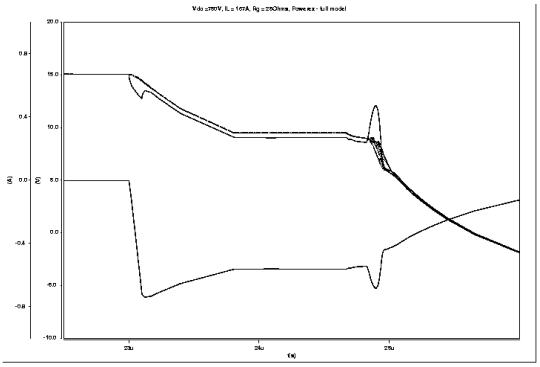

Fig. 19 – Module 1 (full model): turn-off waveforms Vge, Ig
Vdc = 750V, IL = 165A, Rg = 25 Ω.

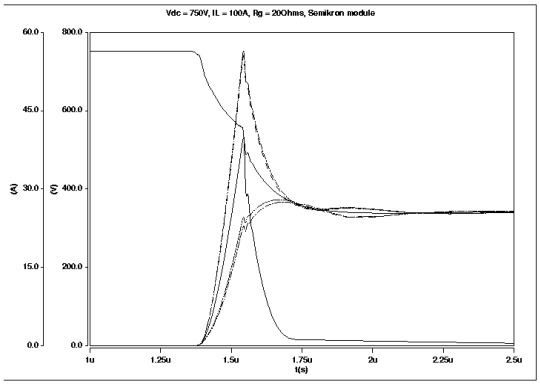

Fig. 20 – Module 2 (full model): turn-on waveforms Vce, Ic
Vdc = 750V, IL = 100A, Rg = 20 Ω.

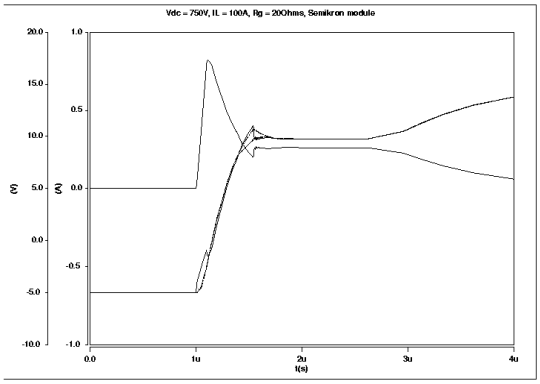

Fig. 21 – Module 2 (full model): turn-on waveforms Vge, Ig Vdc = 750V, IL = 100A, Rg = 20 Ω.

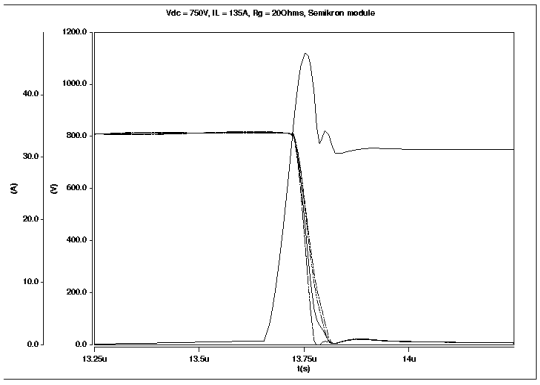

Fig. 22 – Module 2 (full model): turn-off waveforms Vce, Ic Vdc = 750V, IL = 135A, Rg = 20 Ω.

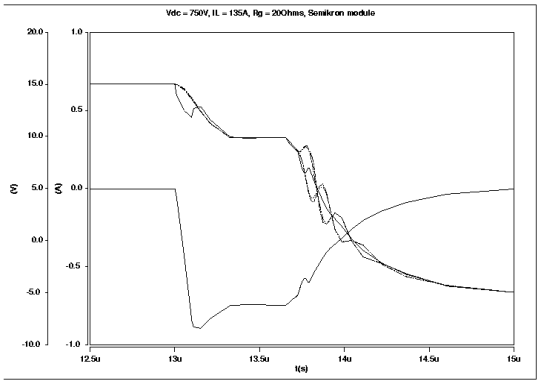

Fig. 23 – Module 2 (full model): turn-off waveforms Vge, Ig Vdc = 750V, IL = 135A, Rg = 20 Ω.

VI. Experimental Results

Experimental results are not so easy to take due to the impossibility to use voltage or current probe inside the modules. Thus, the waveforms that can be looked at are limited to the external connections of the power module. Particularly, modules are tested in a clamped inductive load circuit, shown in Fig. 13. Collector current and voltage and gate current and voltage are reported in Figs. 24 to 27. In Figs. 24 and 26 are reported turn on waveforms for both modules, whereas in Figs. 25 and 27 are reported turn-off waveforms . As can be seen the experimental results are in good agreement with the simulation output. The different power and control connection route inside the module is the reason of different behavior of the two analyzed devices.

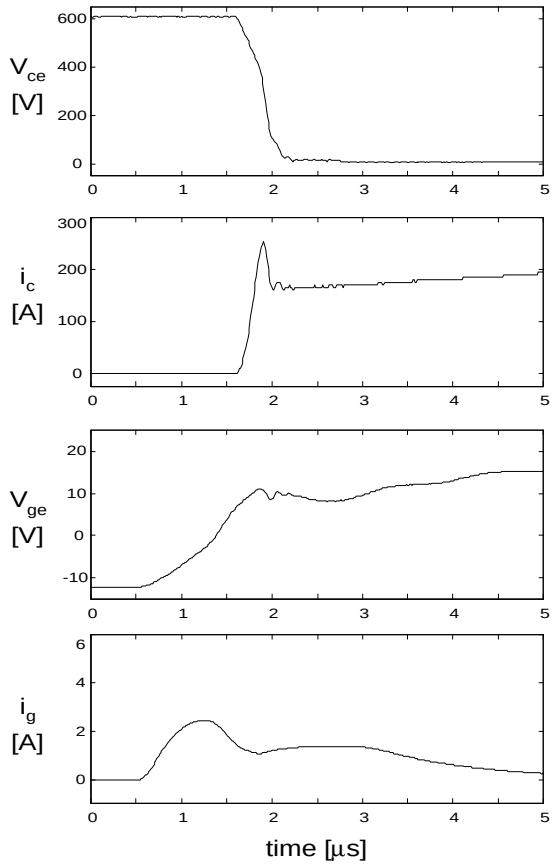

Fig. 24 - Module 1 turn-on waveforms. Vdc = 600V, Rg = 5.6 Ω.

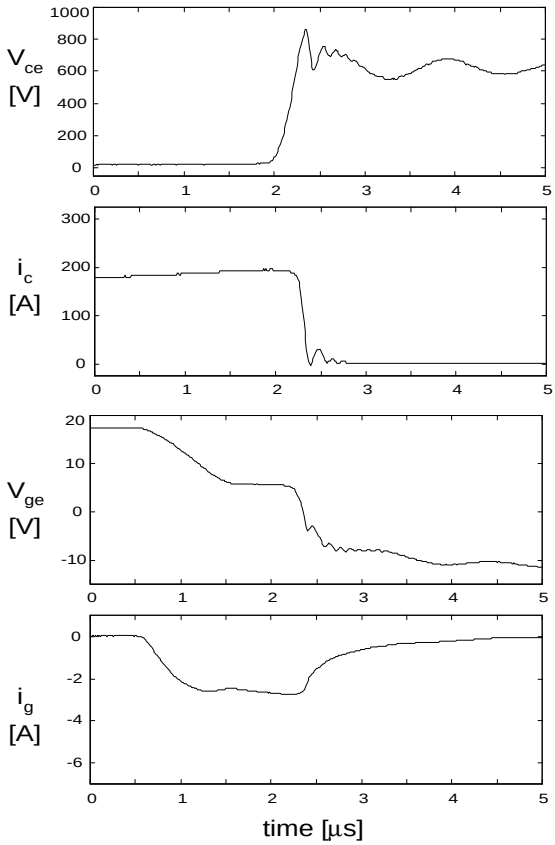

Fig. 25 – Module 1 turn-off waveforms. Vdc = 600V, Rg = 5.6 Ω.

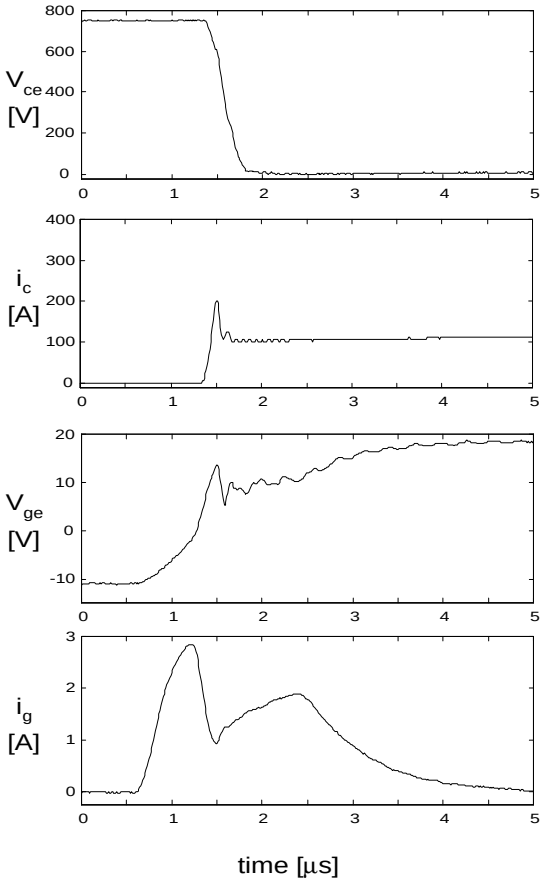

Fig. 26- Module 2 turn-on waveforms. Vdc =750V, Rg = 3.6Ω.

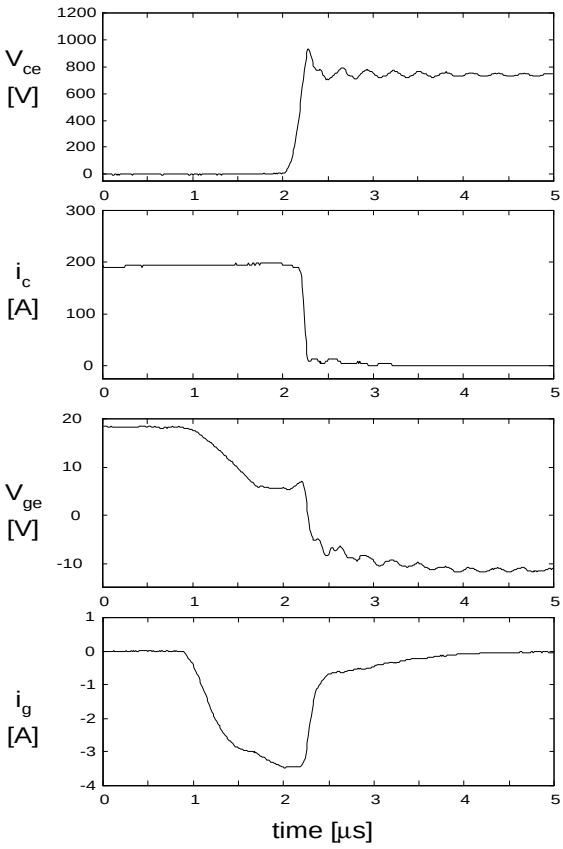

Fig. 27- Module 2 turn-off waveforms. Vdc =750V, Rg = 3.6Ω.

Module 2 gate waveforms are noisier than Module 1, according to the simulation result, since it has a worse internal gate circuit and higher parasitic inductances. This is the result of a non optimized gate circuit which yields to an unsuitable power module for active driving.

VII. Conclusion

In this paper modeling of recent hybrid power IGBT modules has been performed and their behavior has been evaluated in terms of power and control circuits. The obtained results can be used to design any hybrid power electronic integrated structure such as IPM (Intelligent Power Module) which are being more widely used. The impact of the power circuit as well as the control section on the behavior of a power module and then on the system has been analyzed end experimentally validated.

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