Electronics Design Automation Tools in a Power Electronics Laboratory at PUCMINAS

Prof. Lauro de Vilhena Brandão Machado Neto,
Prof. Flávio Maurício de Souza,
Rafael Couto Figueiredo, Rodrigo Costa Ivo

Power Electronics Laboratory
Department Electronic Engineering-PUCMINAS
Av. Dom José Gaspar, 500, P. 03, S. 104,
30.535-610, Belo Horizonte, MG, Brasil,
Tel. +55-31-319.4115 Fax +55-31-319.4224
Email: lvilhena@pucminas.br
Site: www.ipuc.pucmg.br/labep

***Abstract* - The aim of this paper is present the Power Electronics Laboratory, Labep of the Department of Electronics Engineering and Telecommunication from the Polytechnic Institute of PUCMINAS, focusing the electronics design automation tools uses in the laboratory for development of practical courses and research projects. First present the hardware and software infrastructure available. For exemplify the development of practical classes using the infrastructure, is present a step by step procedure for the study of the triphase thyristores inverter. The results of the procedure are presented and analyzed**

I. INTRODUCTION

The technology of Electronic Design Automation is fundamental to the global development of electronic industry [1]. This study concerns our first experience to introduce EDA tools in the Power Electronics Laboratory of the Department of Electronic Engineering and Telecommunication from the Polytechnic Institute of PUCMINAS.

Initially, the courses taught in the various programs of the Institute and their contents are presented, as well as development and research work carried out by the students as practical activity, incorporating new technologies in the area of Power Electronics. The hardware and software used in the Laboratory of Power Electronics are then presented, with the inter-relationship of use of those tools. The final version of the paper will contain an experiment highlighting that inter-relationship.

II. POWER ELECTRONICS COURSES

LABEP, the Laboratory of Power Electronics from PUCMINAS, is part of the Nucleus of Power Electronics of the Department of Electronic Engineering and Telecommunication. The Nucleus integrates the programs of Electronic Engineering and Telecommunication, Electrical Engineering and Mechatronics Engineering in what concerns Power Electronics and Industrial Electronics. Each academic semester offers a set of disciplines with the focus determined by the different aims of the many programs in which they are taught. Table I indicates the disciplines with their respective courses.

TABLE I
DISCIPLINES OF THE NUCLEUS OF POWER ELECTRONICS

ENG. COURSES	COURSES
ELECTRONIC ENGINEERING AND TELECOMUNICATIONS	Power Electronics I – Switches Power Electronics II – Laboratory I Power Electronics III – Converters Power Electronics IV – Laboratory II
ELECTRIC ENGINEERING	Industrial Electronics I Laboratory of Industrial Electronics
MECATHRONICS ENGINEERING	Power Electronics I Power Electronics II Laboratory of Power Electronics

Theoretical disciplines are aimed at developing the subject related to static power converters, beginning with an introduction and proceeding with a detailed study of static switches and the basic topologies of converters, and ending up with details of the main applications in electric machine drives and control and feeding systems.

LABEP aims at developing practical disciplines offered by the nucleus, with the support needed by the particular focus of each discipline. Besides that major aim, the present framework of the laboratory favors the development of research within the area as well as in related fields, such as electrical drives, robotics, renewable energy and control and automation.

Projects elaborated in each discipline are carried out with the available tools in the laboratory and the results obtained so far have met the needs proposed by each program in what concerns Power Electronics. TABLE II shows the practical projects and activities currently developed in the laboratory.

III. POWER ELECTRONICS LABORATORY'S HARDWARE

The infrastructure of the Power Electronic Laboratory consists of 07 PCs, 01 Ultra 5 SUN Workstation, 02 printers, 1 Hub and 1 PC for development, all of which are net-connected. Figure 1 presents the layout and Fig. 2 shows some pictures of the laboratory.

TABLE II
DEVELOPMENT AND RESEARCH PROJECTS

TITLE	FOMENTATION
Mentor Graphics System Administration	PUCMINAS MENTOR GRAPHICS
Design of dc/dc Converters for Automotive Systems Applications	FAPEMIG / PUCMINAS FIAT S. A.
Intelligent Energy Conditioning and Electric System Driver for an AGV	FINEP PUCMINAS
Automation of a Data Collection System for Photovoltaic Panels	GREEN PUCMINAS
Electric Fancing with Photovoltaic Panels	GREEN PUCMINAS
A Photovoltaic System for a Grains Dryer	GREEN PUCMINAS

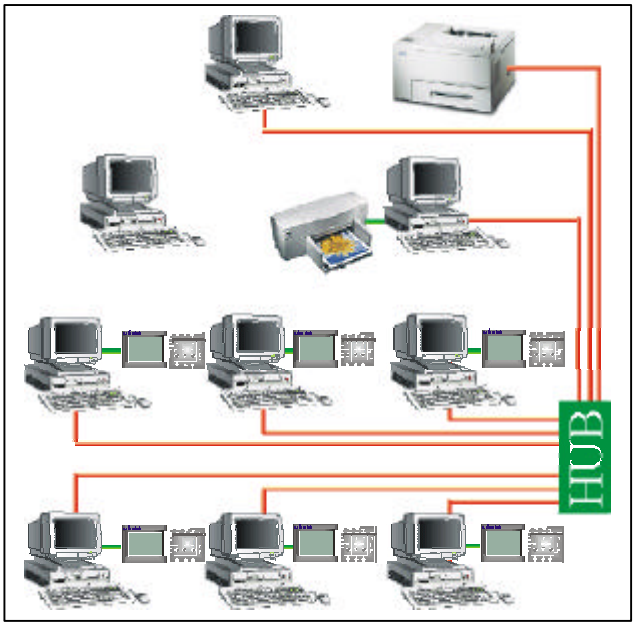


Fig. 1. Layout of the Power Electronics Laboratory

Fig 2. Picture of the Power Electronics Laboratory

The Mentor Graphics tools, license files and users' register are implanted in the Workstation. At present, almost 150 users are registered.

The PCs are used as Workstation terminals; for such, the XWIN-32 software is used, according to the Agreement STARNET-PUCMINAS.

There are also 4 sets of 19 Modules for experiments of rectifiers, choppers, inverters and cycleconverters. All modules make use of the thyristore technology. Practical work developed by the students use up-to-date technologies of power semiconductors, such as MOSFET and IGBT, and dedicated integrated circuits. The laboratory also has 4 sets of microprocessor based inverters and induction motors donated by Siemens (SIMATEC). Digital oscilloscopes are connected to the PCs, allowing the acquisition of the wave forms of students' experiments; and functions generators are also provided.

IV. POWER ELECTRONICS LABORATORY'S SOFTWARE

The aim of this remodeling is to offer students an initial contact with the tools of Electronic Design Automation (EDA) of Mentor Graphics Corporation (Agreement Mentor Graphics/PUCMINAS). Those tools consist of a SPICE (Simulation Program with Integrated Circuit Emphasis) and allow schematic capture with symbols or in analogical or digital hardware description language (HDL), going through simulation, checking, synthesis, Printed Circuit Board (PCB) and the elaboration of integrated circuits layouts (ASIC - Application-Specific Integrated Circuits).

The starting point of the Mentor Graphics tool set uses Design Manager, a software that consists of a graphic shell based on Falcon Framework and allows the start of applications and project management. All operations that may affect projects must be performed through the Design Manager. For instance, the Design Manager allows the deletion, re-naming and copy of projects, while the UNIX *rm*, *ren* and *cp* commands allow the same functions but do not use the database. Fig. 3 presents a window of the Design Manager.

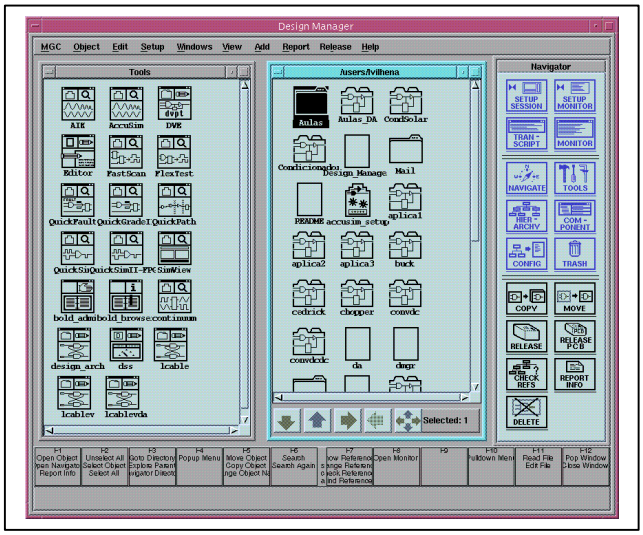


Fig. 3. Design Manager Window

The next step is the Mentor Graphics tool Design Architect, which allows the schematic capture (project input). Design Architect is the basic editor for design processes, such as PCB, ASIC, FPGA and IC. In only one tool there are symbols, schema, VHDL editors and Top-Down Hierarchical Design resources, including the creation of blocks and hierarchic navigation. The tool consists of a design program that recognizes electronic components, connections, bus and electrical rules. With Design Architect the students draws schematics which will be used later on in simulations. The Fig. 4 shows the window of the Design Architect.

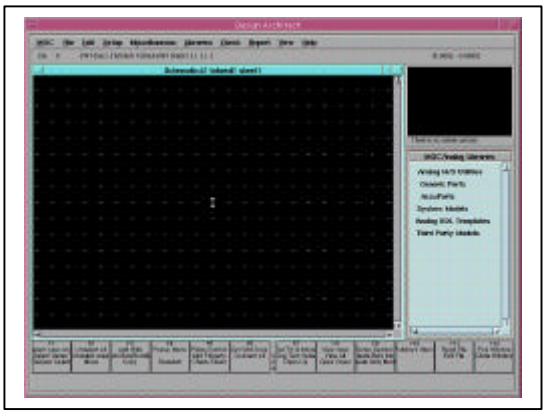


Fig. 4. Design Architect Window

AccuSim II analog simulator performs complete circuit and system analysis from top-down to bottom-up. You can specify internal parameters for display and annotate the schematic diagram with saved parameters or general comments. AccuSim has the capability to spawn remote simulation runs or to operate in batch mode. AccuSim II also offers a powerful compiled analog behavioral language similar to VHDL called HDL-A. Automatic circuit partitioning and One Step Relaxation (OSR) algorithm speed up mixed-mode simulations. S-, Y- and Z-parameter extractions let you develop and run AC simulations on complex structures, and Monte Carlo analysis suite allows statistical and worst-case analysis [1]. The Fig. 5 present a window of the AccuSim II.

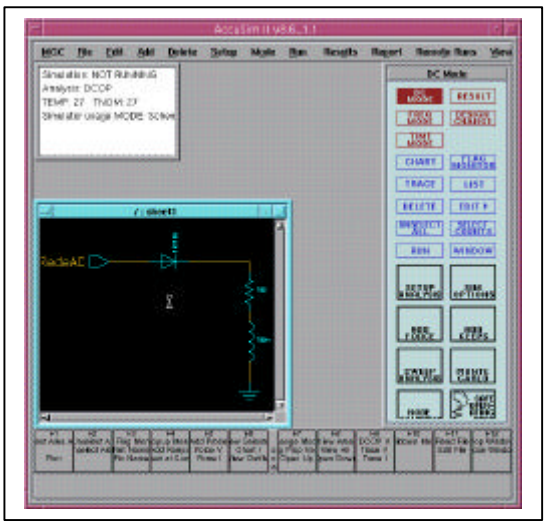


Fig. 5. AccuSim Window

V. METHODOLOGY OF PRACTICAL CLASSES

A. Initial Study of the Simulation Tools

Students will get initial information on the software system installed through the development of three practices called Tutorials, elaborated by the teaching staff. In those tutorials, students will work sequentially with the Design Manager, Design Architect, and AccuSim, learning how to handle them, and visualising all their potentiality. By the end of the third tutorial, students will carry out the simulation of a quite simple circuit, already studied in theoretical classes, and in which they will be able to apply the concepts learned. Those tutorials are distributed among students, but are available in Internet too, in the site of the Power Electronics Laboratory (www.ipuc.pucmg.br/labep) and in the Menthor Graphics Higher Education Program Technical Support Site (www.ge.ee.wustl.edu/HEP).

B. Simulation:

The next development step is the study of power electronics circuits making use of the simulation software. All didactic modules available in the laboratory are already implemented in the system library. Students are informed about that and how to access them. With the help of a tutorial of practical classes, they select the blocks corresponding to each module, and needed for the assemblage of the circuit to be studied, using Design Architect. Once the assemblage is accomplished on the screen, AccuSim is activated to perform the simulation. Students will follow the procedure scheduled in the tutorial. Results, which may be wave forms and/or current and voltage measures, are displayed on the screen, and may be printed for an evaluation report. Through the observation of the circuit performance results, other alternatives for study are proposed, such components value alteration, fault simulation, study and elimination of harmonics, among others.

C. Assemblage

The next step in the development of disciplines of practical classes is the circuits physical assemblage, anticipated in the guide. With its help, students select modules according to the assemblage and perform the procedure. Results are also collected and analysed through the observation in instruments such as oscilloscope and multimeters. In our case, the digital oscilloscope is plugged to the minicomputer, thus allowing circuit wave forms to be captured and analysed with the software itself.

D. Comparison

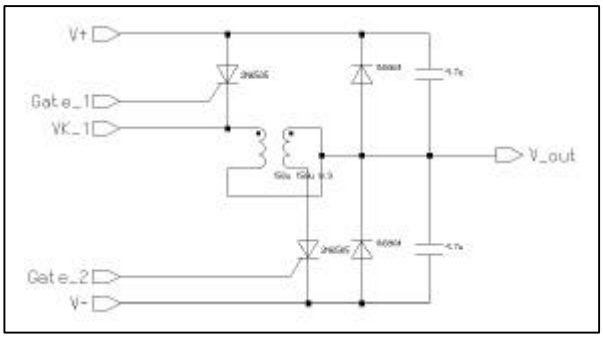
To end up the study sequence of a certain circuit, students are stimulated to make a comparative study between the two methodologies and write a report relating their conclusions and suggestions.

VI. EXAMPLE OF APPLICATION

Aiming at exemplifying that methodology, what follows is the sequence of a study development of a Triphase Thyristored Inverter using the MacMurray-Bedford method of forced commutation.

A. Simulation

The individual circuits and symbols for simulation are displayed in Fig. from 6 to 11, and the complete circuit assembled by Design Architect is shown in Fig. 12.



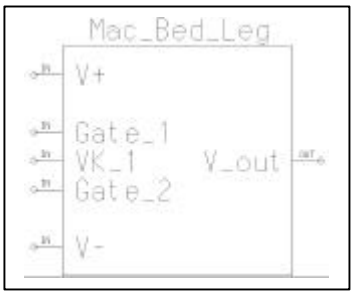
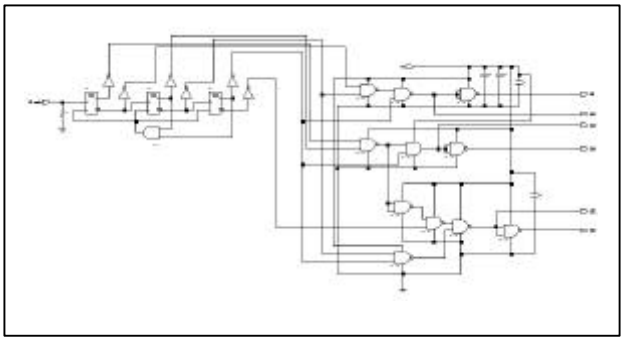


Fig. 6. Power Stage (Inverter Leg)



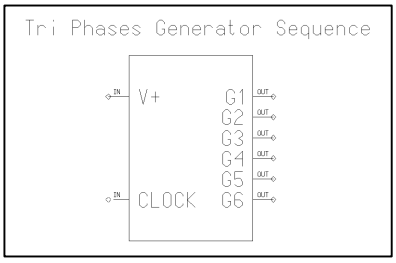
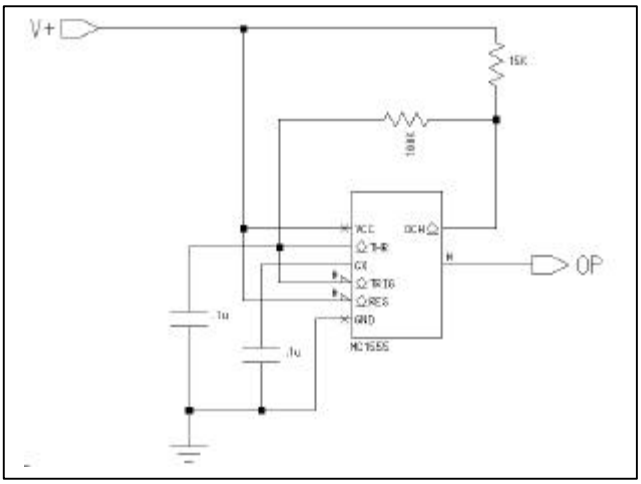


Fig. 7. Triphase Generator Sequence



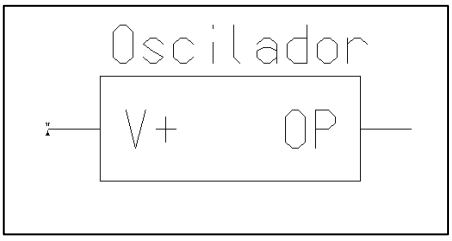
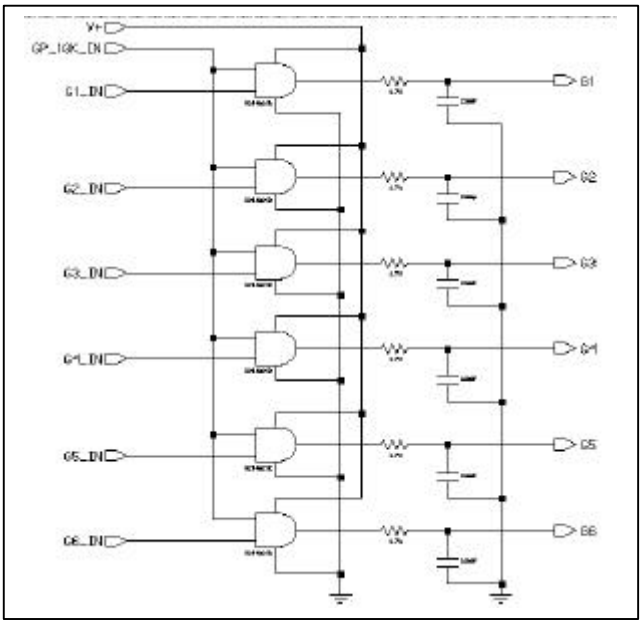


Fig. 8. Pulse Generator



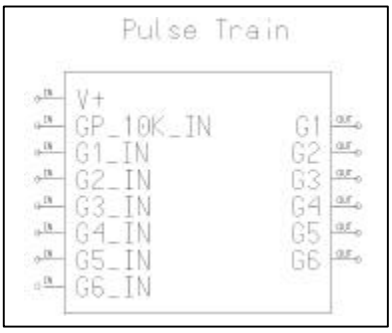


Fig. 9. Pulse Train

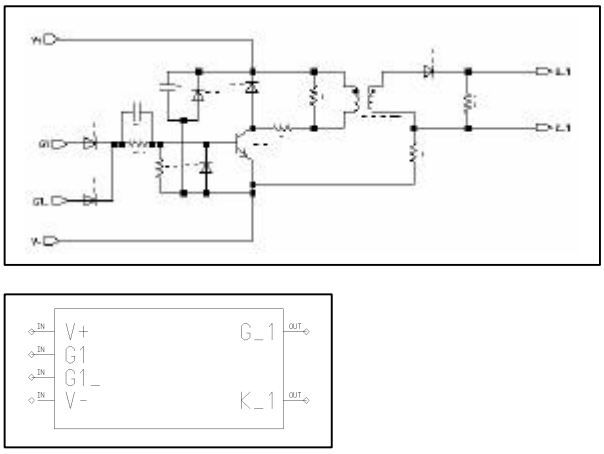


Fig. 10. Pulse Amplifier

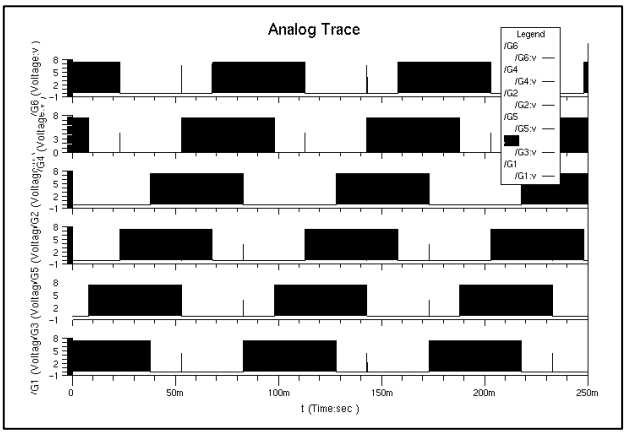


Fig. 13. Triphase Pulse Train

B. Simulation Results

The voltage wave form in the output (phase 1) is shown in Fig. 12 and the sequence pulse is presented in Fig, 13.

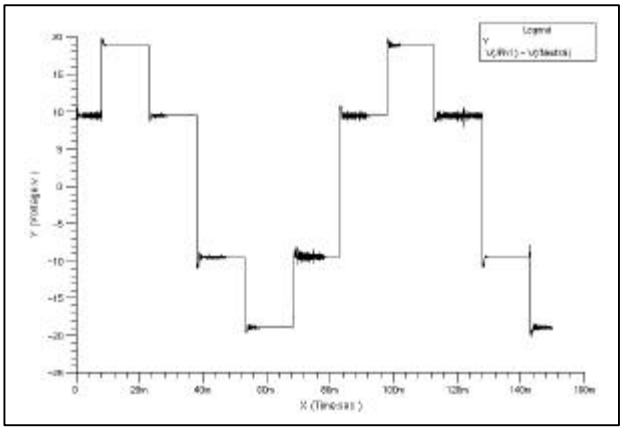


Fig. 12. Voltage wave form in the Phase 1

C. Assemblage

Fig. 14 present the oscillogram of the inverter output through a digital oscilloscope plugged to a µcomputer.

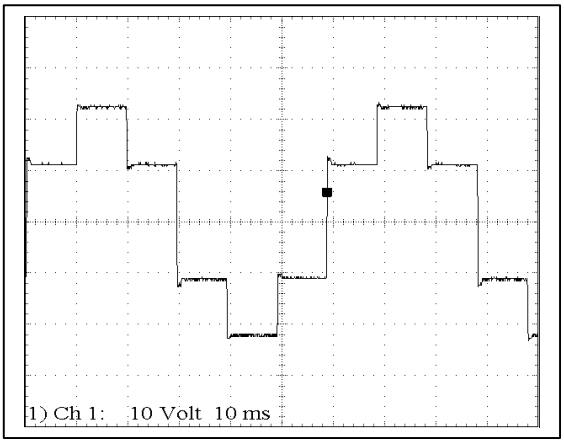


Fig. 14. Oscilogram of the Inverter Output

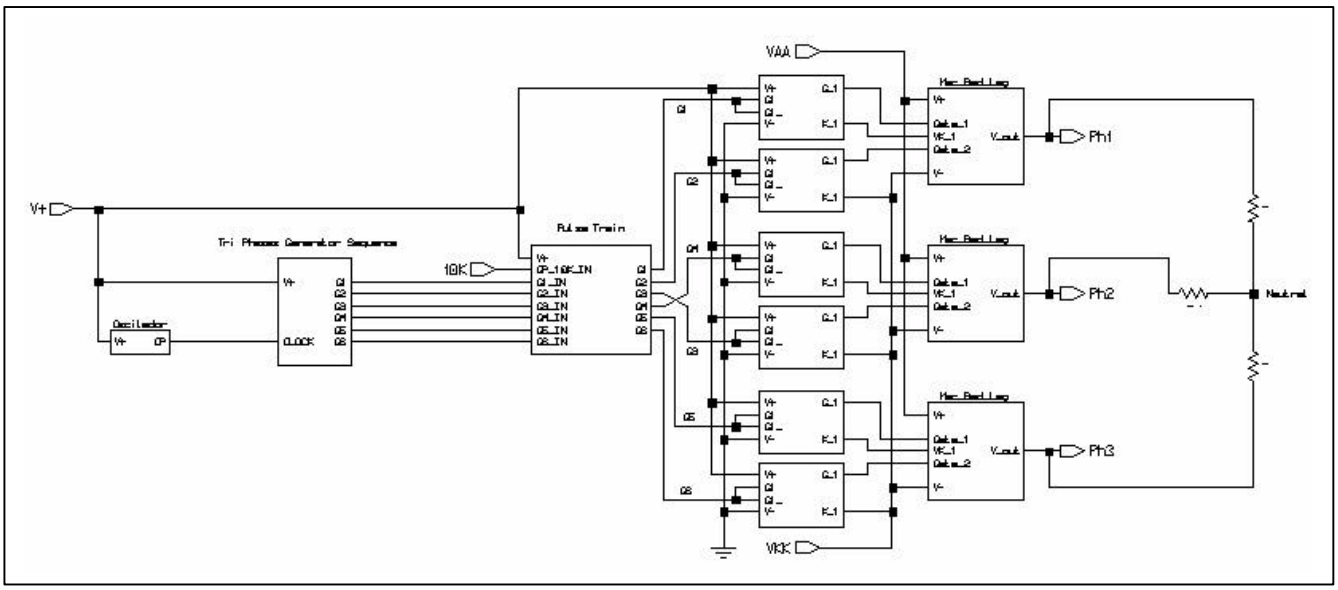


Fig. 11. Complete Circuit in Design Architect

The complete assemblage is displayed below.

VII. CONCLUSION

The methodology presented was introduced with great success and enthusiastic, despite the beginner difficulties in the administration of the system and the change of the culture, both from students and from the professors.
A continuum attendance is necessary and was detected that we have to introduce the Electronics Design Automation (EDA) Tools at the beginner of the course.
The next step is the expansion of the system and introduce the others tools from the package from Mentor Graphics Corporation.

VIII. BIBLIOGRAPHY

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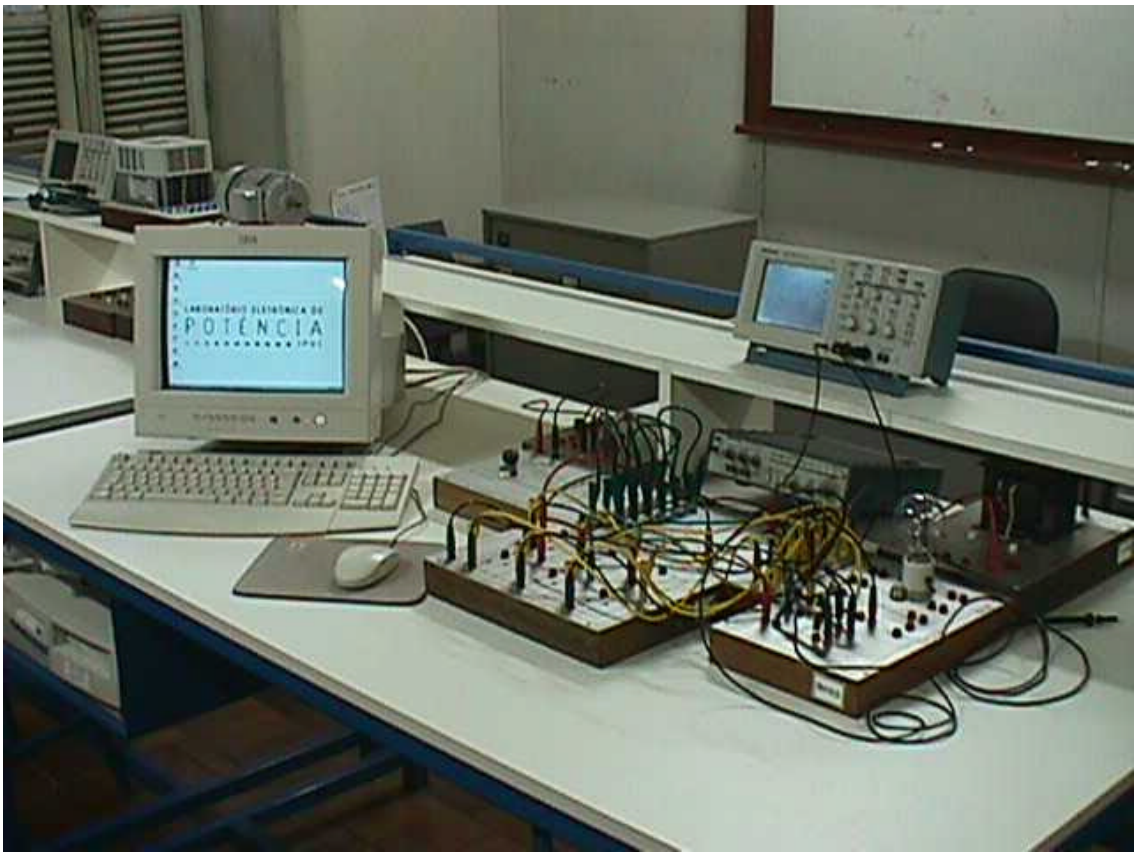
IX. ACKNOWLEDGEMENT

To Mentor Graphics Corporation (Agreement Mentor Graphics-PUCMINAS) and Star Net Communications .
To all the students and staff from PUCMINAS.