A NEW HYBRID MULTILEVEL SYSTEM FOR MEDIUM VOLTAGE AC MOTOR DRIVES

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***Abstract* – This paper proposes a new structure to implement the input dc voltage sources of hybrid multilevel inverters applied to medium voltage ac motor drives. As each cell of a hybrid multilevel inverter processes distinct power levels, this paper proposes a generalized design methodology to determine the phase angles among the secondary windings of the input isolation transformer, even when the active power levels processed by the cells and/or the impedances of the uncontrolled rectifiers are different. The phase angles are obtained to eliminate the fifth harmonic of the input current, once this harmonic component presents an amplitude considerably higher than the amplitude of the other harmonics. Therefore, the proposed design methodology increases the input power factor and reduces the input current THD.**

I. INTRODUCTION

Voltage-source multilevel converters have been used for medium voltage ac motor drives, because low voltage levels are imposed to semiconductor devices and, therefore, voltage change rates are lower than that obtained with two-level converters [1]–[6]. In addition, multilevel adjustable speed drives (ASD's) synthesize waveforms with reduced harmonic content and also present increased efficiency, because they usually operate with low switching frequency.

Among several multilevel structures, hybrid multilevel inverters have been receiving increasing attention [7]–[9], mainly because they can synthesize voltage waveforms with a reduced harmonic content using few series-connected cells. This advantage is achieved by using distinct voltage levels in the different cells, allowing more levels to be created in the output voltage, then minimizing the output voltage THD (Total Harmonic Distortion), and making possible the reduction or even the elimination of the output filter [10]–[12]. In addition, a hybrid modulation strategy can be used so that the higher power cells are modulated to switch at low frequency and lowest power cell is modulated to switch at high frequency. Then, a high-voltage high-quality waveform is synthesized, switching at high frequency only the lowest power cell. On the other hand, as each cell processes distinct power levels, a generalized approach about the implementation of the input dc voltage sources for applications with active power transfer was not still presented.

In applications with active power flow, as medium voltage ASD's, the dc voltage sources of all H-bridge (single-phase full-bridge inverter) cells must supply this active power and maintain the average value of the dc bus voltage constant during the specified time interval. Therefore, the H-bridge cells must be connected to a power supply system, such as batteries [1], or in the utility grid [5], [6]. One of the simplest alternatives to obtain a dc voltage source from the utility grid is to employ an uncontrolled six-pulse rectifier. This rectifier is composed of a three-phase diode bridge rectifier and a filter capacitor, utilized to reduce the dc bus voltage ripple. However, the current waveforms drawn from the utility grid present high THD when the input inductance is not large enough to minimize the harmonic currents [13], [14].

Since it is necessary to employ an isolation transformer with several secondary windings to implement the isolated dc voltage sources, it is possible to reduce the harmonic components of the input currents with multipulse connection of rectifiers [15]–[17]. With adequate phase angles among the secondary windings, the harmonic currents generated by one diode rectifier can be cancelled by the harmonics produced by the others rectifiers. Nevertheless, some low frequency harmonics of the input currents will be eliminated only when the active power levels processed by all rectifiers and their impedances (input inductances and dc bus capacitors) are equal, by using the conventional design methodology to compute the phase angles among the secondary windings. Hence, for hybrid multilevel inverters, where the H-bridge cells usually process distinct power levels, the line currents will present some undesired harmonics by using the conventional design methodology.

To overcome this problem, this paper proposes a new structure to implement the input dc voltage sources of hybrid multilevel inverters applied to medium voltage ac motor drives, which is illustrated in Fig. 1. The isolation transformer has one primary winding, and $3n$ secondary windings that supply energy for all cells that compose the three-phase multilevel inverter. A new generalized design methodology to determine the phase angles among the secondary windings of the isolation transformer, even when the active power levels processed by each rectifier and/or their impedances are different, is proposed. The phase angles are obtained to eliminate the fifth harmonic of the input currents, once this harmonic component presents an amplitude considerably higher than the amplitudes of the other components [13], [14]. With this, the proposed design methodology increases the input power factor and reduces the input current THD.

II. DESCRIPTION OF HYBRID MULTILEVEL INVERTERS

A phase output voltage of a multilevel inverter with n series-connected H-bridge cells per phase is obtained by summing the output voltages of the cells, e.g.:

$$v_a(t) = v_{a,1}(t) + v_{a,2}(t) + ... + v_{a,n}(t) . \quad (1)$$

If the dc voltage sources of all H-bridge cells are equal, the maximum number of levels of the phase voltage is:

$$m = 1 + 2n . \quad (2)$$

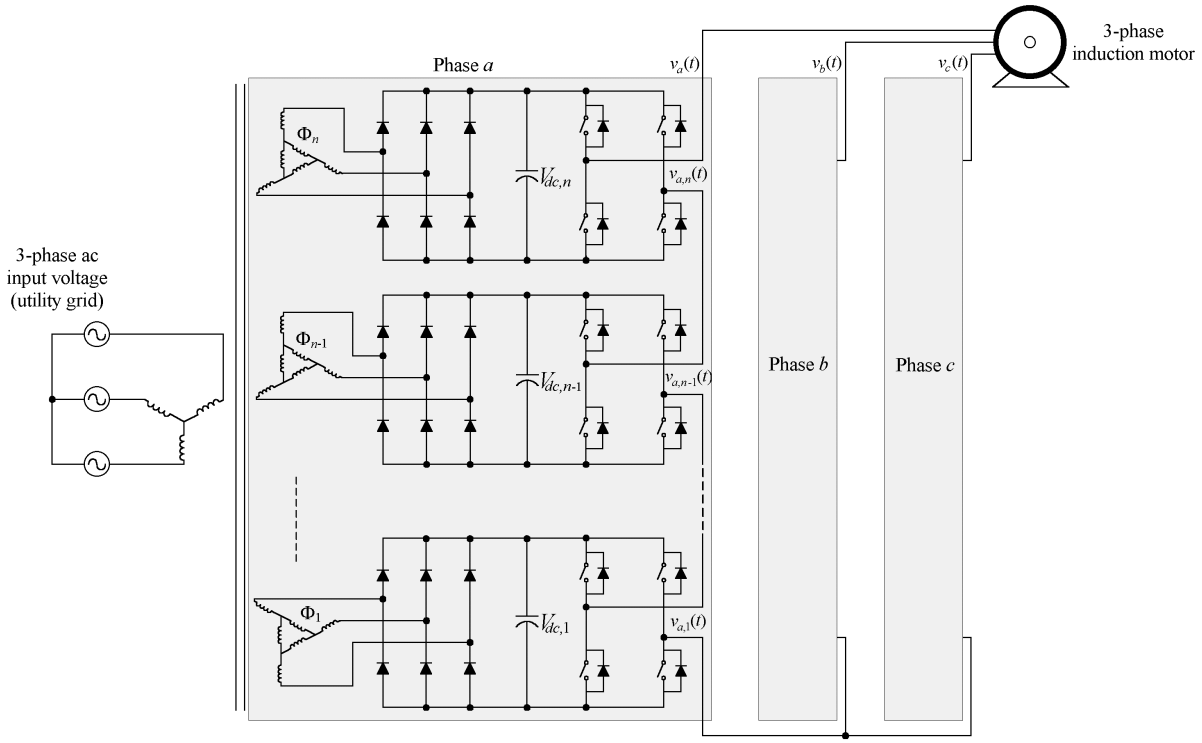

Fig. 1 – Proposed hybrid multilevel system.

On the other hand, if at least one of the dc voltage sources is different from the other ones, the multilevel inverter shown in Fig. 1 can be called asymmetric multilevel inverter [10]. Considering that the lowest dc voltage source ($V_{dc,1}$) is chosen as base value for the p.u. notation of the hybrid inverter, the normalized values of all dc voltage sources must be natural numbers ($V_j \in \mathbb{N}$) and they also must respect the following relation to obtain uniform step multilevel waveforms [11]:

$$V_j \le 1+2\sum_{k=1}^{j-1} V_k \ , \quad j = 2, 3, ..., n \tag{3}$$

where it is also considered that the dc voltage sources are arranged in an increasing way, that is:

$$V_1 \le V_2 \le V_3 \le ... \le V_n. \tag{4}$$

Therefore, the maximum number of levels of an output phase voltage waveform can be given by [11]:

$$m = 1+2\sigma_n \tag{5}$$

where:

$$\sigma_n = \sum_{j=1}^{n} V_j \ . \tag{6}$$

From (2) and (5)–(6) it is possible to verify that asymmetric multilevel inverters can generate a larger number of levels with the same number of cells.

However, the power devices of different cells are subjected to distinct voltage levels. Therefore, a hybrid approach has been proposed in [7], called hybrid multilevel inverter, for high power and high performance applications. This hybrid multilevel inverter uses a synergistic approach that combines the fast switching ability of IGBT's and large voltage blocking capability of IGCT's. These devices are modulated differently, so that the IGCT inverter (high power inverter) is modulated at fundamental frequency of the inverter output and the IGBT inverter (low power inverter) is modulated at high frequency.

A. Modulation strategy

A generalized modulation strategy has been presented in [8], which uses stepped voltage waveform synthesis in higher power H-bridge cells in conjunction with high frequency pulsewidth modulation (PWM) in the lowest power cell.

However, to synthesize a voltage waveform modulated at high frequency among all adjacent voltage steps, switching at high frequency only the lowest power inverter, the dc voltage sources must satisfy the following equation:

$$V_j \le 2\sum_{k=1}^{j-1} V_k \ , \quad j = 2, 3, ..., n. \tag{7}$$

Thus, if (7) is satisfied, the spectral response of the output voltage depends on the switching frequency of the lowest power cell, while the power processing depends basically on the inverter with the highest dc voltage source.

Fig. 2 shows that the reference signal of the hybrid multilevel inverter is the command signal of the H-bridge cell with highest dc voltage source (V_n). This signal is compared with a voltage level corresponding to the sum of all smaller dc voltage sources (σ_{n-1}). The command signal of the j^{th} cell is the difference between the command signal and the output voltage

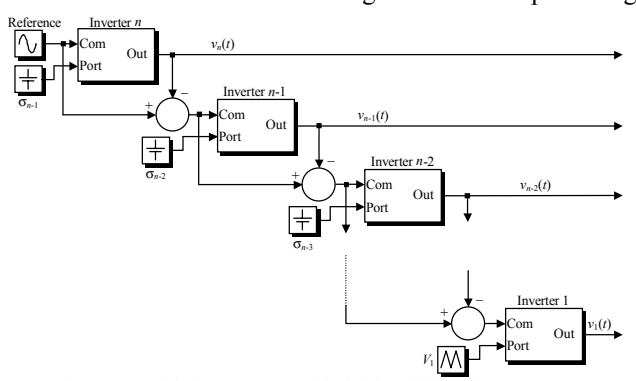

Fig. 2 – Modulation strategy of hybrid multilevel inverters [8].

of the inverter j+1. In this way, the command signal of the j^{th} cell contains information about the harmonic content of the output voltage of all higher voltage cells. This command signal is compared to the sum of all voltage sources until the inverter j–1 (σ_{j-1}). Finally, the command signal of the lowest power inverter is compared with a high frequency signal, resulting in a high frequency output voltage.

B. Design methodology

There are several possibilities for setting the value of the dc voltage source of each cell to obtain the same number of levels, mainly when the number of levels increases. For instance, although different configurations of dc voltage sources can result in the same number of levels, the power processing of the overall hybrid multilevel inverter is different from one configuration to another. Therefore, it is important to employ a design methodology to define the number of cells and the value of the dc voltage sources [19].

The definition of the number of cells and the dc voltage levels of each cell must consider the topologies employed to implement these sources. Assuming that all dc voltage sources will be implemented with six-pulse diode rectifiers, then it will not be possible to regenerate energy from load to source. Then, Fig. 3 presents the normalized values of the dc voltage sources that ensure that all H-bridge cells will not regenerate energy in motor mode for any value of m_a (amplitude modulation index). Consequently, with these dc voltage levels, it is possible to use six-pulse diode rectifiers.

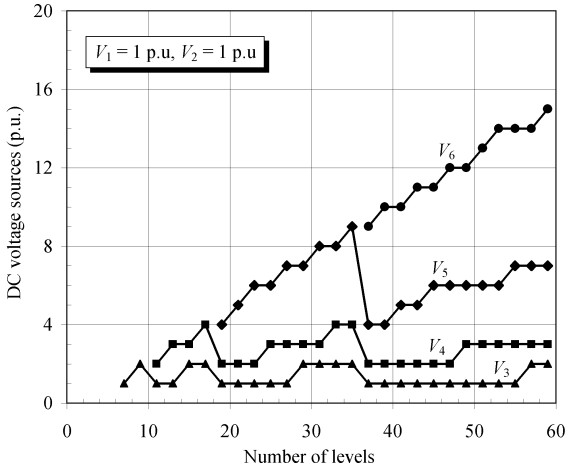

Fig. 3 – Normalized dc voltage sources of the H-bridge cells.

III. Analysis of Six-pulse Diode Rectifiers

The harmonic analysis of the input currents drawn by the six-pulse rectifier shown in Fig. 4 assumes a symmetrical three-phase power supply, represented by a sinusoidal phase voltage V_s and an inductance L_s. Considering that this rectifier composes the input stage of a high-power ASD, the internal resistances of the input power supply are small and, therefore, they are neglected in this analysis. Moreover, the dc bus capacitor C_b produces a dc voltage V_{dc} with low frequency ripple, and the dc current source I_{dc} models the rectifier load, due to the harmonic current path provided by the capacitor.

Moreover, it is interesting to normalize all variables and system parameters so that the results obtained in the harmonic analysis are independent from voltage and current levels of the six-pulse rectifier. Hence, the rms value of the

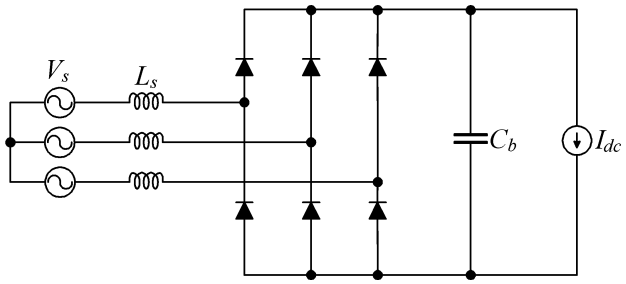

Fig. 4 – Equivalent circuit of the uncontrolled six-pulse rectifier.

power supply phase voltage is chosen as voltage base value and the fundamental component of the input line current is defined as current base value for the input stage, that is:

$$V_{base} = V_s \quad \text{and} \quad I_{base} = \frac{V_{dc} I_{dc}}{3 V_s \cos \varphi_1} \tag{8}$$

where φ_1 is the phase displacement between the phase voltage and the fundamental component of the line current.

After, the diode rectifier depicted in Fig. 4 has been extensively simulated to evaluate its harmonic performance. It is well known that the input current harmonics sensibly decrease for higher values of X_L. In addition, fifth and seventh harmonics present the highest amplitudes [13], [14]. Therefore, these two harmonics should be eliminated or minimized to reduce the input current THD.

Thus, as fifth harmonic presents the highest amplitude, Fig. 5 shows the fifth harmonic amplitude I_5, referred to the fundamental current I_1, $i_5 = I_5/I_1$, versus the input reactance

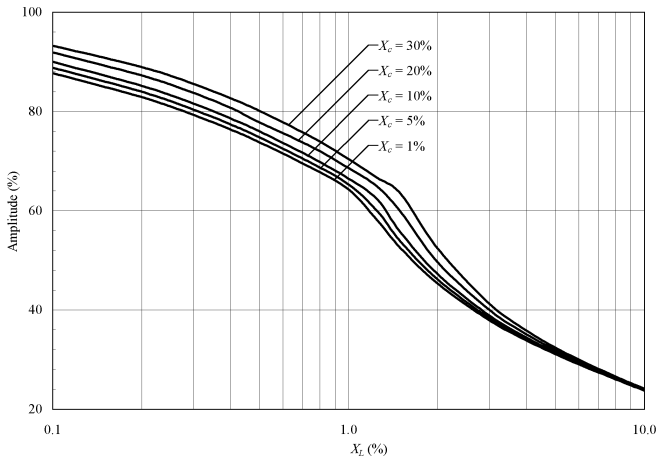

Fig. 5 – Fifth harmonic amplitude, i_5, versus input reactance, X_L.

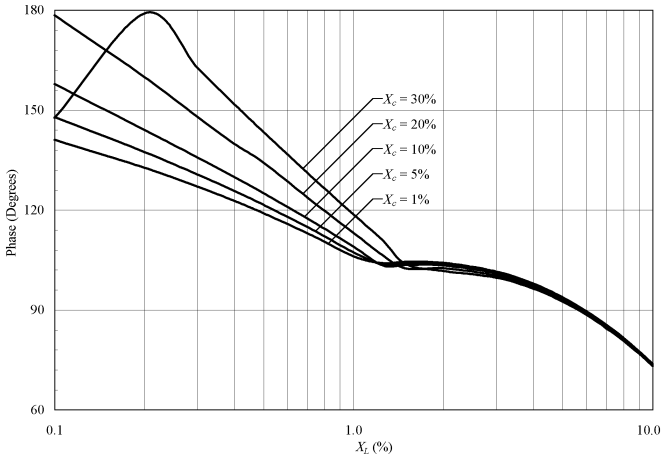

Fig. 6 – Phase angle of the fifth harmonic, φ_5, versus input reactance, X_L.

and for different values of the dc bus capacitor reactance. Besides the knowledge of the fifth harmonic amplitude, it is also necessary to identify its phase angle to eliminate this harmonic with multipulse connection of rectifiers. Hence, Fig. 6 presents the phase angle between the phase voltage and the fifth harmonic of its respective line current.

Consequently, from this analysis it is possible to estimate the fifth harmonic of the input currents. These results will be used after in a generalized design methodology for multipulse connection of rectifiers.

IV. MULTIPULSE CONNECTION OF RECTIFIERS: CONVENTIONAL DESIGN METHODOLOGY

Uncontrolled diode rectifiers have been widely used in the input stage of medium voltage ASD's [3]–[5], because they have a simple structure and a smaller cost, if compared with controlled rectifiers [6], [18]. Nevertheless, besides these uncontrolled rectifiers do not allow the bi-directional power flow between load and source, the input currents of six-pulse diode rectifiers with capacitive filter present high THD.

As an input transformer must be employed to implement the isolated voltage sources, it is possible to reduce the harmonic content of the input currents by using multipulse connection of rectifiers [15]–[17]. Multipulse converters use the phase shift among the secondary windings of transformers to cancel some harmonic currents and to reduce the dc bus voltage ripple. Consequently, besides the galvanic isolation among the dc voltage sources and the voltage adaptation between the input source and the dc voltage sources of the different cells, the input transformer can be utilized to minimize the harmonic content of the input currents and also to reduce the common-mode voltage at the induction motor terminals [20].

Fig. 7 shows the equivalent circuit of one phase of the input stage of a multilevel inverter with n series-connected cells. The dc current source $I_{cc,j}$ represents the average value of the input current of the j^{th} H-bridge cell. Then, due to the fact that each cell presents distinct voltage and current ratings, each input rectifier has its own voltage and current base values.

The secondary windings line currents (input currents of the six-pulse diode rectifiers) can be expressed by:

$$\begin{aligned} i_{S,n}(t) &= \sum_{h=1,5,7,\ldots}^{\infty} \sqrt{2} I_{h,n} \sin\left[h\left(\omega t + \Phi_n\right) + \varphi_{h,n}\right] \\ &\vdots \\ i_{S,2}(t) &= \sum_{h=1,5,7,\ldots}^{\infty} \sqrt{2} I_{h,2} \sin\left[h\left(\omega t + \Phi_2\right) + \varphi_{h,2}\right] \\ i_{S,1}(t) &= \sum_{h=1,5,7,\ldots}^{\infty} \sqrt{2} I_{h,1} \sin\left[h\left(\omega t + \Phi_1\right) + \varphi_{h,1}\right] \end{aligned} \tag{9}$$

where Φ_j is the angle between the line voltage of the j^{th} secondary winding and the primary line voltage, and $I_{h,j}$ and $\varphi_{h,j}$ are, respectively, the rms value and the phase (without consider the phase shift between the primary and secondary windings) of the h^{th} input current harmonic of the six-pulse diode rectifier that supply the j^{th} cell.

The corresponding primary line current is given by:

$$i_P(t) = \sum_{j=1,2,\ldots}^{n} \hat{i}_{S,j}(t) \tag{10}$$

where $\hat{i}_{S,j}(t)$ is the line current in the j^{th} secondary winding, reflected to the primary side.

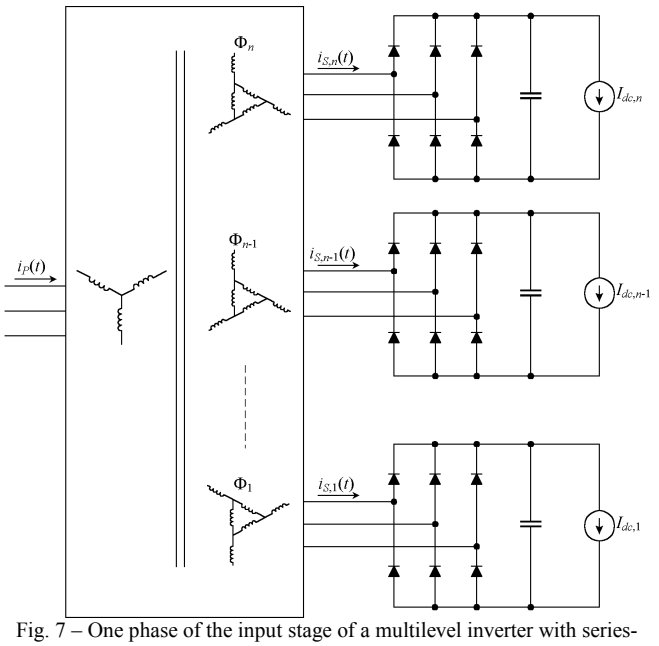

Fig. 7 – One phase of the input stage of a multilevel inverter with series-connected H-bridge cells.

All positive-sequence current components (I_1, I_7, I_{13}, ...) of the primary line current *lag* their corresponding positive-sequence current components in the secondary line current by a phase angle Φ_j. On the other hand, all negative-sequence current components (I_5, I_{11}, I_{17}, ...) of the primary line current *lead* their corresponding harmonic components in the secondary line current by the same angle Φ_j [17].

Consequently, the primary line current is:

$$i_P(t) = \sum_{j=1,2,\ldots}^{n} \frac{\sqrt{2} V_{S,j}}{V_P} \left[\begin{array}{l} I_{1,j} \sin\left(\omega t + \varphi_{1,j}\right) + \\ + \sum_{h=5,11,\ldots}^{\infty} I_{h,j} \sin\left[h\left(\omega t + \Phi_j\right) + \Phi_j + \varphi_{h,j}\right] + \\ + \sum_{h=7,13,\ldots}^{\infty} I_{h,j} \sin\left[h\left(\omega t + \Phi_j\right) - \Phi_j + \varphi_{h,j}\right] \end{array} \right] \tag{11}$$

where V_P is the primary line voltage and $V_{S,j}$ is the line voltage of the j^{th} secondary winding.

Negative and positive-sequence harmonics, respectively, of the primary line currents can be represented as vectors, that is:

$$I_{h,P}\angle\varphi_{h,P} = \sum_{j=1,2,\ldots}^{n} \frac{V_{S,j}}{V_P} I_{h,j} \angle\left(h+1\right)\Phi_j + \varphi_{h,j} \text{ , } h = 5, 11, \ldots \tag{12}$$

$$I_{h,P}\angle\varphi_{h,P} = \sum_{j=1,2,\ldots}^{n} \frac{V_{S,j}}{V_P} I_{h,j} \angle\left(h-1\right)\Phi_j + \varphi_{h,j} \text{ , } h = 7, 13, \ldots \tag{13}$$

Therefore, from (12), (13) and considering that the impedances and active power levels processed by all cells are equal, it is possible to verify that the minimum phase angle ($\Delta\Phi_{min}$) among the secondary windings to cancel the dominant input current harmonics can be obtained by:

$$\Delta\Phi_{min} = 60/n \text{ (degrees).} \tag{14}$$

Fig. 8 presents simulation results of a multipulse connection with three identical rectifiers, which process the same active power levels. The phase shift among the secondary windings

are obtained from (14), so that: $\Phi_1 = -20º$, $\Phi_2 = +20º$ e $\Phi_3 = 0º$. Fig. 8(a) shows the input currents of the six-pulse rectifiers. Although these currents present high THD, Fig. 8(b) illustrates that the primary line current has a reduced harmonic content (THD = 4.5%). The high-quality current drawn from the utility is due to the multipulse connection, which eliminates the 5th, 7th, 11th and 13th harmonics, as can be seen in Fig. 8(c).

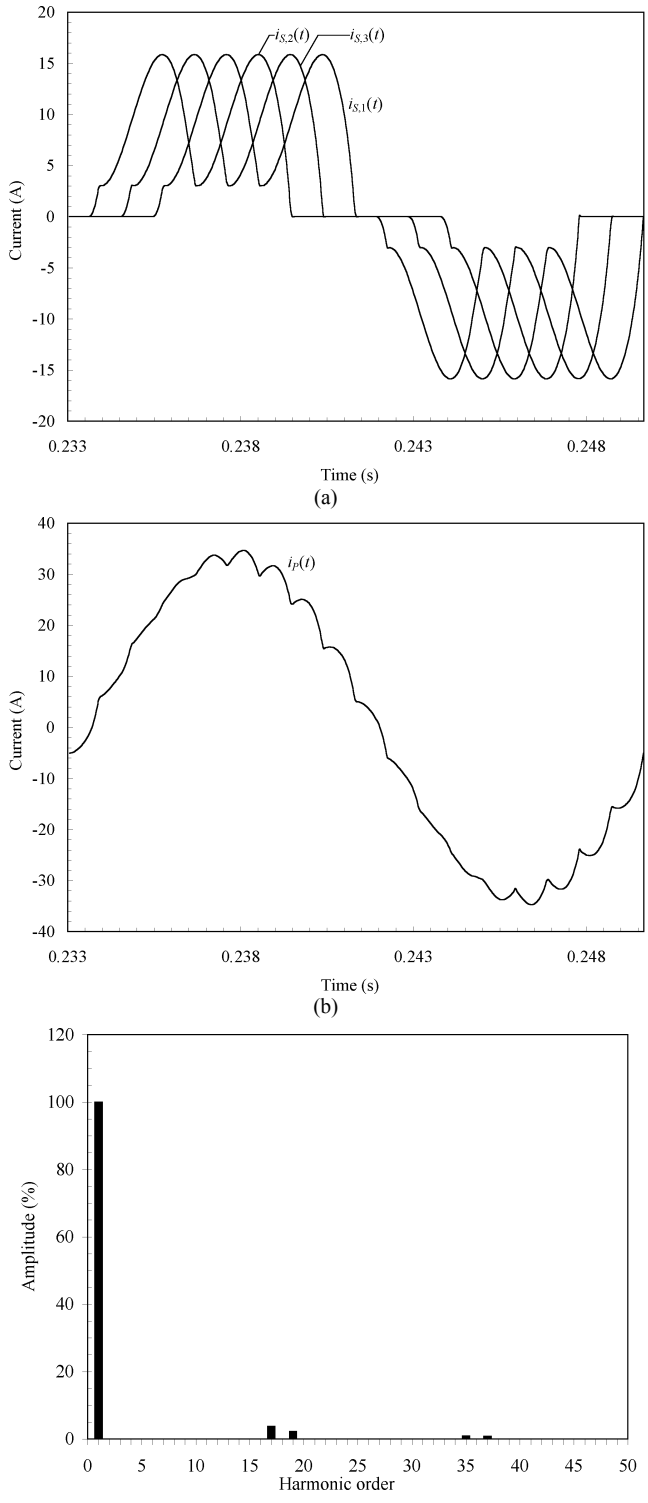

Fig. 8 – Conventional multipulse connection of rectifiers. Reactances and active power levels processed by all rectifiers are equal ($X_{c,j}$ = 0.05 p.u.$_j$, $X_{L,j}$ = 0.02 p.u.$_j$, $V_{S,j}$ = 100 V, $I_{cc,j}$ = 10 A). (a) Secondary line currents. (b) Primary line current. (c) Harmonic spectrum of the primary line current.

On the other hand, Fig. 9 shows simulation results of a multipulse connection with three rectifiers processing distinct active power levels and maintaining the same phase shift among the secondary windings. The harmonics of the primary line current (Fig. 9(b)) are not eliminated, as can be seen from Fig. 9(c), resulting in an input current waveform with a higher THD (10.9%).

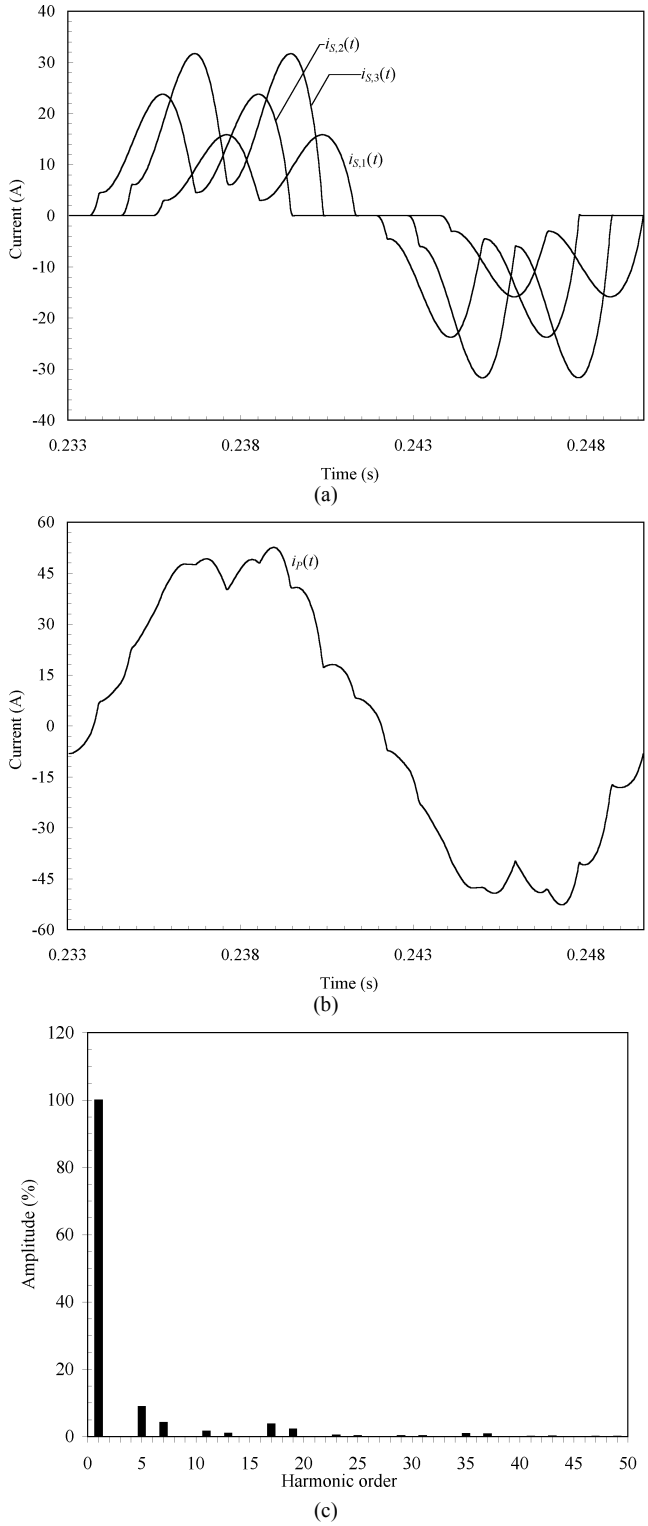

Fig. 9 – Conventional multipulse connection of rectifiers. Rectifiers processing distinct active power levels ($X_{c,j}$ = 0.05 p.u.$_j$, $X_{L,j}$ = 0.02 p.u.$_j$, $V_{S,j}$ = 100V, $I_{cc,1}$ = 10A, $I_{cc,2}$ = 15A, $I_{cc,3}$ = 20A). (a) Secondary line currents. (b) Primary line current. (c) Harmonic spectrum of the primary line current.

Then, it is important to develop a generalized design methodology to compute the phase shift among the secondary windings, mainly considering the active power processed by each rectifier. This methodology is important, for instance, to design the input stage of hybrid multilevel inverters, where each cell usually process a distinct active power level.

V. Multipulse Connection of Rectifiers: Generalized Design Methodology

As fifth harmonic typically presents the highest amplitude, it would be desirable to eliminate this harmonic, even when the rectifiers process distinct active power levels. From (12), the fifth harmonic can be represented as a sum of vectors:

$$I_{5,P}\angle\varphi_{5,P} = \sum_{j=1,2,...}^{n} \frac{V_{S,j}}{V_P} I_{5,j}\angle 6\Phi_j + \varphi_{5,j} \,. \quad (15)$$

Considering that Φ_n = 0º (reference angle), then the fifth harmonic amplitude can be obtained by:

$$I_{5,P} = \sqrt{\left[\frac{V_{S,1}}{V_P} I_{5,1}\cos\left(6\Delta\Phi_1 + \varphi_{5,1}\right) + ... + \frac{V_{S,n}}{V_P} I_{5,n}\cos\left(\varphi_{5,n}\right)\right]^2 + \left[\frac{V_{S,1}}{V_P} I_{5,1}\sin\left(6\Delta\Phi_1 + \varphi_{5,1}\right) + ... + \frac{V_{S,n}}{V_P} I_{5,n}\sin\left(\varphi_{5,n}\right)\right]^2} \quad (16)$$

From (16), it is possible to verify that the fifth harmonic amplitude is a function of these phase angles, that is:

$$I_{5,P} = f\left(\Delta\Phi_1, \Delta\Phi_2, ..., \Delta\Phi_{n-1}\right). \quad (17)$$

Considering that (17) has at least one minimum point, the following conditions must be satisfied to obtain the phase angles that result in a minimum value of $I_{5,P}$ [21]:

$$\frac{\partial f}{\partial \Delta\Phi_1} = \frac{\partial f}{\partial \Delta\Phi_2} = ... = \frac{\partial f}{\partial \Delta\Phi_{n-1}} = 0 \,, \quad (18)$$

$$\frac{\partial^2 f}{\partial \Delta\Phi_1^{\,2}} > 0 \left(\text{or } \frac{\partial^2 f}{\partial \Delta\Phi_2^{\,2}} > 0 \text{ or ... or } \frac{\partial^2 f}{\partial \Delta\Phi_{n-1}^{\,2}} > 0 \right). \quad (19)$$

The global minimum point inside the specified interval ($-\pi/6 \le \Delta\Phi_j \le \pi/6$) presents the second derivative with the highest amplitude among the points that satisfy (18) and (19).

Consequently, from secondary line voltages and from fifth harmonic amplitude and phase of the input current of the six-pulse rectifiers, which can be obtained from Fig. 5 and Fig. 6, it is possible to determine the phase shift among the secondary windings, by using (16), (18) and (19), to minimize or even eliminate the fifth harmonic of the primary line currents.

For instance, Fig. 10 shows the fifth harmonic amplitude of the primary line current by varying the phase angles among the secondary windings of a multipulse connection with three rectifiers processing distinct active power levels and with same normalized impedances. In this case, when the active power processed by the second rectifier is 50% greater than the power of the first cell and the active power processed by the third rectifier is two times greater than the active power of the first rectifier, the fifth harmonic of the primary line current has minimum points when $\Delta\Phi_1$ = -22,24º and $\Delta\Phi_2$ = +25,17º, or $\Delta\Phi_1$ = +22,24º and $\Delta\Phi_2$ = -25,17º. The fifth and seventh current harmonics are cancelled by using these phase angles, as can be verified in Fig. 11(b). Without these harmonics, the THD of the input current shown in Fig. 11(a) is 6.6% while the input current THD using the conventional design methodology (Fig. 9(b)) is 10.9%.

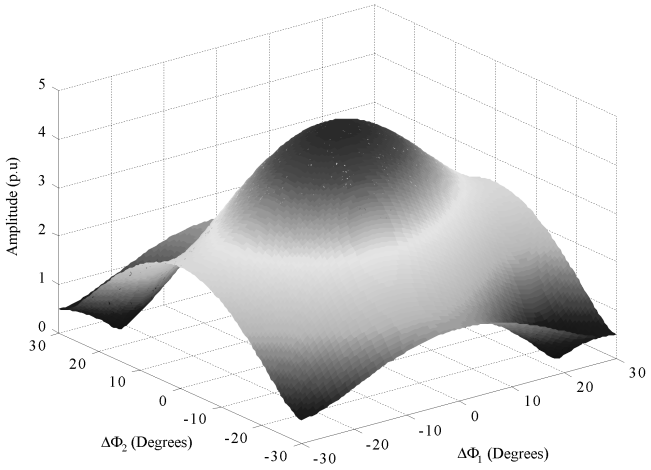

Fig. 10 – Fifth harmonic amplitude of the primary current versus phase angles of the secondary windings. Distinct power levels ($P_2 = 1.5P_1$ and $P_3 = 2P_1$).

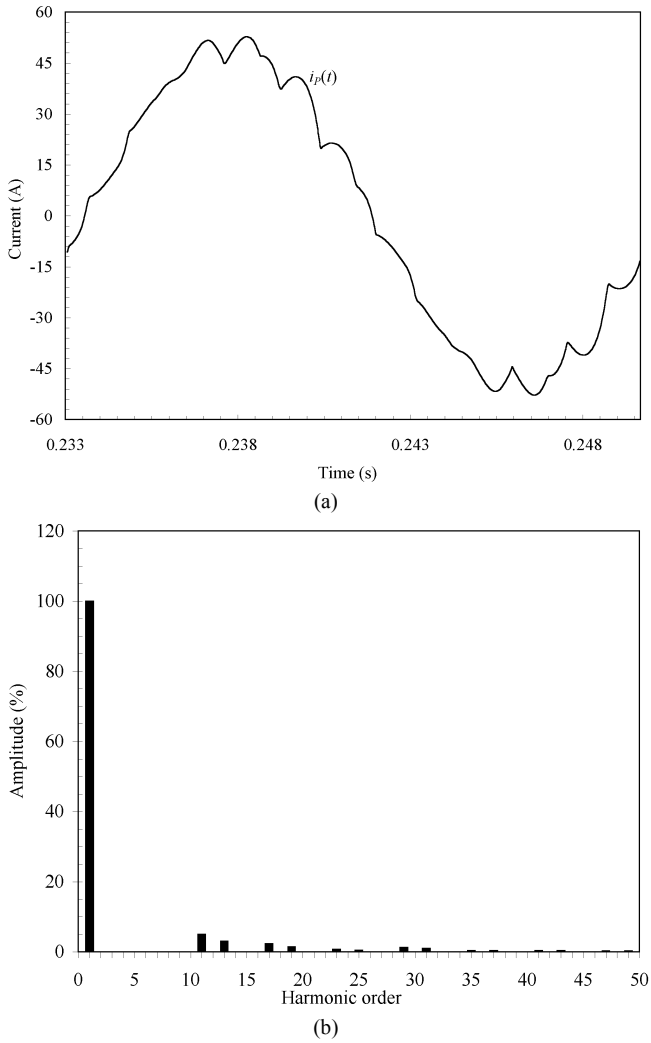

Fig. 11 – Generalized design methodology of the multipulse connection of rectifiers. Distinct active power levels ($X_{c,j}$ = 0.05 p.u.$_j$, $X_{L,j}$ = 0.02 p.u.$_j$, $V_{S,j}$ = 100 V, $I_{cc,1}$ = 10 A, $I_{cc,2}$ = 15 A, $I_{cc,3}$ = 20 A, $\Delta\Phi_1$ = -22.24º and $\Delta\Phi_2$ = +25.17º). (a) Primary line current. (b) Harmonic spectrum.

Due to the fact that the proposed design methodology computes the phase angles among the secondary windings of the isolation transformer even with rectifiers processing distinct active power levels, it can be applied to the input stage of hybrid multilevel inverters.

VI. Multipulse Connection of Uncontrolled Rectifiers Applied to Hybrid Multilevel Converters

The THD of the unfiltered output voltage waveforms can be used to determine the number of levels of a hybrid multilevel inverter. For instance, defining that the THD of the unfiltered line voltage waveform should be less than 5 % for a unitary amplitude modulation index, the multilevel inverter should be able to synthesize voltage waveforms with at least 15 levels [19].

On the other hand, as diode rectifiers do not allow the bi-directional power flow between load and source, the dc voltage sources of the H-bridge cells that compose the hybrid multilevel inverter must be correctly determined so that all cells can not regenerate energy in any operating point.

Table I shows the parameters of a hybrid inverter able to synthesize phase voltages with fifteen distinct levels, resulting in line voltages with THD smaller than 5% for m_a = 1. The normalized values of the dc voltage sources have been obtained from Fig. 3 and, therefore, they can be implemented with diode rectifiers.

TABLE I - PARAMETERS OF A HYBRID MULTILEVEL INVERTER.

Parameter	Value
Number of levels (m)	15
Series-connected H-bridge cells (n)	4
Normalized dc voltage sources (V_j)	V_1 = 1 p.u. V_3 = 2 p.u. V_2 = 1 p.u. V_4 = 3 p.u.
Frequency modulation index (m_f)	61

Fig. 12 presents the fundamental components of the output voltages of the H-bridge cells and it also indicates the fundamental components of these voltages for m_a = 0.9, which has been defined as nominal operating point. As these H-bridge cells are connected in series, the same current flows through them and, therefore, the active power levels processed by these cells have a feature similar to that illustrated in Fig. 12.

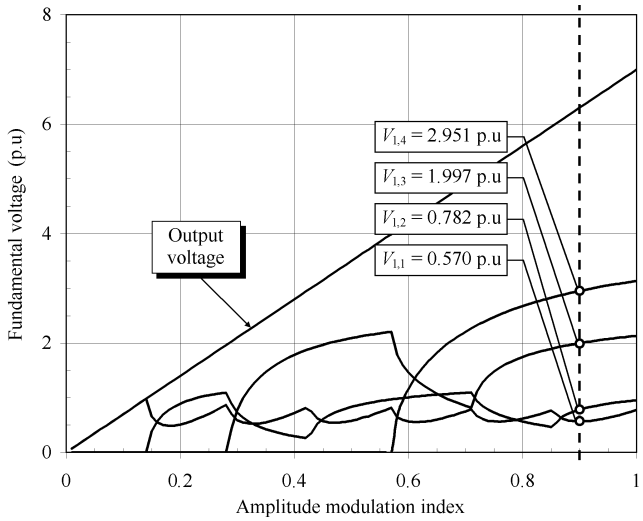

Fig. 12 – Fundamental voltages ($V_1 = V_2$ = 1 p.u., V_3 = 2 p.u., V_4 = 3 p.u.).

From the active power level processed by each H-bridge cell at the nominal operating point and using (16), (18) and (19), it is possible to demonstrate that a set of phase angles among the secondary windings of the isolation transformer that eliminates the fifth harmonic of the primary line current in this operating point is given by: $\Delta\Phi_1$ = +21.53º, $\Delta\Phi_2$ = -23.26º and $\Delta\Phi_3$ = +29,69º.

Fig. 13(a) presents a line current (THD = 7.8%) drawn from utility (V_s = 220 V) in the nominal operating point of a three-phase 4160 V/100 kW (@ m_a = 0.9) hybrid multilevel inverter able to synthesize fifteen distinct voltage levels (Table I). The dc voltage sources of all H-bridge cells are implemented with six-pulse diode rectifiers and the secondary windings are phase-shifted among them with the angles mentioned above. As expected, Fig. 13(b) shows that the fifth harmonic is eliminated by using these phase angles. Moreover, Fig. 14 presents an output phase voltage waveform with fifteen distinct voltage levels at the nominal operating point.

Finally, Fig. 15 presents the THD of a primary line current, using different connections for the input isolation transformer. This figure shows that the input current

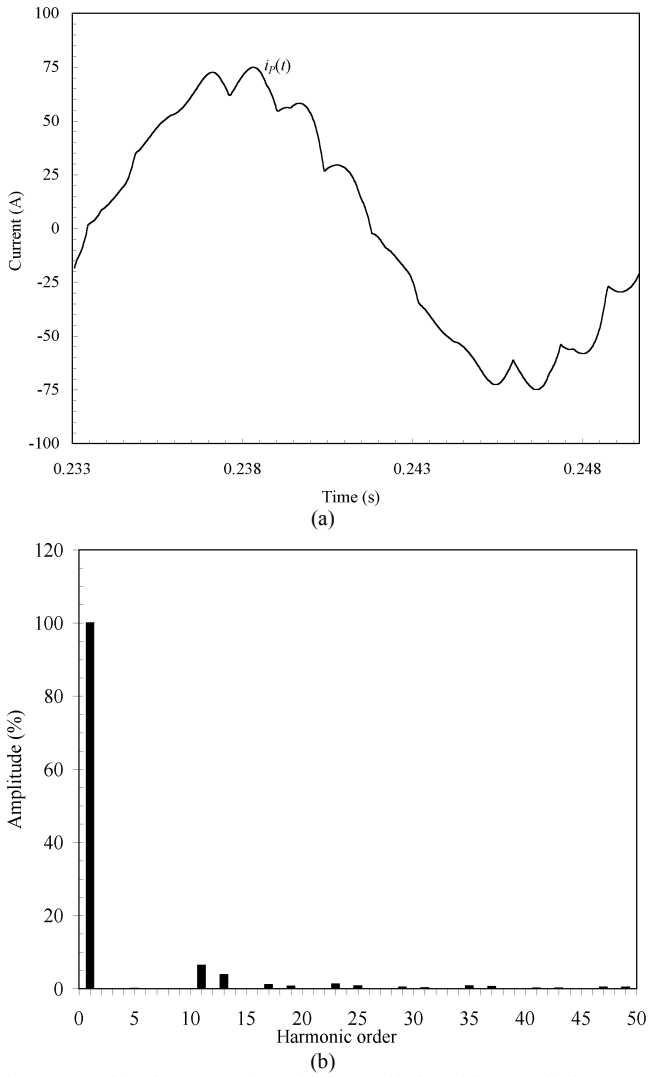

Fig. 13 – Multipulse connection of uncontrolled rectifiers applied to a 15-level hybrid inverter (m_a = 0.9, $X_{c,j}$ = 0.05 p.u.$_j$, $X_{L,j}$ = 0.02 p.u.$_j$, $\Delta\Phi_1$ = 21.53º, $\Delta\Phi_2$ = -23.26º and $\Delta\Phi_3$ = 29.69º). (a) Primary line current. (b) Harmonic spectrum.

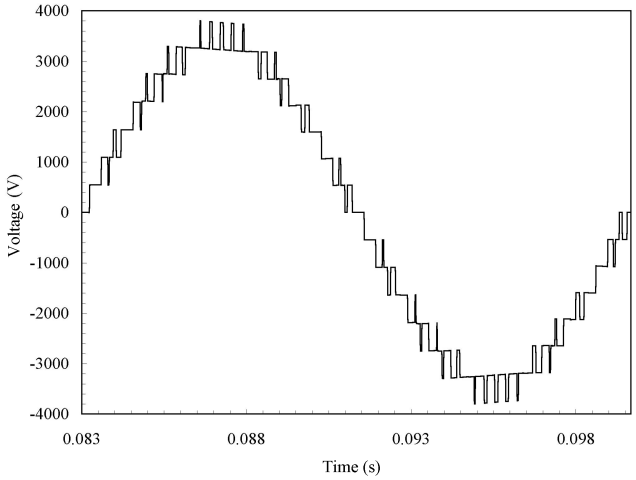

Fig. 14 – Output phase voltage (m_a = 0.9, $X_{c,j}$ = 0.05 p.u.$_j$, $X_{L,j}$ = 0.02 p.u.$_j$, $\Delta\Phi_1$ = 21.53º, $\Delta\Phi_2$ = -23,26º and $\Delta\Phi_3$ = 29.69º).

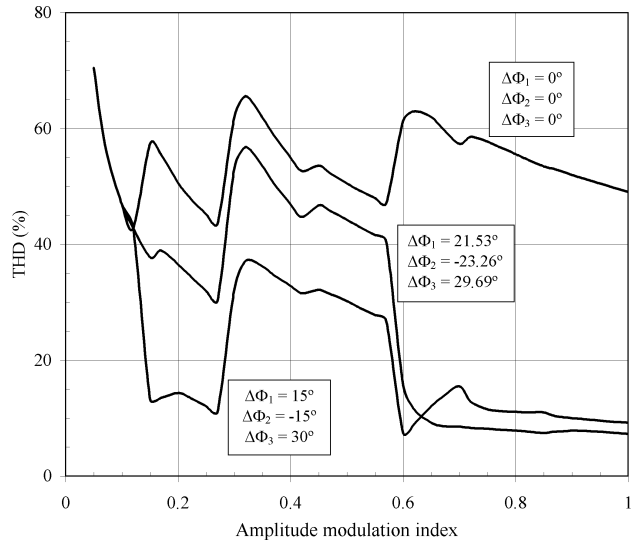

Fig. 15 – Primary line current THD ($X_{c,j}$ = 0.05 p.u.$_j$, $X_{L,j}$ = 0.02 p.u.$_j$).

waveform presented a smaller THD for a wide range around the nominal operating point by using the phase angles computed from the proposed generalized design methodology. However, for low m_a values, the hybrid system presented a better input performance with the phase angles obtained from conventional design methodology, because the ratios among the active power levels processed by the H-bridge cells are not the same for different values of m_a, with the adopted modulation strategy.

VII. CONCLUSIONS

This paper proposed a new generalized design methodology to determine the phase angles of the secondary windings of the input isolation transformer, even when the active power levels processed by each rectifier and/or their impedances are different. Consequently, this generalized design methodology can be employed to design multipulse connection of rectifiers for the input stage of hybrid multilevel inverters, once the series-connected cells usually process distinct active power levels. The phase angles of the secondary windings are obtained to eliminate the fifth harmonic of the input current, once this harmonic component presents an amplitude considerably higher than the amplitudes of the other components. Therefore, the proposed design methodology can be employed to increase the input power factor and to reduce the input current THD.

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