METHODOLOGY FOR OPTIMIZATION OF THE EFFICIENCY IN DC-DC PWM POWER CONVERTERS ACCORDING TO APPLICATION.

Everton Luiz Ferret dos Santos, M.Eng.
João Carlos dos Santos Fagundes, Dr.
Federal University of Santa Catarina – Power Electronics Institute – INEP
P.O Box 5119 – Phone: 55-48-331-9204 – Fax: 55-48-234-5422
e-mail: everton@inep.ufsc.br - 88.040.970 – Florianópolis – SC – Brazil

Abstract – This paper presents a methodology for optimization of DC-DC PWM converters according to its application. The methodology consists in analysis of losses, selection and evaluation of strategies to their minimization and finally choice of the structure to be employed from the analysis concerning efficiency, volume and cost.

KEYWORDS:

Optimization, efficiency, power converters.

I. INTRODUCTION:

The design of electronic power systems requires the application of several distinct acknowledgement areas related to engineering such as electricity, magnetism, thermodynamics and mechanics.

The most common strategy employed by designers establishes a variable set and adopts some simplified analyses. Based on the definition of the problem, as preliminary results are obtained, demanding a reasonable amounts of iterations and time required by the tests of prototypes. The ability and experience may lead to satisfactory results, although they are not often optimized. Therefore, there is the need of studying static power converters with improved efficiency according to application.

A typical design with improved efficiency presents the following advantages:
- It consists in an organized and objective way of analyzing applications;
- It implies the increase of the amount of relevant variables, avoiding simplifications;
- Reduction of the number of experimental tests, built prototypes and production costs;
- Better energetic performance and resulting advantages.

In order to improve the performance of a converter for a given application, the first step consists in determining the power losses in the converter when it operates associated to the load.

After that, the power components responsible for the losses must be aborded so that they can be minimized. This is the main target of the proposed work.

The methodology to be adopted includes the analysis of losses and the definition of adequate strategies to deal with them.

II. METHODOLOGY FOR OPTIMIZATION:

The methodology of optimization consists of the steps described below, and shown in the block diagram presented in fig.1:

1. Preliminary choice of topologies that are prominent solutions according to the operation requirements, which includes the type of load and source, the need of isolation, the load range and the standards to be attended;

2. Choice of power components according to voltage and current requirements, operating frequency and the following criteria:
- conduction losses at 100^{o}C and commutation losses for semiconductors technology;
- geometry, type of material, nature and distribution of conductors for magnetic elements;
- equivalent series resistance will select the filter capacitor;
- thermal design for type and size of heat sinks;

3. Definition of the control strategy, considering the converter as a linearized system around a boundary condition, modeled for small signals. The controller topology is selected to attend requirements such as maximum overshoot, response time and static error, defined by the type and characteristics of the application;

4. Definition of the distribution profile of the power losses according a preliminary design;

5. Selection and evaluation of strategies to minimize losses;

6. Determination of the structure to be employed from the results concerning efficiency, volume and cost;

7. Simulation and evaluation of the relevant results concerning the circuit, so that a prototype is built and experimental results can be obtained.

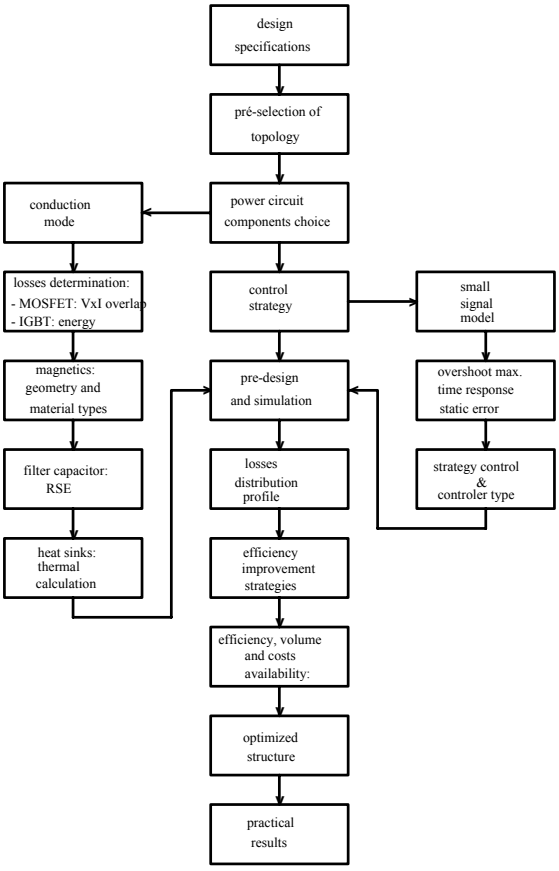

Fig.1: Block diagram of optimization methodology.

III. ANALYSIS OF LOSSES:

Power losses in PWM DC-DC converters can be classified in conduction and switching losses, losses in capacitances and losses in magnetic components.

Conduction losses are caused by resistances and semiconductor voltage drops in current loops, and can be calculated as show in table 1:

Table 1: Conduction losses in semiconductor devices.	
Diodes:	$P_{cdd} = V_f \cdot I_{av} + R_s \cdot I_{rms}^2$ (1)
Mosfets:	$P_{cdm} = R_{dson(Tj)} \cdot {I_{rms}}^2$ (2) $R_{dson(Tj)} = R_{dson(25)} \cdot (1 + 0{,}01 \cdot \alpha)^{(Tj-25)}$ (3)
IGBTs:	$P_{cdi} = V_{ce(sat)} \cdot I_{av}$ (4)

These losses, due to the non-ideal characteristics of the switching devices, are more difficult to calculate than the conduction losses. For acceptable accuracy, waveforms for current and voltage should be measured at turn on and turn off switch stages.

Switching losses are generated during short periods of time, as small amounts of energy. Three major mechanisms that contribute to the switching losses:

- Current voltage overlap at turn on / turn off transition;
- Discharging of capacitance across the switch;
- Reverse recovery process of the diode.

The switching losses are listed in table 2:

Table 2: Switching losses in semiconductor devices.	
Diodes:	$P_{cmd} = \frac{V_{rm} \cdot I_{rm} \cdot t_{rr}}{6} \cdot f$ (5)
Mosfets:	$P_{on} = \frac{V_{dsoff} \cdot I_{don} \cdot (t_{fv} + t_{ri})}{2} \cdot f$ (6) $P_{off} = \frac{V_{dsoff} \cdot I_{don} \cdot (t_{fi} + t_{rv})}{2} \cdot f$ (7)
IGBTs:	$P_{on} = \frac{I_{con} \cdot V_{ceoff} \cdot t_{on}}{2} \cdot f$ (8) $P_{off} = \frac{I_{con} \cdot V_{ceoff} \cdot t_{off12}}{2} \cdot f + \frac{I_{ct} \cdot V_{ceoff} \cdot t_{off23}}{2} \cdot f$

If diode reverse recovery effect is considered, an extra loss in turn on is defined as:

$$P_{rr} = \frac{I_{rm} \cdot V_{dsoff} \cdot t_{rr}}{2} \cdot f \quad (10)$$

In fact, not all of the energy is lost at turn off, a portion is stored in the internal capacitances (C_{oss}, C_{rss}) of the MOSFET, and any stray capacitance on the PCB, as they are charged to out voltage. At turn on, however, this energy is discharged through the closing switch, and dissipated. Normally, when using large MOSFETs, C_{oss} is

predominant, and other capacitances can be neglected. An expression for the energy stored in C_{oss} prior to turn on time is given by:

$$P_{Coss} = \frac{2 \cdot V_{dsoff}{}^2 \cdot C_{oss}}{3} \cdot f \quad (11)$$

It should be noted that manufacturers normally specify C_{oss} at relatively low drain-source voltage, typically at 25 V – 50 V. A correct value for C_{oss} at higher drain-source voltage is given by:

$$C_{oss} = \sqrt{\frac{25}{V_o}} \cdot C_{oss25} \quad (12)$$

If driven from low enough impedance, very little power is dissipated in the MOSFET at turn off, as all available current is used to charge the MOSFET's internal capacitances. Usually a compromise has to be made between turn off rate and EMI.

The alternating component of the current that flows through the series resistance (R_{se}) of the filter capacitors causes joule losses, which can damage the capacitor. The voltage supported by this element is directly proportional to the value of R_{se}. The losses are calculated by the following expression:

$$P_{Co} = R_{se} \cdot I_{rms}^2 \quad (13)$$

The losses in magnetic, neglecting the losses in the dielectric medium, are classified in copper losses and core losses. The copper losses are given by:

$$P_{cb} = \rho_{cb} \cdot V_{cb} \cdot J_{mx}{}^2 \quad (14)$$

The copper resistivity is a function of the temperature and it must be adjusted to the temperature in which the converter operates:

$$\rho_{cb} = \rho_{(20^oC)} \cdot [1 + \kappa \cdot (T_e - 20)] \quad (15)$$

An alternative way to determine the copper losses can be obtained via the product of the equivalent resistance and the square of the maximum rms current:

$$P_{cb} = R_{eq} \cdot I_{rmsmx}{}^2 \quad (16)$$

$$R_{eq} = \frac{4 \cdot \rho_{cb} \cdot n_e \cdot MLT}{n_{ce} \cdot \pi \cdot d_{cemx}{}^2} \quad (17)$$

The equivalent resistance R_{eq} must take in account the skin and proximity effects due to the operation at high frequency.

The core losses are defined by:

$$P_{nu} = V_e \cdot C_m \cdot f_s{}^x \cdot \Delta B_{mx}{}^y \quad (18)$$

The coefficients x and y depend of the magnetic material.

IV. STRATEGIES EMPLOYED IN THE REDUCTION OF LOSSES:

The losses in an converter must be minimized by improving the local performance of components, maintaining or increasing the overall performance. The design specification must be respected, since it is inherent to the type of application.

All the techniques discussed here make use of one of the following basic strategies, or a combination of them:

- reduction of the conduction losses in the switches;
- reduction of commutation losses in the switches;
- reduction of losses in magnetic components;

The losses in conventional power converters are present in several components, e.g., diodes, switches, capacitors and magnetic components. The switches present higher losses, as part of them are due to the reverse recovery of diodes. Therefore the strategies presented in this work will focus mainly on the reduction of switches losses. The reduction of losses in the filter capacitor lies in the search of optimum manufacturing technologies in order to minimize the equivalent series resistance.

The most adequate temperature range for the operation of magnetic components varies from to 60^oC to 100^oC , according to technical specifications. A mean temperature equal to 80^oC will be adopted as default, and the copper resistivity will be adjusted according to this value. The stray range of the magnetic flow is adopted in function of each topology. The core geometry is chose to attend each application adequately. The resistance increases with the frequency in conductors when the skin effect is considered.

1. Reduction of conduction losses in the switches:

The strategies to reduce the conduction losses in switches, available in the literature are as follows:

1.1. Association of circuits and components:

The parallelism of components can be very useful method to reduce losses in converters. Power MOSFETs are particularly adequate to this solution, since that a balanced current sharing is assured in each component. As the losses are divided among several transistors each MOSFET will operate at low junction temperatures, where R_{dson} is consequently reduced. On the other hand, IGBTs are not adequate to the parallelism, because the saturation voltage independs on the current. However, an interesting combination results when IGBTs and MOSFETs are associated. If the MOSFET is turned off immediately after the IGBT, the overshoot voltage over the switch is reduced when the IGBT current tail is flowing, as the commutation losses in the devices are reduced as well.

Diodes present negative temperature coefficients for the direct voltage drop (V_f), what makes the parallelism more difficult than using MOSFETs. A thermal coupling is not obtained, unless the diodes are encapsulated in a single arrangement or over the same heat sink.

Advantages:
Reduced R_{dson} (MOSFET); Improved heat distribution; Lower current ratings for individual devices;
Disadvantages:
High component count; Less compact PCB layout.

1.2. Choice of the most adequate semiconductor:

The main factor responsible for the fast increase of conduction losses in MOSFETs is the resistive characteristic of the device (R_{dson}) , where the losses are proportional to the square of the rms current. On the other hand, an IGBT always exhibits a constant voltage drop ($V_{ce(sat)}$), and the conduction losses are linearly proportional to the rms current. Therefore, IGBTs consist in prominent choices for topologies that operate with high voltage stresses over the switches.

The main disadvantage of such device lies in the long turn-off time, where the characteristic of current tail in the collector increases the commutation losses as well as limits the operating frequency. In order to achieve an optimum overall efficiency IGBTs must be turned off with zero current (ZCS).

Advantages:
Low conduction losses at high current; Low temperature coefficient of $V_{CE(sat)}$; Fast turn-on.
Disadvantages:
Current "tail" causes turn-off losses; Difficult to parallel.

1.3. Reduction of the total voltage drop on semiconductors:

High conduction losses result since there are a considerable number of semiconductors in the current path. In order to reduce such losses, it is necessary to adopt an alternative topology or even limit the operating range to voltage levels that provide low voltage stresses.

Fig.4 shows an alternative topology for the boost converter acting as a pre-regulator circuit with high power factor [9]. This solution has the advantage of presenting only two semiconductors in the current path, propitiating the reduction of conduction losses and the elimination of the use of a rectifier bridge.

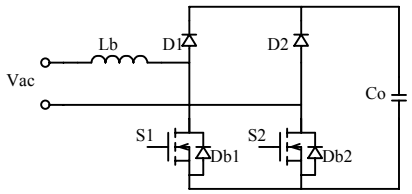

Fig.4: Boost converter by Souza/Barbi.

Advantages:
Only two voltage drops mean less conduction losses; No need of a rectifier bridge.
Disadvantages:
Require twice the number of switches; Risk of common mode disturbances.

1.4. Reduction of commutation losses in the switches:

The strategies for the reduction of the commutation losses in the switches are as follows:

1.4.1. Fast diodes and soft recovery diodes:

The development of the ultra fast diodes is intrinsically related to the use of static converters

in computers and telecommunications. Another preponderant factor is the creation of new topologies that employ very high operating frequencies.
Such devices present reduced commutation periods, i.e., about tens of nanoseconds, causing the commutation losses to be significantly reduced. A comparison between ultra-fast diodes and soft recovery diodes is presented in [10], where the effects of the reverse recovery are emphasized.
Ultra-fast diodes present lower commutation periods than soft recovery diodes, causing the commutation losses to be reduced. However, very low commutation periods imply higher EMI levels.

1.4.2. Passive snubber:

A passive snubber reduces losses when the conduction begins. It consists in a prominent alternative if compared to complex active snubbers. Even though the losses in the capacitances during commutation are not reduced, it still presents a satisfactory cost-benefit ratio when applied to MOSFETs. Therefore the drain-source voltage reaches zero before the drain current starts to flow, reducing I-V overlap. Additionally, the current rate in the diodes is limited, reducing the reverse recovery peak current.

The other components (diode and capacitor) only transfer the stored energy to the output when the switch is turned off. Passive snubbers can reduce the conduction and also reverse recovery losses. Fig.5 shows a typical passive snubber applied to a boost converter.

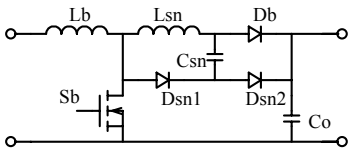

Fig.5: Passive snubber.

where:
L_b: boost inductance;
D_b: boost diode;
S_b: main switch;
L_{sn}: snubber inductance;
C_{sn}: snubber capacitance;
D_{sn1}, D_{sn2}: snubber diodes.

Advantages:
Simplicity and low cost; Reduces the most serious types of switching losses in MOSFETs; Allows correct sizing of the boost diode; Allows higher switching frequency; Reduced EMI.
Disadvantages:
Unable to reduce capacitive switching losses.

1.4.3. Active snubbers:

To reduce even more the commutation losses, several types of active snubbers, which redirect all the energy stored in the elements during switching process, have been presented. They include an auxiliary switch, causing the main switch to conduct under zero voltage and/or current, while the energy stored in the output capacitor is discharged to the load by means of resonance. The switching speed is an important factor to the accurate operation of such circuits. Fig.6 shows an example regarding an active snubber applied to a boost converter too.

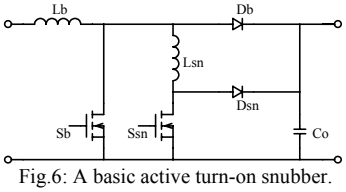

Fig.6: A basic active turn-on snubber.

where:
S_{sn}: snubber active switch;
D_{sn}: snubber diode;
C_o: output converter capacitance.

Advantages:
Reduce all types of switching losses; Allows slower turn-off, reducing EMI.
Disadvantages:
Increase complexity and cost.

1.4.4. Soft commutation:

The methods described previously intend to initially suggest some possibilities to minimize the commutation losses. However, such reduction implies the improvement of the overall efficiency on the converter, and can be performed by the cautions choice of switches, drive circuits and operating frequency, as a compromise among conduction losses, commutation losses and EMI levels is maintained. To reduce commutation losses and EMI levels more effectively, some type of soft commutation technique is need.

Several topologies are used to minimize losses in switches e.g. IGBTs and MOSFETs. The main objectives of soft commutation are:
a. control of the current rate di/dt when conduction starts, in order to reduce reverse recovery diodes;
b. minimization of voltage and current overlap when conduction starts;
c. reduction of losses in the intrinsic capacitances of switches;
d. minimization of voltage and current overlap during turn off process.

For MOSFETs items (a), (b) and (c) are the most important requirements, and for IGBTs item (d) is the main one due to current tail of the collector.

Soft commutation of converters also offers some indirect advantages as the operation in high frequencies and reduction of EMI levels. Higher operating frequencies imply the reduction of magnetic and capacitors volume, what increases the power density and dynamic response of the converter. However it may cause the losses in core and the losses in transformers and inductors to increase.

V. CONCLUSIONS:

A study concerning the nature of losses and PWM DC-DC converters as well as a design procedure have been presented in order to improve converter efficiency. From a set of specifications and restrictions imposed by application the power and control circuits are implemented, and thermal design is performed. If the profile of the power losses distribution is defined, some strategies can be used to increase the efficiency of the converter since the overall performance is not affected.

The strategies discussed previously include the correct choice of the switch according to its characteristics, the association of components or even circuits and the use of auxiliary commutation circuits.

The chosen topology will attend the efficiency, volume and cost requirements quite satisfactorily according to each type of application.

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