THREE LEVEL 24 KW 35 KHZ DC-DC CONVERTER FOR TELECOMMUNICATIONS

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***Abstract* – This paper shows a high frequency, high output power DC to DC converter designed to operate as part of a telecommunication supply system. Three level modulation technique was chosen due to high input voltage. Soft switching provided the improved efficiency of the converter. Experimental results taken from a lab model are presented.**

KEYWORDS

DC-DC Converter, Three Level, High Power, Efficiency.

I. INTRODUCTION

The proposed three-level DC-DC converter is the output stage of a three-phase power supply for telecommunications applications comprising the following specifications:

- Output voltage Vo=60V;
- Output current Io=400A;
- Output power Po=24 kW;
- Efficiency η=0.96;
- Switching frequency fs=35 kHz;
- Input voltage Vi=900V.

The features of the converter are as follows:

• Regulated output DC voltage;
• Unidirectional power flow;
• High reliability;
• High efficiency;
• Low cost;
• Galvanic isolation;
• Simple modulation, control and switching strategies;
• Short circuit and overload protection;
• Output inductor/capacitor filter.

Different topologies can be used as a solution. However, for high input voltage applications, the three level topologies are more indicated because the voltage across the switches is half of the DC bus voltage.

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II. PROPOSED CONVERTER

Figure 1 shows the proposed converter. It is a half bridge topology based on the Neutral Point Clamped - NPC cell and the Floating Capacitor – FC [1], [2], [3], [4], [5] and [6]. Advantages of both topologies are present as excellent voltage split and simple modulation applied to a high power density and high frequency requirements.

Switches S_1, S_2, S_3 and S_4 are the main commutation cell. The anti-parallel diodes D_1, D_2, D_3, and D_4 conduct the reverse current and clamp the reverse voltage across the switches. Diodes D_5 and D_6 are responsible to clamp the voltages across the switches on Vi/2.

Capacitor Cb blocks DC current on the primary of the transformer. Capacitor Cc helps to equalize voltage across switches improving the three level modulation. The inductor Lr and the capacitors C_1, C_2, C_3 and C_4 provide the ZVS turn on of the switches. These capacitors also control the voltage slope during turn off. The switching characteristics make this topology very efficient.

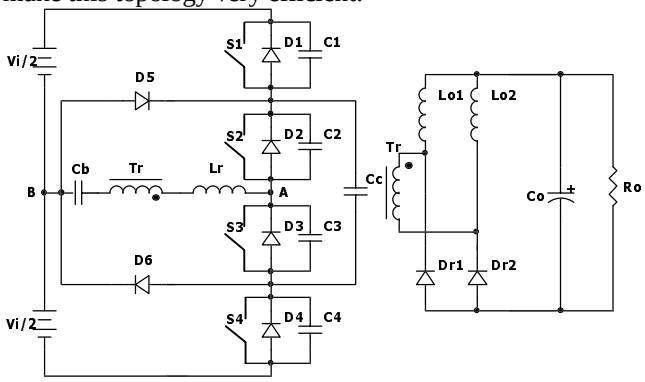

Fig. 1 – Three level converter that was the base for the generation topology.

The transformer T_r provides insulation and adapts voltage level between input and output.

References [7] and [8] propose an alternative output rectifier called *"Hybridge"*; it presents better efficiency and allows clamping reverse voltage in a simpler way. The circuit is obtained from a full bridge rectifier by replacing

the upper diodes for inductors of the output filter. The main characteristic of this structure is the reduction of the current through secondary windings.

Figure 2 shows the simplified waveforms of the steady state operation.

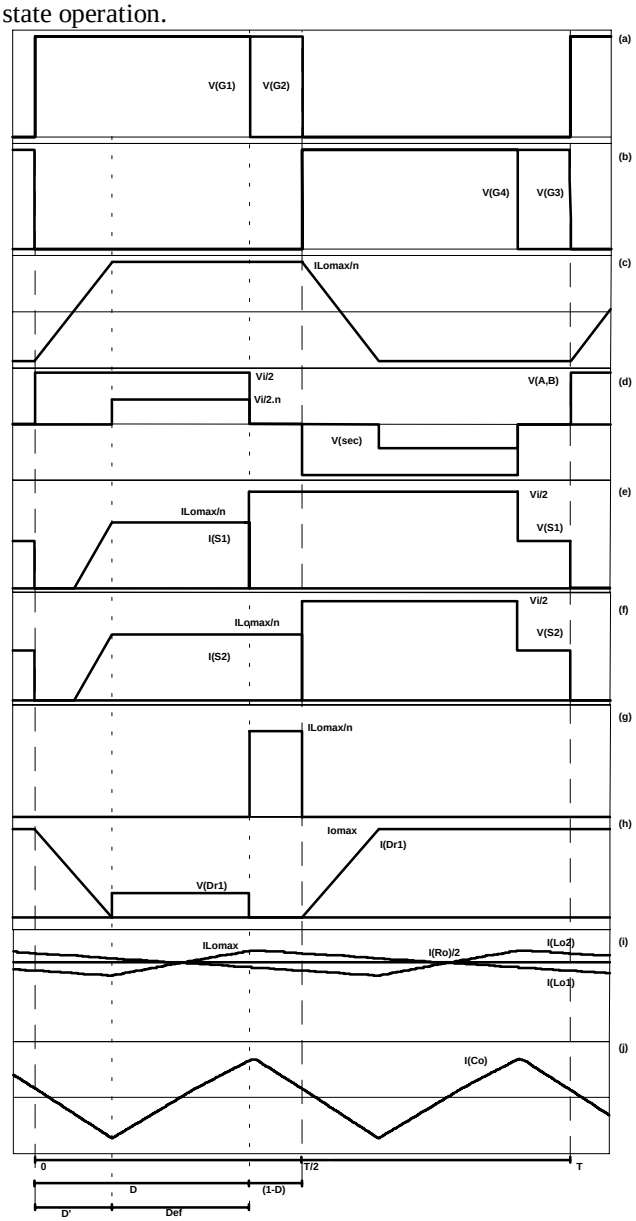

Fig. 2 – Simplified waveforms: (a) command S_1 and S_2; (b) command S_3 and S_4; (c) current through L_r; (d) voltage across A and B and secondary voltage; (e) voltage and current through S_1; (f) voltage and current through S_2; (g) current through D_5; (h) voltage and current through Dr_1; (i) current through L_{o1} and L_{o2} and load current; (j) current through C_o.

Output voltage is determined by expression (1).

$$Vo = \frac{Vi}{2 \cdot n} \cdot Def \quad (1)$$

During the time interval Δt, that is related to the lost of duty-cycle, the voltage across the resonant inductor is Vi/2 and its current range is from –Io/n to +Io/n. This way, the lost of duty-cycle is defined by equation (2), in seconds, or by expression (3), in percentage.

$$\Delta t = Lr \cdot \frac{2 \cdot Io/n}{Vi/2} \quad (2)$$

$$D' = \frac{\Delta t}{T/2} = Lr \cdot \frac{2 \cdot Io/n}{Vi/2 \cdot T/2} \quad (3)$$

Effective duty-cycle of the converter is defined by equation (4) and the output voltage is defined by equation (5).

$$Def = D - D' = D - Lr \cdot \frac{2 \cdot Io/n}{Vi/2 \cdot T/2} \quad (4)$$

$$Vo = \frac{Vi}{2 \cdot n} \cdot \left(D - Lr \cdot \frac{2 \cdot Io/n}{Vi/2 \cdot T/2} \right) \quad (5)$$

Equation (5) allows us to trace the output characteristics of the converter. Figure 3 presents this curve to constant V_i, L_r and T, normalized in function of the duty-cycle D.

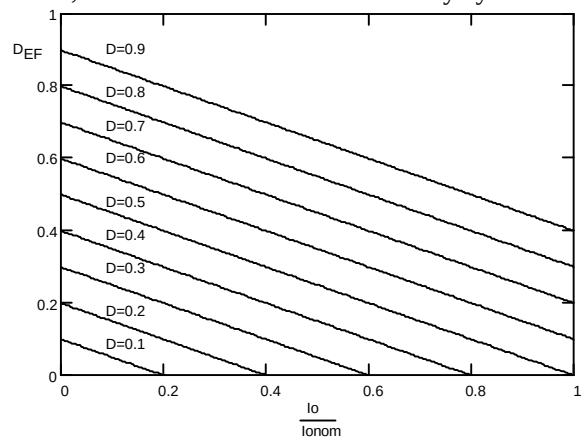

Fig. 3 – Output characteristics.

Table 1 presents current and voltage stress on semiconductors. The currents appear normalized to load current.

Table 1 – Current and voltage stresses.

Component	S_1, S_4	S_2, S_3	D_5, D_6	D_{R1}, D_{R2}
Maximum Voltage	$Vi/2$	$Vi/2$	$Vi/2$	Vsec
Normalized RMS Current	$\sqrt{\frac{1}{2} - \frac{5}{6} \cdot D'}$	$\sqrt{D - \frac{5}{6} \cdot D'}$	—	—
Normalized Average Current	—	—	$1/2 - D$	$1/2$

In the expressions of Table 1, D represents the duty-cycle and D' the duty-cycle reduction due to reactive flow imposed by soft switching. Equation (3) defines D' in function of the switching frequency, resonant inductance, load current and input voltage. Expression (6) defines the minimum load where soft switching is present.

$$Io_{min} = \frac{Vi}{2} \cdot \sqrt{\frac{1{,}5 \cdot C}{Lr}} \quad (6)$$

Where:

$C = C_1 = C_2 = C_3 = C_4$.

In order to achieve a wide range of soft commutation, the value of L_r must be as large as possible. However, as greater the value of L_r, greater will be the value of D' and lower will be the effective duty-cycle of the converter. This way, a successful design must reduce soft commutation in liter loads, where losses are smaller, in order to optimize efficiency at nominal load.

III. EXPERIMENTAL RESULTS

The final power circuit is shown in Figure 4.

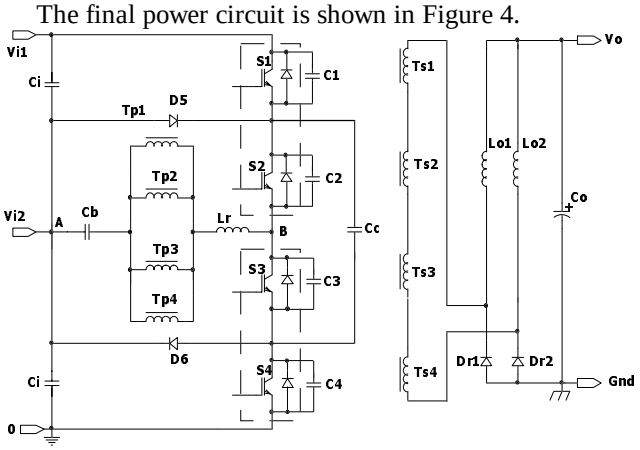

Fig. 4 – Power schematic of the NPC-ZVS-PWM converter.

Several components are connected in parallel due to the power level:

- Blocking capacitor C_b is composed of 12 polypropylene capacitors in parallel;
- Switching capacitors C_1, C_2, C_3 and C_4 were implemented with 3 polypropylene capacitors in parallel;
- Output capacitor is composed by a bank of 6 electrolytic capacitors due to the reduced series equivalent resistance that is needed to achieve the output voltage ripple;
- The transformer was built with 4 smaller transformers. Primary windings are connected in parallel and secondary windings are connected in series to ensure appropriate power splitting;
- Two power switches modules were connected in parallel to improve power dissipation and system reliability;
- Clamping diodes D_5 and D_6 are intrinsic diodes of modules. It is not a mandatory condition, but it was used to easy mechanical assembly;
- Capacitors C_i were implemented to eliminate parasitic inductances in the connecting cables. They are not part of the topology.

Experimental results were obtained from 900V input and 60V output. The output power was 24 kW and the converter was operating at closed loop control.

Figures 5 until 10 show the main waveforms of the converter. Figures 5 and 6 show the voltage across switches S1/S2 and current through the resonant inductor when the converter is delivering zero amps and 400 amps respectively. Voltage across switches is an important parameter to evaluate the secure operation of the converter.

Figure 7 shows the voltage across points A and B and the current through resonant inductor Lr. Notice that the converter is operating near to maximum duty-cycle.

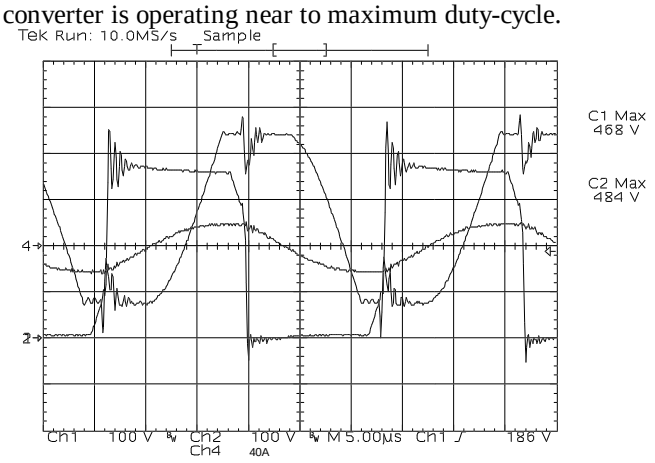

Fig. 5 – Voltages across S1 and S2 and current through L_r at no load condition.

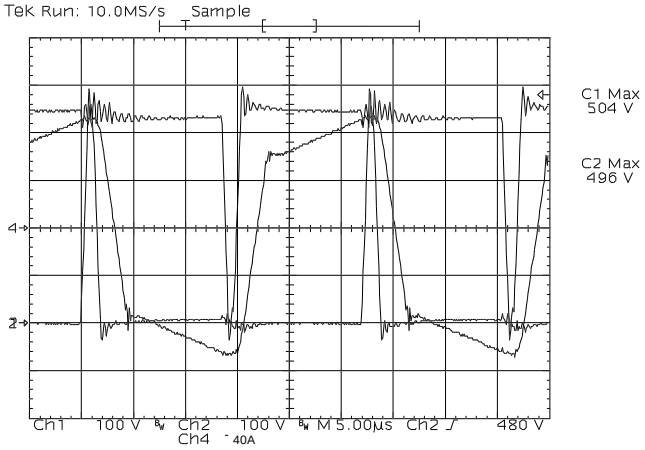

Fig. 6 – Voltages across S1 and S2 and current through L_r at full load condition.

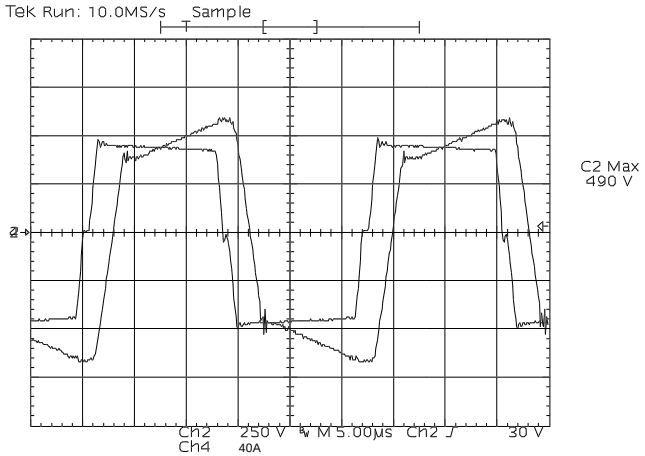

Fig. 7 – Voltage VAB and current through L_r.

Figure 8 presents the output voltage (60V) and current (400A) at full load condition. Figure 9 shows output voltage ripple that is in the specification range.

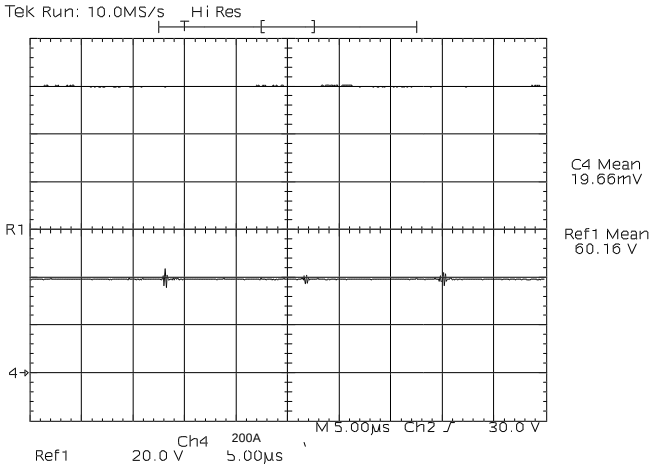

Fig. 8 – Output Voltage and output current at nominal load condition.

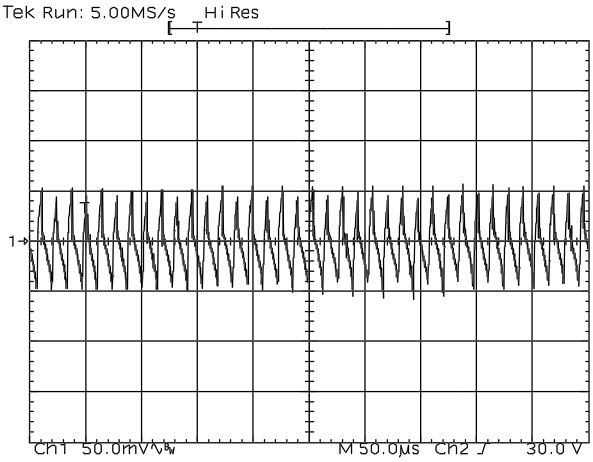

Fig. 9 – Output voltage ripple.

Figure 10 presents the experimental efficiency curve obtained from the prototype. The input and output power were measured during half an hour in each measurement point to ensure steady state operation. Peak efficiency reached 97.2% and nominal efficiency above 96% was achieved. Auxiliary power supply, fans and clamping circuit were turned on during the test. Final lab model is presented in Fig. 11.

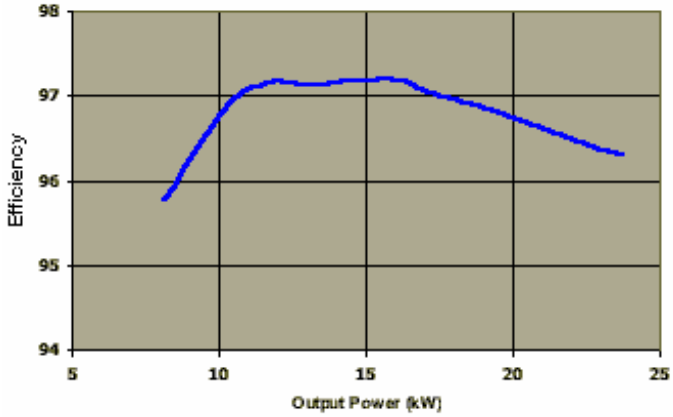

Fig. 10 – Efficiency curve.

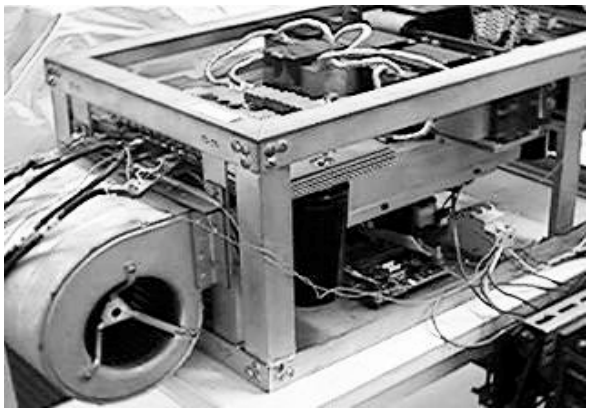

Fig. 11 – Final prototype.

IV. CONCLUSIONS

This paper presents the topology used in a 24 kW 35 kHz DC-DC Converter applied to a telecommunication rectifier. Due to the high input voltage, a three level topology was chosen. Nominal power was achieved with high efficiency due to the use of ultra fast IGBTs. Experimental results taken from a lab model proves the viability of the concept.

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