

Simulation study of a low-cost series compensator for voltage sags, harmonics and unbalances applied to a practical system

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Abstract – In this paper a low-cost Dynamic Voltage Restorer (DVR) is introduced. Its major objective is to deliver, to a sensitive load, three-phase sinusoidal balanced and regulated voltages, even under voltage sags, harmonics and unbalances. In order to validate the developed DVR, it is necessary to study its performance when operating in a practical power utility distribution system. In this paper, a simulation study using the Saber simulator is presented, showing the DVR dynamics in the presence of a three/single-phase short-circuit faults on a practical distribution system.

KEYWORDS

DVR, voltage sag, custom power, power utility distribution system, short-circuit fault, power quality.

I. INTRODUCTION

The concept of Custom Power has been familiar to industry experts since the beginning of the last decade, when the industrial and commercial customers of utilities have reported a rising tide of misadventures related to power quality. In this context the reliability concept have been changed in terms of short interruptions and voltage sags, among others aspects. Voltage sags are said harmful to critical loads and should be compensated in order to supply regulated voltage to such loads. The dynamic voltage restorer (DVR) [1], represents a good choice to overcome such problems. By using this device it is possible to compensate voltage sags, harmonics and unbalances, in such way that the voltages delivered to the critical load are sinusoidal balanced and regulated.

A DVR is a system composed of a converter, a dc storage capacitor, and a transformer connected in series with a

distribution bus-bar, which compensates for voltage disturbances on the bus-bar.

The DVR presented is an improved version of the DVR proposed in [2], adding the harmonic and unbalance active compensations feature to the original project, as suggested by the authors.

It is important to clarify that this particular implementation of a DVR was done under certain costs restrictions. So, achieving a low cost configuration was a main concern of this project.

The final goal is the implementation of a prototype based on the proposed DVR, focused on a distribution system operation.

II. THE DVR CIRCUIT AND ITS OPERATION

The block diagram of the proposed DVR is presented in Fig. 1. Its principle of operation is based on the compensation of the positive-sequence voltage drop caused by the occurrence of voltage sags, as at the start up of huge induction motors, line short-circuits, etc. Its improved control strategy also guarantees compensation for unbalances and harmonics, as will be presented.

The power circuit is composed by a three-phase diode full-bridge rectifier with a large value ac-side inductance, a DC capacitor, a SPWM three-phase voltage-source inverter, a series transformer and a RLC low-pass filter.

The control strategy executed by the digital signal processor (DSP) in Fig. 1, measures the three-phase voltages of the in-bus v_{in}^{abc} and the out-bus v_{out}^{abc} , and gives six digital-control signals that will command the three-phase inverter. The control circuit used in this DVR is shown in Fig. 2 and most of its components are well discussed in [3].

The following definitions are used in the explanation of the control circuit:

- $v_{in}^a, v_{in}^b, v_{in}^c$ – DVR's in-bus voltages.
- v_{as}, v_{bs}, v_{cs} – positive sequence components of voltages $v_{in}^a, v_{in}^b, v_{in}^c$.
- $v_{out}^a, v_{out}^b, v_{out}^c$ – DVR's out-bus voltages (critical load).
- v_{ha}, v_{hb}, v_{hc} – DVR's in-bus voltages without its positive sequence components. So, they are the harmonic and unbalanced components of the in-bus voltages.
- v_{as}, v_{bs}, v_{cs} – unit-value rms voltages synchronized with

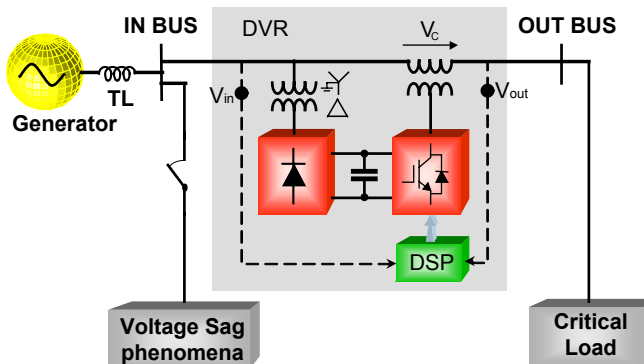


Fig. 1: DVR unifilar block diagram.

the in-bus positive sequence voltages components.

- $v_{asc}, v_{bsc}, v_{csc}$ – control signals for voltage sag compensation.
- $v_{*ac}, v_{*bc}, v_{*cc}$ – control signals for voltage sag, unbalance and harmonic compensation.
- v_{fa}, v_{fb}, v_{fc} – voltages in the terminals of the DVR's series transformer, that were generated by the inverter.

Resuming the control operation, when the voltage-sags, harmonics or unbalances disturbances are detected, the control circuit calculates the compensation signals that the inverter uses as reference to produce the compensation voltages to be added to the in-bus voltages v_{in}^{abc} , by means of a series transformer, that will result in a three-phase constant-rms voltage (v_{out}^{abc}) without harmonics and unbalances applied to the critical load at the out-bus.

The control strategy has three major parts. The first one is the algorithm based on the instantaneous power theory (*pq Theory*), to deal with harmonics and/or unbalances of the measured voltages. The second is a control algorithm in order to compensate voltage sags. The last one is the improved sine PWM (SPWM) technique to synthesize the compensation voltages. All the control operations are based on the measured signals in per-unit (*pu*) of the system bases.

A. The harmonics and unbalances compensation algorithm

Any voltage of a three-phase system can be expressed according to equation (1), derive for phase A only. Its first term represents the fundamental positive sequence component, defining the voltage equation (2). The others terms define the voltage equation (3), and represent the unbalances (negative and zero sequences) and harmonics components.

$$v_{in}^a = \sqrt{2}V_+ \sin(\omega\omega t + \phi_+) + \sqrt{2}V_- \sin(\omega\omega t + \phi_-) + \sqrt{2}V_0 \sin(\omega\omega t + \phi_0) + \sum \sqrt{2}V_{ah} \sin(\omega_h t + \phi_h) \quad (1)$$

$$v_a' = \sqrt{2}V_+ \sin(\omega t + \phi_+) \quad (2)$$

$$v_{ha}' = \sqrt{2}V_- \sin(\omega t + \phi_-) + \sqrt{2}V_0 \sin(\omega t + \phi_0) + \sum \sqrt{2}V_{ah} \sin(\omega_h t + \phi_h) \quad (3)$$

In order to compensate the undesirable harmonics and/or unbalances, this algorithm uses a positive sequence detector, detailed in [3] and [2], to extracts the voltages v_a', v_b', v_c' from the measured voltages $v_{in}^a, v_{in}^b, v_{in}^c$, respectively. Therefore, the differences between them are the voltages $v_{ha}', v_{hb}', v_{hc}'$, which represents the harmonics and unbalances components of the voltages in the in-bus. Thus, the control signals needed to compensate these disturbances must be the opposite of the voltages $v_{ha}', v_{hb}', v_{hc}'$, and it is why they are subtracted from the voltage sags compensation signals.

B. The voltage sag compensation algorithm

This algorithm ensures that the positive sequence components of the voltages $v_{out}^a, v_{out}^b, v_{out}^c$, applied to the critical load, will be at their rated values.

First, the control voltages v_{as}, v_{bs}, v_{cs} are generated by the “Sin Generator” block. These control signals are pure sinusoidal waves, in phase with the in-bus fundamental positive-sequence voltage. To synthesize such signals, the use of a robust synchronizing algorithm is necessary. A phased locked loop (PLL) algorithm tracks, continuously, the frequency of the in-bus fundamental positive-sequence voltage. The design of the PLL allows proper operation

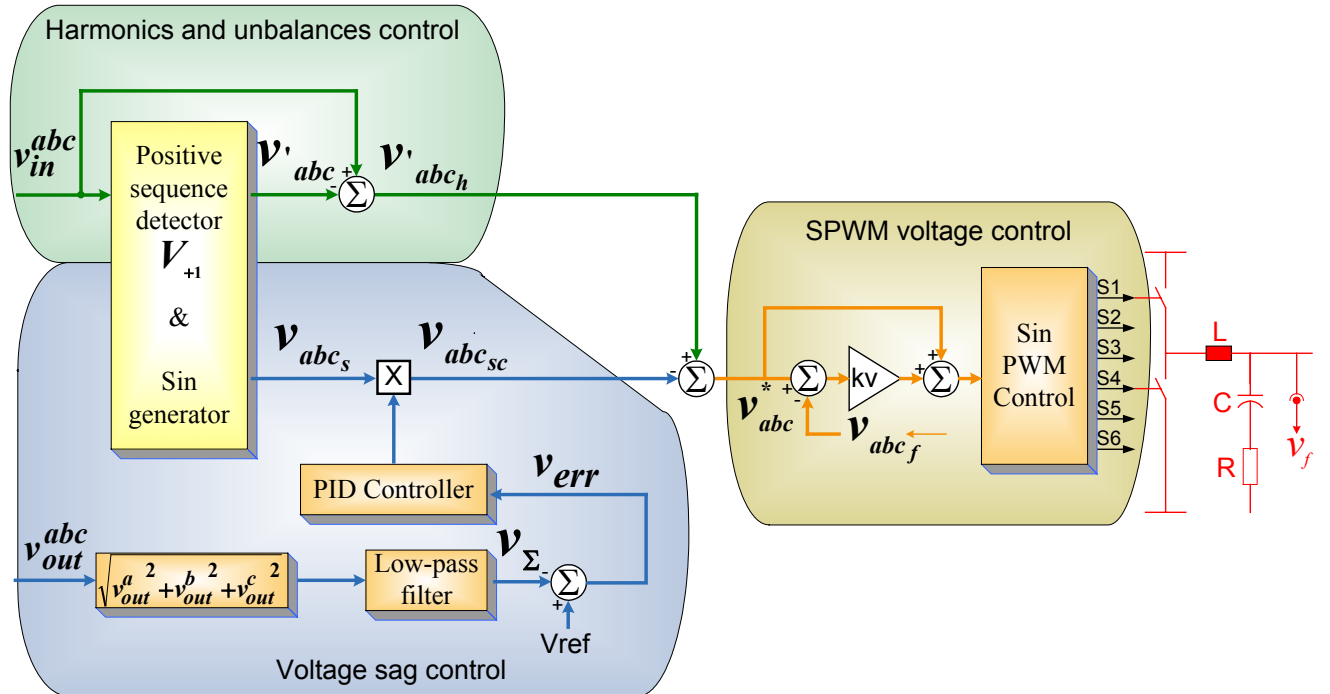


Fig. 2: Unifilar diagram of the control algorithm.

under high distorted and unbalanced system voltages. This PLL is also used by the positive sequence detector module of the previous algorithm, and is explained in [3] and [2].

The next step, and the goal of this algorithm, is to find the amplitude value for v_{as} , v_{bs} , v_{cs} to form the reference signal needed to compensate the voltage sag.

To understand how this amplitude signal is obtained, it is important to notice that the previous control block has already filtered the harmonics and unbalances present in the out-bus voltages, leaving only the fundamental positive-sequence component. So, the concept of the aggregate voltage calculation, defined by the equation (4), applied in these specific voltages, gives its representative three-phase line voltage rms value. An important feature of this definition is that it only needs the instantaneous value of those voltages.

$$v_{\Sigma} = \sqrt{v_{aout}^2 + v_{bout}^2 + v_{cout}^2} \quad (4)$$

By multiplying the aggregate voltage (v_{Σ}) by $\sqrt{\frac{2}{3}}$ gives the amplitude of the out-bus phase-voltages v_{out}^a , v_{out}^b , v_{out}^c . Then, this amplitude signal is compared with the reference of 1 pu giving an error signal which is used as the input of the PID controller, which produces the amplitude modulation index for the sinusoidal voltages v_{as} , v_{bs} , v_{cs} , synthesizing the voltage-sag compensation signals. The parameters of the PID controller, were defined by applying the method proposed in [6].

C. SPWM voltage control algorithm

The conventional Sine PWM (SPWM) techniques are based on the comparison between the control signal and a triangular waveform. The frequency of the triangular waveform establishes the inverter switching frequency and

generally is kept constant along with its amplitude [5].

In this work, the algorithm used to control the inverter is based on an improved Sine PWM voltage control technique proposed in [3], which intends to minimize the deviation between the reference value and the actual value in the terminals of the series transformer, caused by the power low-pass RLC filter in the output of the inverter.

III. PROPOSED DVR PERFORMANCE: MODELLING AND SIMULATION

Before the construction of a DVR prototype to operate in a distribution system, it is necessary to study the performance of the developed DVR in such environment, in order to validate its operation. For that, an already studied practical distribution system, presented in [4], was modeled in the Saber simulator.

The practical system layout is presented in Fig. 3. The following main values, retrieved from [4], were assumed:

1. network primary voltage (HV side): 32 kV - 50 Hz, with a short circuit power of 2400 MVA, secondary voltage (MV side) 20 kV, insulated neutral;
2. main transformer: 132/20 kV, 40 MVA, short circuit voltage $U_{cc} = 13\%$, copper losses 0.6%;
3. nine departing lines: rated power of 5 MVA and 10 km length each line (parameters: series resistance 0.224 Ω /km, series inductance 1.13 mH/km, capacity 10.3 nF/km);
4. actual load of the lines: 4.4 MW and 2.3 MVAR (PF 0.88) each.

One of the nine loads is classified as critical and is intended to be protected by the serial DVR proposed.

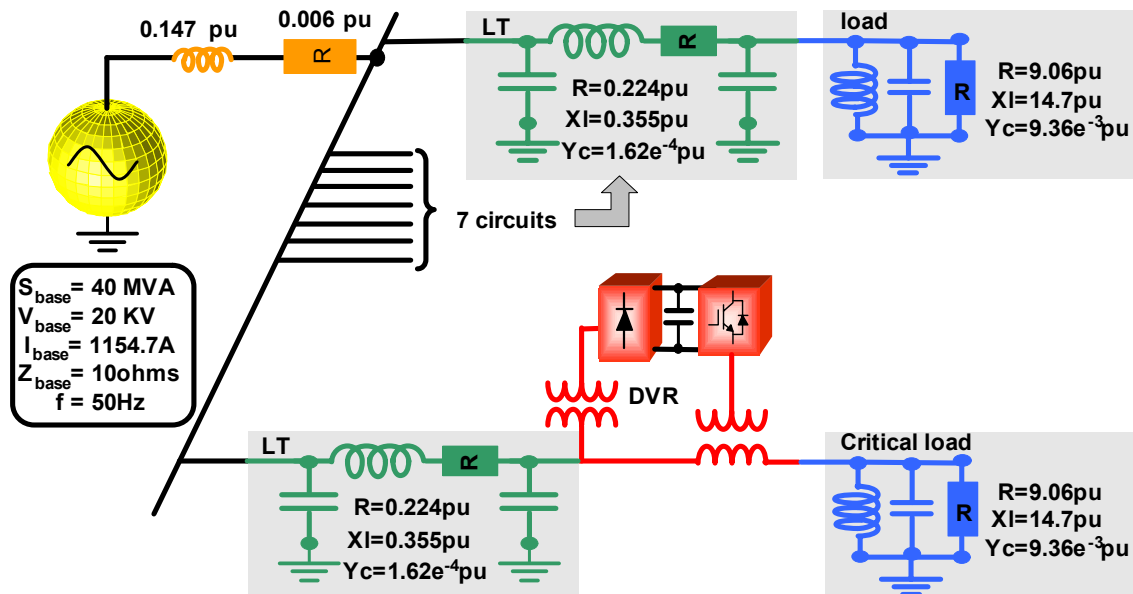


Fig. 3: Practical system unifilar diagram.

A. Three-phase short-circuit simulation

A three-phase short-circuit is a possible fault that can occur in a distribution system, producing voltage sags in neighbor lines [7].

The purpose of this simulation is to study the behavior of the DVR when a three-phase short-circuit occurs in some point of one of the eight neighbors lines of the system.

The practical case-study system was implemented in Saber simulator. At 1.4 s, a three-phase short-circuit was applied in the first line, not protected by the DVR. The fault is located 40% far from the load. The short-circuit has a 1.5Ω resistance and a duration of 300 ms.

First, the system was simulated without the presence of the DVR. The Fig. 4 shows the load voltages of the neighboring lines, including the critical load, before and after the short-circuit occurrence. The graphics shows a balanced three-

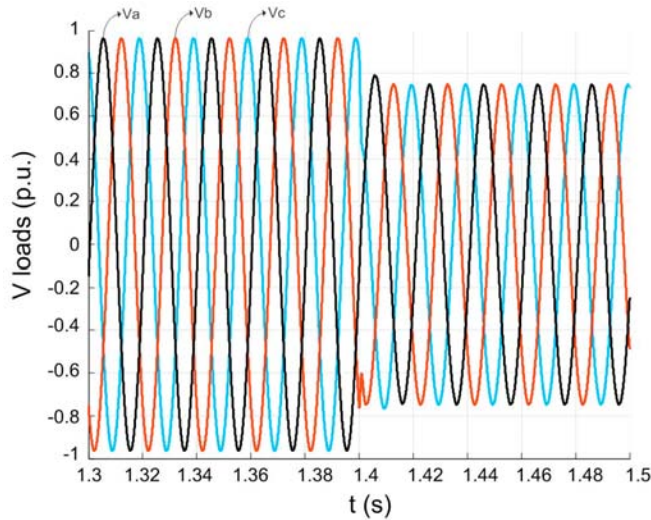


Fig. 4: Loads voltages without the DVR. (three-phase short-circuit study)

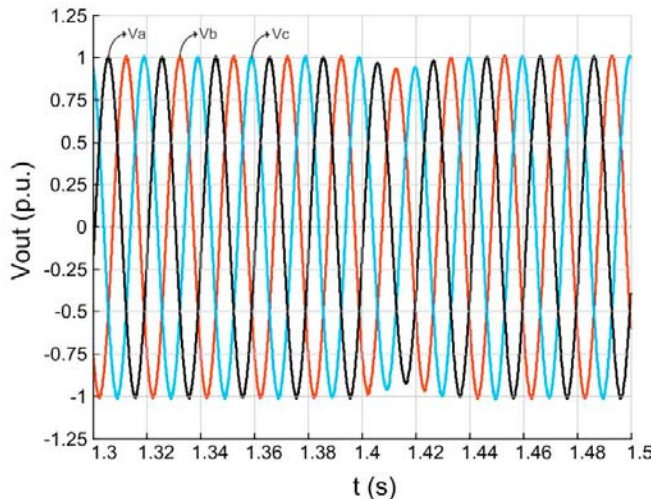


Fig. 5: Critical load voltages protected by the DVR. (three-phase short-circuit study)

phase 0.95 pu load voltage, before the short-circuit, due the three-phase voltages of 1.1 pu generated by the three-phase source (generator) of the system. After the short-circuit, the load voltages suffers a voltage sag of, approximately, 25% in respect to the reference of 1 pu.

In the second simulation, the DVR was introduced in series with the critical load. Fig. 5 shows the critical load voltages, before and after the short-circuit. When the DVR turns on, its dynamic compensates the system's intrinsic voltage drop of 0.05 pu, rising the critical load voltage to 1 pu. This situation is observed until the short-circuit occurrence, when the DVR compensates a 0.27 pu voltage sag in 1.5 cycles. This compensated voltage supplies the critical load with a total harmonic distortion (THD) of 1.4%.

The DVR's rectifier introduces large amount of harmonic currents in the feeder in which is connected. Due the line's impedance, these harmonic currents introduces harmonic voltages in the in-bus voltages (v_{in}^{abc}), as is shown in Fig. 6. The THD of these voltages are 25%.

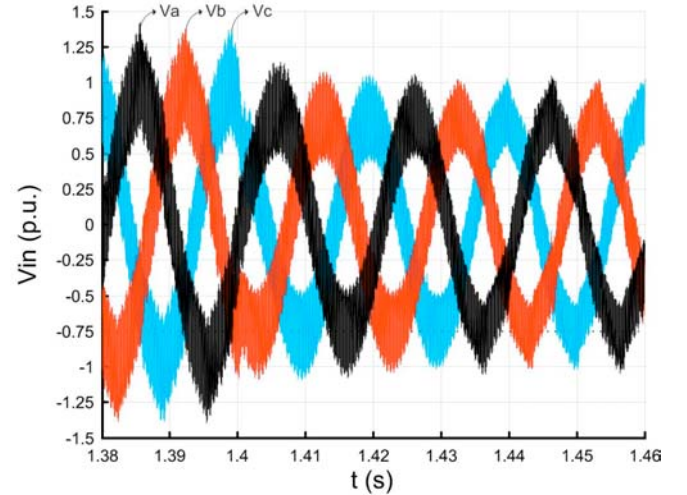


Fig. 6: In-bus voltages of DVR. (three-phase short-circuit study)

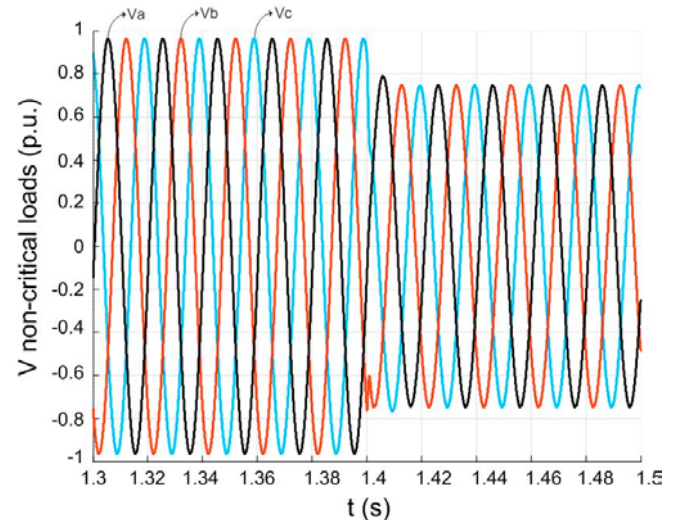


Fig. 7: Voltages of the non-critical loads in the presence of the DVR. (three-phase short-circuit study)

Comparing the in-bus voltages (v_{in}^{abc}) and the out-bus voltages (v_{out}^{abc}), one can see that the DVR also compensates the harmonics produced by itself, reducing a THD of 25% to 1.4%.

The influence of the DVR dynamics in the voltage of the other loads of the system has acceptable levels for this case-study where the DVR was inserted, as shown in Fig. 8. The impedances of the feeders, as well as the short-circuit power (2400 MVA) at the distribution substation bus (see Fig. 3), are relatively high. Due to this, the high distorted currents drained by the shunt diode rectifier of the DVR does not affect considerably the supply voltages of the other feeders. The THD_V measured at the end of a feeder supplying a non-critical load is 1.3% and its positive-sequence voltage is practically equal to the same voltages when there is no DVR in the system (Fig. 4).

B. Single-phase short-circuit simulation

The single-phase short-circuit is the fault that happens more frequently in distribution systems. This type of fault causes voltage sag in only one phase, producing great unbalances in the system.

The same procedure applied to the three-phase fault was applied in this single phase short-circuit study.

Fig. 8 shows the voltages in the critical load. The voltages before the short-circuit event was 1 pu, since the DVR had already compensated the intrinsic 0.05 pu voltage sag of the system. The short-circuit was applied in 1.4s. At this moment a voltage sag, approximately 0.25pu, occurs on phase A of all loads of this system, as presented in Fig. 9. This single-phase sag characterizes the presence of unbalanced voltages in the system.

As defined in [7], the “unbalance, or three-phase unbalance, is the phenomenon in a three-phase system, in which the rms

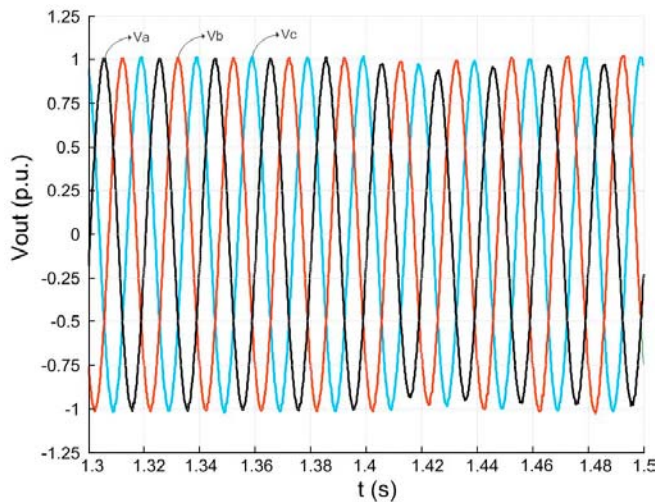


Fig. 8: Critical load voltages protected by the DVR. (single-phase short-circuit study)

values of the voltages or phase angles between consecutive phases are not equal”. The International Electrotechnical Commission (IEC) defined, in [8], a way to express the voltage unbalance in a three-phase system, which is the ratio of the negative-sequence and the positive-sequence voltage component. To comply with this standard, this indicator should be less than 2%.

The presence of the fault is detected by the DVR control, triggering its compensation action. After less than 2 cycles, the out-bus (critical load) voltages of the DVR achieve a steady-state that compensates almost all the unbalance due to the fault. The graphics show a small presence of unbalance. To apply the IEC unbalance voltage indicator it is necessary to determine the symmetrical voltages components [9]. These calculated components are presented in Table I. Therefore, the calculated unbalance voltage indicator is 1.52%, which complies with the IEC standard [8]. This shows a limitation of this DVR, although in this case-study it is still acceptable.

TABLE I
Symmetrical components transformation

Phases	Fundamental voltage magnitude (pu)	Sequence	Component magnitude (pu)
A	$0.9701 \angle 0^\circ$	Positive	$0.9993 \angle 0.7444^\circ$
B	$1.0176 \angle -118.9^\circ$	Negative	$0.01519 \angle -163.1^\circ$
C	$1.0104 \angle 121.1^\circ$	Zero	$0.01699 \angle -149.7^\circ$

The THD of the out-bus (critical load) voltages was calculated for the three phases. The maximum value of it was 1.35%.

As in the three-phase case, the DVR operation does not influence substantially the voltages of other loads of the system.

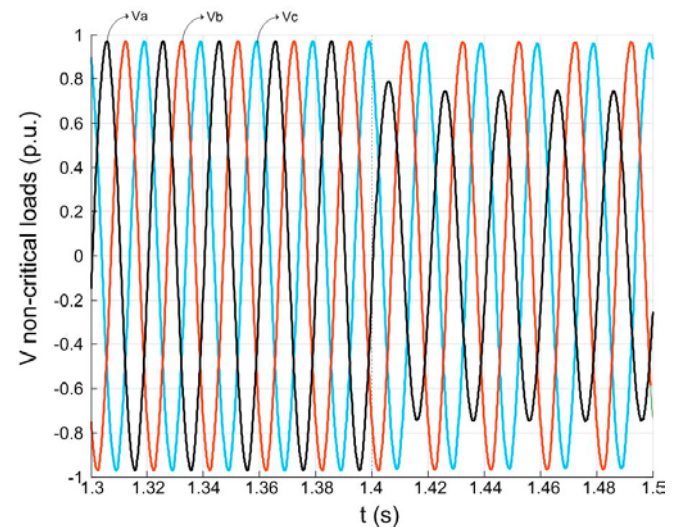


Fig. 9: Voltages of the non-critical loads in the presence of the DVR. (single-phase short-circuit study)

IV. CONCLUSIONS

The proposed DVR operation in a typical distribution system was described. The digital simulation results shows that the DVR successfully compensates the voltage sags and harmonics due a three-phase short-circuit fault, protecting the critical load.

For this case-study, the influence of the DVR over the loads in the neighboring lines, due its harmonics injection in the system, are at acceptable levels.

The unbalance compensation was not fully achieved, as shown in the single-phase results, due limitations of this DVR hardware structure. Although the costs limitations, the performance presented in this case-study are considered acceptable.

Therefore, the use of the proposed DVR in a practical distribution system, like the one presented here, has shown to be viable protecting a critical load connected to a dedicated feeder.

REFERENCES

- [1] N. G. Hingorani, "Introducing Custom Power", *IEEE Spectrum*, vol., no. , pp. 41-48, June 1995.
- [2] O. G. S. Castellões, M. Aredes, "A Series Compensator for Voltage Sags", *Proceedings of the 6th Brazilian Power Electronics Conference*, pp.372-377, November 2001.
- [3] M. Aredes, "Active Power Line Conditioners", *Ph.D. Thesis*, Technische Universität Berlin, Berlin, 1996.
- [4] F. Tosato and S. Quaia, "Voltage Sags Through Fault Current Limitation", *IEEE Transaction on Power Delivery*, vol. 16, no. 1, pp.364-370, January 2001.
- [5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: converters, applications, and design*, John Wiley & Sons, 2nd Ed, New York, 1995, pp. 108,226.
- [6] J.C.Basilio and S.R.Matos, "Design of PI and PID Controllers With Transient Performance Specification", *IEEE Transactions on Education*, vol. 45, no. 4, pp. 364-370, November 2002.
- [7] Math. H. J. Bollen, "Understanding Power Quality Problems – Voltage Sags and Interruptions", *IEEE Press*, New York, 1999, Chapter 1,8.
- [8] Electromagnetic compatibility (EMC), Part2: Environment, Section 2: Compatibility levels for low-frequency conducted disturbances and signalling in public low-voltage power supply systems, *IEC Std. 61000-2-2*.
- [9] C. L. Fortescue, "Method of Symmetrical Co-ordinates Applied to the Solution of Polyphase Networks", *A.I.E.E Trans.*, vol. 37, June 1918, pp. 716-727.