HIGH INPUT VOLTAGE ISOLATED DC-TO-DC CONVERTERS BASED ON MULTILEVEL CELLS

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***Abstract* – This paper presents an overview analysis of high input voltage isolated dc-to-dc converters obtained from the association of multilevel voltage cells, which presents half of the input voltage across the main switches. These converters are suitable for applications in power supplies that have power factor pre-regulators in their input stage. The main topologies of these converters, as well as experimental results 1.5kW, 60V output voltage, 600V input voltage and 50kHz are presented. It is also presented auxiliary circuits that allow an extended range of soft commutation, reduction in the voltage ringing over the output rectifier diodes and blocking of dc components of the current across the isolation transformer.**

KEYWORDS

Multilevel converters. DC-to-DC converters. Soft switching.

I. INTRODUCTION

The power supplies for telecommunications are generally composed by two stages: ac-to-dc and cc-to-cc stages. That equipment has to present high efficiency and to comply with regulations as the IEC61000-3-2. In order to meet the requirements of this standard, the power factor correction (PFC) technique is adopted in the rectifier unit of that equipment. The three-phase single-switch boost rectifier is an interesting option for this PFC stage, since it can easily comply with the IEC61000-3-2 with simplicity, efficiency, reliability, and low cost. However, the use of the three-phase PFC rectifiers leads to an output voltage of the ac-to-dc stage higher than 700V and even high to 1000V, resulting in an increase of the voltage across the switches in the dc-to-dc stage of the power supply.

For output power of 6kW, the dc-to-dc stage is usually implemented with a full-bridge zero-voltage-switching pulse-width modulation (FB-ZVS-PWM) converter [1], associated with a three-phase boost rectifier as shown in Fig. 1. In this case, each switch in the full-bridge topology is subjected to the full bus voltage, leading to an increase of the power losses if MOSFET devices are used in the dc-to-dc converter, or a reduction of the switching frequency if IGBT devices are employed.

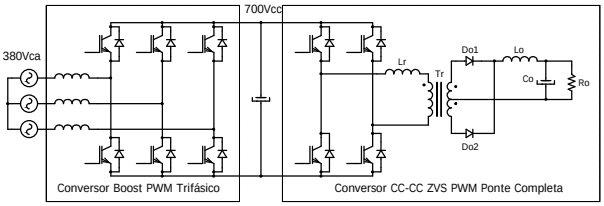

Fig. 1 – High power factor power supply.

In order to reduce the voltage stress across the switches of the dc-to-dc converter, many techniques are being used as: series connection of the switches, multilevel commutations cells association and multilevel converters association.

In the series connection of switches, the static and dynamic sharing of the voltage across the switches are difficult to obtain and requires specific techniques to make sure that all the switches commutate at the very same time: otherwise the switch that turns-off first (or that turns-on last) would have to sustain all of the voltage[3].

The multilevel topologies seems to be a more effective solution because they can solve the problem of static and dynamic sharing of the voltage, and reduce problems of EMI, once dV/dt over the switches can be limited to standard values.

The association of multilevel cells consists of a commutation cell using series-connected semiconductors with clamping circuits ensuring the voltage sharing across the blocking switches.

This paper presents an analysis of three high-input voltage isolated dc-to-dc converters based on the multilevel cell association, as well as experimental results 1.5kW, 60V output voltage, 600V input voltage and 50kHz. Auxiliary circuits that allow an extended range of soft commutation, reduction in the voltage ringing over the output rectifier diodes and blocking of dc components of the current across the isolation transformer, are also presented and discussed.

II. ZVS PWM DC-TO- DC CONVERTER BASED ON THE NEUTRAL-POINT-CLAMPED MULTILEVEL CELL (NPC)

The ZVS-PWM DC-to-DC Converter proposed in [2], based on the three-level neutral-point-clamped cell is presented in Fig. 2.

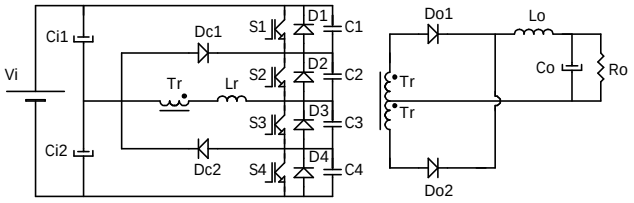

Fig. 2 – The ZVS-PWM DC-to-DC converter based on the three-level neutral-point-clamped cell (NPC).

The switches S1, S2, S3 and S4 form the main commutation leg. The diodes D_1, D_2, D_3 and D_4 conduct inverse polarity current and clamp the switch voltage at a reverse voltage (-1V).

The inductance L_r (which incorporates the leakage inductance of the isolation transformer T_r) and the capacitors C_1, C_2, C_3 and C_4, provide a resonant transition permitting zero-voltage turn-on, that eliminates turn-on switching power losses. The capacitors $C_1$to C_4, also provide capacitive turn-off snubbing reducing the commutation losses.

The diodes D_{c1} e D_{c2} are the responsible for the voltage clamping across the main switches to half of the input voltage (Vi/2).

The transformer T_r provides galvanic isolation and voltage transformation between the source and the load.

The output stage is formed by the rectifiers diode D_{o1} e D_{o2}, and by the output filter composed of L_o and C_o.

The current and voltage stresses of the switches are presented on Table I. The variable D, defined in (1), represents the reduction of the duty-cycle of the converter due to reactive energy circulation in the converter, necessary to assure soft commutation.

$$D = \frac{4.f_s.L_r.I_o}{V_i} \qquad (1)$$

TABLE I
Current and Voltage Stresses– NPC converter

Component	S_1,S_4	S_2,S_3	D_{c1},D_{c2}	D_{o1},D_{o2}
Peak Voltage	Vi/2	Vi/2	Vi/2	Vsec
RMS Current (p.u.)	$\sqrt{D - \frac{5}{6}.D}$	$\sqrt{\frac{1}{2} - \frac{5}{6}.D}$	--	--
Average Current (p.u.)	--	--	1/2 - D	1/2

III. ZVS PWM DC-TO- DC CONVERTER BASED ON THE FLYING CAPACITOR MULTILEVEL CELL (FC)

The ZVS-PWM DC-to-DC Converter proposed in [3], based on the three-level flying capacitor cell is presented in Fig. 3.

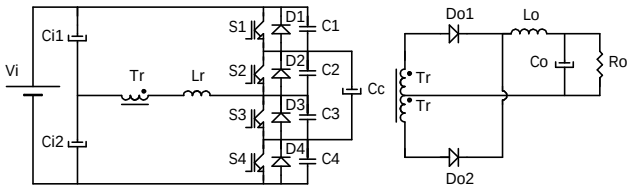

Fig. 3 – The ZVS-PWM DC-to-DC converter based on the three-level flying capacitor cell (FC).

The flying capacitor C_c is the responsible of the voltage clamping across the main switches to half of the input voltage (Vi/2).

The other components has identical functions as described in the converter NPC.

The current and voltage stresses of the switches are presented on Table II, with the variable D defined in (1).

TABLE II
Current and Voltage Stresses– FC converter

Component	S_1,S_3	S_2,S_4	C_C	D_{o1},D_{o2}
Peak Voltage	Vi/2	Vi/2	Vi/2	Vsec
RMS Current (p.u.)	$\sqrt{\frac{1}{2} - \frac{5}{6}.D}$	$\sqrt{D - \frac{5}{6}.D}$	$\sqrt{1 - 2.D}$	--
Average Current (p.u.)	--	--	--	1/2

IV. ZVS PWM DC-TO- DC CONVERTER BASED ON THE MODIFIED FLYING CAPACITOR MULTILEVEL CELL (MFC)

The ZVS-PWM DC-to-DC Converter proposed in [4], based on the three-level modified flying capacitor cell is presented in Fig. 4.

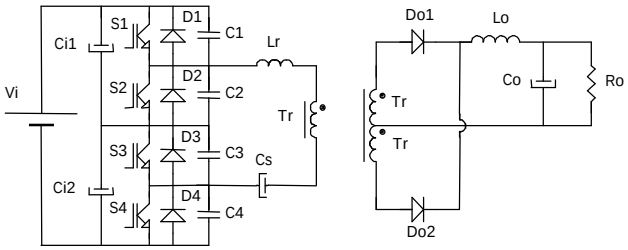

Fig. 4 – The ZVS-PWM DC-to-DC converter based on the three-level modified flying capacitor cell (MFC).

This converter consists in an association of two commutation legs, S_1-S_2 and S_3-S_4. In the connection of these two legs is connected the middle point of an capacitive divider composed by the input capacitors C_{i1} e C_{i2} that are responsible by the voltage clamping across the main switches to half of the input voltage (Vi/2).

The capacitor C_S is a dc-blocking capacitor that blocks the dc voltage from being applied to the series combination L_r-T_r, allowing a three-level voltage across the power transformer T_r.

The current and voltage stresses of the switches are presented on Table III, with the variable D defined in (1).

TABLE III
Current and Voltage Stresses– MFC converter

Component	S_1,S_3	S_2,S_4	C_S	D_{o1},D_{o2}
Peak Voltage	Vi/2	Vi/2	Vi/2	Vsec
RMS Current (p.u.)	$\sqrt{D - \frac{5}{6}.D}$	$\sqrt{\frac{1}{2} - \frac{5}{6}.D}$	1/n	--
Average Current (p.u.)	--	--	--	1/2

V. COMMUTATION ANALYSIS

In all converters the resonant inductance L_r along with snubber capacitors C_1 to C_4 provide a resonant transition

permitting zero-voltage turn-on that eliminates turn-on switching power losses. The energy stored in L_r charges and discharges the snubber capacitors during a conduction gap that is provided between turning-off one switch and turning-on the other switch of the pair. The action brings the switch voltage to zero before the switch is turned-on.

The minimum load current that guarantees zero-voltage switching for the NPC converter is defined in (2) and for FC and MFC converters is defined in (3), where $C = C_1 = C_2 = C_3 = C_4$.

$$Io_{\min} = \frac{Vi}{2}\sqrt{\frac{3C}{2Lr}} \qquad (2)$$

$$Io_{\min} = \frac{Vi}{2}\sqrt{\frac{2C}{Lr}} \qquad (3)$$

For all converters the output voltage can be calculated using (4). From (1) and (4) can be noticed that the larger Lr is, the larger the reduction of the output voltage caused by the reactive voltage drop. So a good design involves sacrificing the soft-commutation at light load, where the conduction losses are low, to obtain high efficiency at full-load.

$$Vo = \frac{Vi}{n}.(D \quad D) \qquad (4)$$

VI. EXPERIMENTAL RESULTS

In order to compare experimentally the behaviour of the converters, three prototypes were built with the input data presented in Table IV.

The design procedures of the converters studied in this paper are presented in [2], [3] and [4].

MOSFETs were used to implement switches S_1, S_2, S_3 and S_4. The diodes D_1, D_2, D_3 and D_4 are the MOSFET´s body diodes and the capacitors C_1, C_2, C_3 and C_4, are the MOSFET´s C_{oss} capacitances.

TABLE IV
Input Data

Input voltage – Vi (V)	600
Output voltage – Vo (V)	60
Output power – Po (kW)	1.5
Switching frequency – fs (kHz)	50
Input voltage ripple - Vi (V)	15
Output current ripple - Io (A)	2.5
Output voltage ripple - Vo (V)	0.06
Clamping voltage ripple - V_{Cc} (V)	3
ZVS load range (%)	30-100
Maximum duty-cycle – D_{max}	0.4

Experimental results of an output power of 1.5kW, output current of 25A, input voltage of 600V, and switching frequency of 50kHz are shown in Figs. 5 to 10. The figures present, for each converter, the three-level voltage of the inverter stage, the current through the resonant inductor and the voltages and currents of the main switches. In each case the duty-cycle was set in order to obtain an output voltage Vo equal to 60 V for full load (25 A).

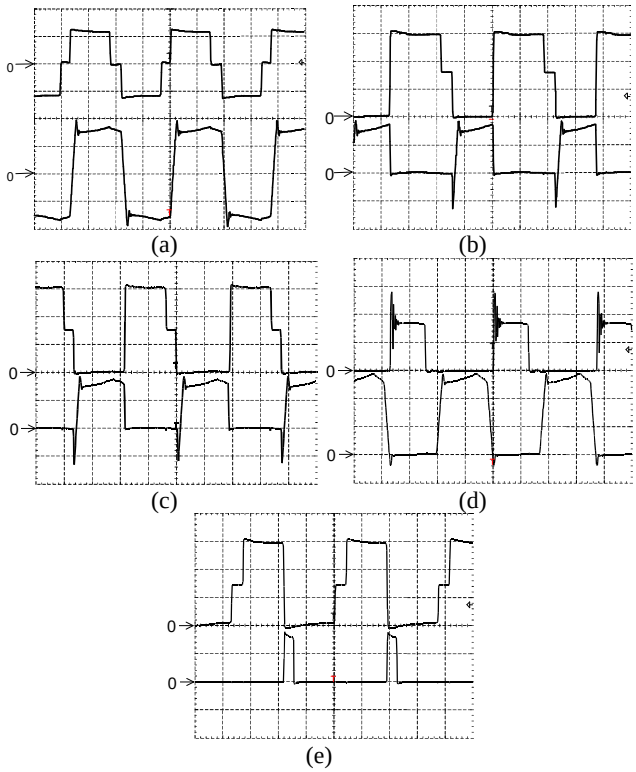

Fig. 5 – Experimental waveforms – NPC converter.
(a) upper trace: voltage v_{ab} (250V/div); lower trace: current i_{Lr}(5A/div);
(b) upper trace: voltage v_{S1} (100V/div); lower trace: current i_{S1} (5A/div);
(c) upper trace: voltage v_{S2} (100V/div); lower trace: current i_{S2} (5A/div);
(d) upper trace: voltage v_{Do1} (100V/div); lower trace: current i_{Do1} (10A/div);
(e) upper trace: voltage v_{Dc1} (100V/div); lower trace: current i_{Dc1} (5A/div);
Time scale: 5 s/div

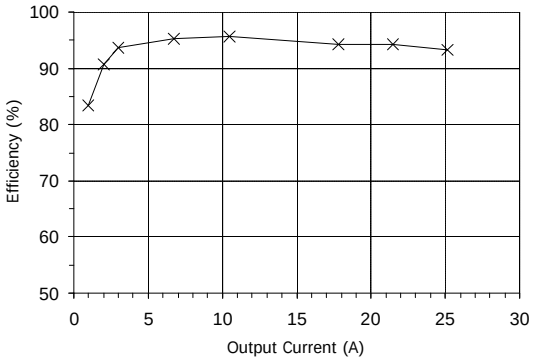

Fig. 6 – Efficiency x output current – NPC converter.

It is important to emphasize that the peak voltage across the switches, for all the converters, is 300 V, half of the 600 V dc input voltage. All the converters present similar switches voltage and current waveforms and zero-voltage switching.

TABELA V
Converter Components

COMPONENT	CONVERTER		
	NPC	FC	MFC
S_1-S_4	IRFP460 – 500V, 20A (Harris)		
L_r	16 H –ferrite core E42/15 IP12 (Thornton)		20.5 H - ferrite core E42/15 – IP12 (Thornton)
$C_{i1} – C_{i2} – C_{i3} – C_{i4}$	2 F/400V – polyester (Icotron)	3 F/400V – polyester (Icotron)	1 F/400V – polyester (Icotron)
$C_c – C_{c1} – C_{c2} – C_s$	-	3 x 2 F/400V – polyester o (Icotron)	3 x 2 F/400V – polyester (Icotron)
D_{c1}-D_{c2}	MUR840 (Motorola)	-	
T_r	2 ferrite cores E65/26 - IP12 (Thornton) Prim.: 17 esp. Sec.: 5+5 esp. - 22AWG		
D_{o1} - D_{o2}	MUR1560 – 600V, 15A (Motorola)		
L_o	89 H – ferrite core E55/21 - IP12 (Thornton)		
C_o	220 F/100V - electrolytic (Icotron)		

Figs. 6, 8 and 10 present the measured efficiency of the converters as a function of the output current, experimentally obtained for constant input voltage equal to 600 V and constant duty-cycle. In general the measured value at full load is above 92%.

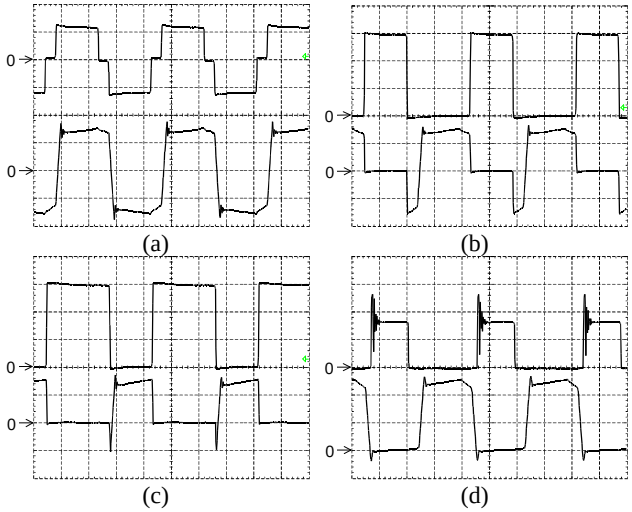

Fig. 7 - Experimental waveforms – FC converter.
(a) upper trace: voltage v_{ab} (250V/div); lower trace: current i_{Lr}(5A/div);
(b) upper trace: voltage v_{S1} (100V/div); lower trace: current i_{S1} (5A/div);
(c) upper trace: voltage v_{S2} (100V/div); lower trace: current i_{S2} (5A/div);
(d) upper trace: voltage v_{Do1} (100V/div); lower trace: current i_{Do1} (10A/div);
Time scale: 5 s/div.

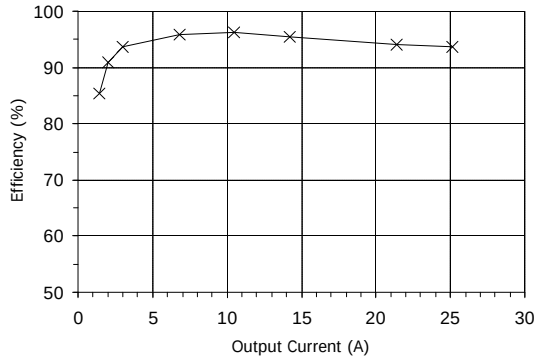

Fig. 8 – Efficiency x output current – FC converter.

The main sources of losses are diode and MOSFET conduction losses, magnetic and snubber losses. The switching losses at full load are practically zero due to zero-voltage turn-on and capacitive turn-off snubbing.

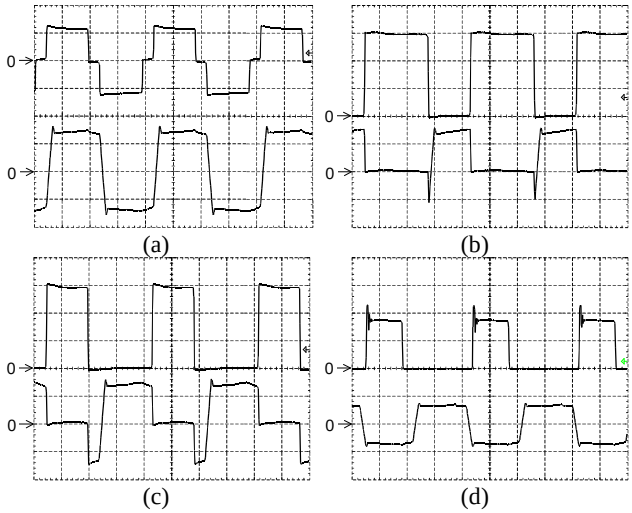

Fig. 9 - Experimental waveforms – MFC converter.
(a) upper trace: voltage v_{ab} (250V/div); lower trace: current i_{Lr}(5A/div);
(b) upper trace: voltage v_{S1} (100V/div); lower trace: current i_{S1} (5A/div);
(c) upper trace: voltage v_{S4} (100V/div); lower trace: current i_{S4} (5A/div);
(d) upper trace: voltage v_{Do1} (100V/div); lower trace: current i_{Lr} (10A/div);
Time scale: 5 s/div.

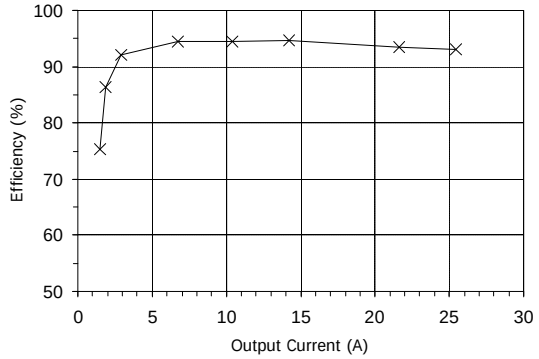

Fig. 10 – Efficiency x output current – MFC converter.

The efficiency for all the converters clearly decreases for load currents lower than 5 A, when the ZVS commutation is lost and the converter starts to operate with hard-switching.

VII. AUXILIARY CIRCUITS

A. Extended soft commutation range

As seen in section V, the dc-to-dc converters based on the

multilevel cells needs a minimum load current in order to guarantees zero-voltage switching in all of their switches. To assure soft-switching over all the load range, it was proposed in [5] the introduction of an auxiliary circuit composed by two capacitors and one inductor in the NPC converter, as shown in Fig. 11.

Even with the increase of the circulating energy in the converter, the converter presented no significant reduction in the overall efficiency at full load.

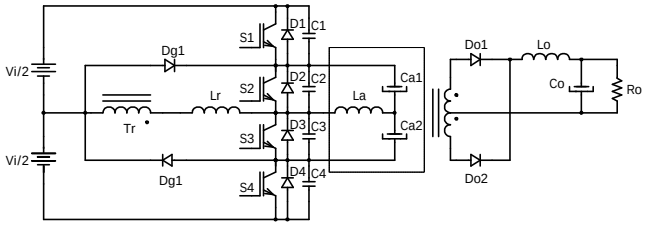

Fig. 11 – NPC converter with commutation auxiliary circuit.

B. Output rectifier voltage clamping

In the waveforms of the voltage across the output rectifiers (Fig. 5d, 7d e 9d) it can be observed voltage oscillations due to the process of reverse recovery of the diodes with the leakage inductance of the power transformer and the resonant inductance reflected to the secondary.

These oscillations cause power losses in the RCD snubber circuit used to dump the voltage spikes and also generate high level of EMI [6].

In order to eliminate the oscillations and the voltage spike, it has been proposed many techniques as:

a) the use of two small clamping diodes (D_{g1} e D_{g2}), with no heatsink [6], presented in Fig. 12, which creates an alternative path for the reverse recovery current of the output diodes for the input source. In this manner, this current doesn't circulate through the resonant inductance L_r;
b) the use of a "Hybridge" rectifier with a passive clamping circuit, presented in Fig. 13 in a NPC converter [7], which reduces the current through the secondary winding of the power transformer, limits the peak voltage across the output diodes to the voltage defined by the clamping circuit, and sends the energy of reverse recovery from the diodes to the load/
c) the use of a "Hybridge" rectifier with a active clamping circuit based on the forward converter, presented in Fig. 14 in a NPC converter [8], that allows an increase of the overall efficiency of the converter in comparison to the circuit of Fig. 13.

C. Blocking of dc components of the current across the isolation transformer

Small unbalances in the input voltage or differences in the gate signals of the switches can cause the circulation of dc current components through the isolation transformer. These components can saturate the transformer, and must be avoided [7].

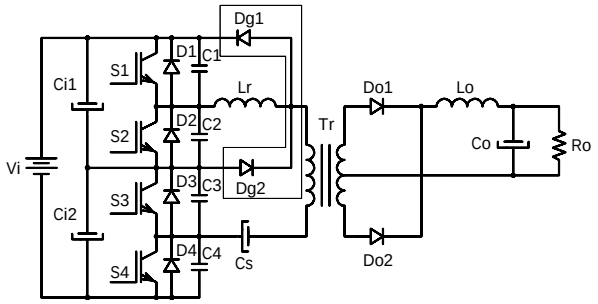

Fig. 12 – CFM converter with two clamping diodes.

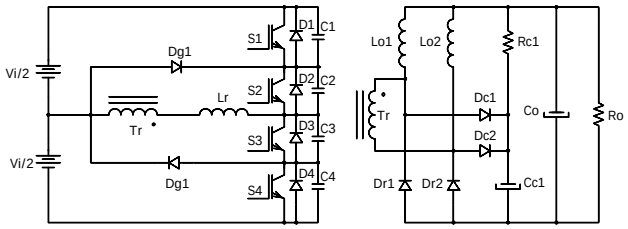

Fig. 13 – NPC converter with "Hybridge" rectifier and passive clamping circuit.

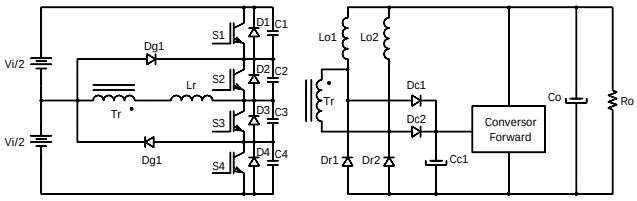

Fig. 14 – NPC converter with "Hybridge" rectifier and active clamping circuit.

To block such components the use of blocking capacitor in series with the primary of the transformer is proposed in [7], and it is presented in Fig. 15 in a FC converter. This solution can be used for an NPC converter. In the case of the MFC converter, the blocking capacitor is a part of the original converter, so it is not necessary to include another one.

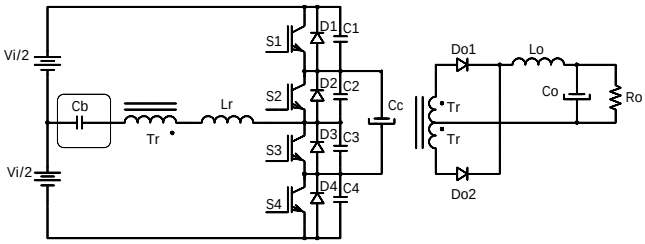

Fig. 15 – FC converter using a blocking capacitor.

VIII. CONCLUSIONS

This paper presented an analysis of the main topologies of isolated dc-to-dc converters with zero-voltage commutation and pulse-width modulation based on the multilevel cell association, as well as experimental results 1.5kW, 60V output voltage, 600V input voltage and 50kHz.

The converters analysed presented identical characteristics to the FB-ZVS-PWM converter with half of the input voltage across the blocking switches, and high efficiency (above 92%

at full load) due to ZVS commutation on the switches.

It was also presented auxiliary circuits that allow an extended range of soft commutation, reduction in the voltage ringing over the output rectifier diodes and blocking of dc components of the current across the isolation transformer, avoiding its saturation.

From the results obtained, one can conclude that the converters presented in this paper are appropriate for applications in high input voltage power supplies, since they allows the use of switches of lower voltage than the ones that would be used in a full bridge ZVS-PWM dc-to-dc converter, with the same level of efficiency.

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