IMPROVEMENT OF A POSITIVE-SEQUENCE COMPONENTS DETECTOR IN A UNBALANCED THREE-PHASE SYSTEM

FÁBIO D. JESUS*, CARLOS F. T. SOARES*, JOSÉ L. S. NETO*, EDSON H. WATANABE*, MAURÍCIO AREDES*, JOSÉ R. D. CARVALHO**, MARCELO J. LEAL**

*COPPE – Laboratório de Eletrônica de Potência, Programa de Engenharia Elétrica
Universidade Federal do Rio de Janeiro
PO Box 68.504, CEP21.945-970, Rio de Janeiro, RJ, Brasil

fabio@coe.urfj.br; cfts@coe.ufrj.br; luizneto@dee.ufrj.br; watanabe@coe.ufrj.br and aredes@ufrj.br

**CERJ – Companhia de Eletricidade do Rio de Janeiro
Praça Leoni Ramos, no 1
CEP 24210-205,Niteroi, RJ, Brasil
jcr@cerj.com.br and mleal@cerj.com.br

***Abstract* – This paper presents an improvement on the structure of a Phase Locked Loop (PLL), to detect in real time the phase-angle of the positive-sequence component of the voltage in an unbalanced three-phase system. In conventional PLL algorithms, when the voltages are unbalanced, the detected phase-angle presents errors that may be unacceptable for some FACTS controllers. The improvement proposed in this work is to minimize this error keeping a fast dynamic response in the range of a cycle. Comparative simulation results between the conventional PLL and the proposed new-structure will be shown.**

KEYWORDS

Phase Locked Loop (PLL), unbalanced system, FACTS.

I. INTRODUCTION

Several different equipments based on Power Electronics devices are used in industrial applications and in power system applications. These equipments, in many cases, need the precise information about the phase angle of the positive-sequence voltage component of the system to operate properly. This information is typically obtained from the grid using some form of a phase locked loop (PLL) circuit. However, when the voltages present in the system are distorted with harmonics, including notches, unbalances or deviations frequency, they induce an error in the measurement of the phase angle. Thus, for some applications, as STATCOMs for instance, this error may be unacceptable.

Many papers have been presented in the literature addressing the problem of minimization the errors due to voltage distortions or unbalances [1].[2],[3]. In [2] the method of symmetrical optimum [4] is proposed to calculate the PI-regulator (Proportional-Integral) gains, to improve the dynamics of the PLL. In [5] the Winner method [6] is used to have the best optimization method for the second order PLL systems. Although these works present good results, they are not robust against unbalanced voltages and therefore should be improved.

In order to overcome the problems present in conventional PLL systems, this paper proposes a new structure of PLL with the addition of a moving-average filter in series with the proportional–integral regulator. Some comparative simulation results and discussions on differences between the conventional PLL and the proposed PLL are shown.

II. PLL PRINCIPLE OF OPERATION

The voltages at a transmission- or distribution- system can be balanced or unbalanced, with or without harmonics. Thus, the general phases voltages (v_a,v_b and v_c) can be represented by :

$$\begin{aligned} v_a &= \sqrt{2}_{+}V \sin(wt+f_{+}) + \sqrt{2}V \sin(wt+f) + \\ &\quad \sqrt{2}^{+}V_{ah} \sin(w_h t+f_h) \\ v_b &= \sqrt{2}_{+}V \sin(wt \quad 2p/3+f_{+}) + \sqrt{2}V \sin(wt+2p/3+f) + \\ &\quad \sqrt{2}^{\pm}V_{bh} \sin(w_h t+f_h) \\ v_c &= \sqrt{2}_{+}V \sin(wt+2p/3+f_{+}) + \sqrt{2}V \sin(wt \quad 2p/3+f) + \\ &\quad \sqrt{2}^{\pm}V_{ch} \sin(wt+f_h) \end{aligned} \qquad (1)$$

where the subscripts (+), ( ) and (*h*) denote the positive, negative sequence variables and harmonics components. V+, V are the rms-values of the fundamental components of the positive and negative sequences voltage components, respectively.

The objective of the PLL is to detect phase-angle of the fundamental positive-sequence voltage in phase "*a*", i.e. = ($t+f_+$). The phase angles for the others phases are displaced by 120° and 240° respectively. The basic configuration of the PLL algorithm is shown in Fig. 1. This

configuration is defined as q-PLL and, as it can be seen, based on the instantaneous real and imaginary power theory [7].

In Fig. 1, the set of three-phase instantaneous voltages in (a-b-c) coordinates can be transformed to (- -0) coordinates by:

$$\begin{matrix} v_a \\ v_b \end{matrix} = \sqrt{\frac{2}{3}} \cdot \begin{matrix} 1 & 1/2 & 1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{matrix} \cdot \begin{matrix} v_a \\ v_b \\ v_c \end{matrix} \qquad (2)$$

In the block diagram in Fig. 1, the voltages v_a and v_b are multiplied by two fictitious currents : i'_a and i'_b respectively. This product results in a fictitious instantaneous imaginary power (q´) represented by:

$$q' = v_b i_a' \quad v_a i_b' \qquad (3)$$

This imaginary power (q') is the input of the proportional-integral controller (PI), which outputs a signal corresponding to the angular frequency, $_c$. This frequency signal is integrated to produce the synchronizing signal q_c. When the angular frequency $_c$ (rad/s) generated by PLL is equal to the angular frequency of the fundamental component of the system (rad/s), the fictitious currents i'_a and i'_b are in phase with the voltages of the system, v_a and v_b. In this situation, the average value of q' will be null. The integrator block is reset wherever q_c reaches 2 . This is the ideal operation of the PLL shown in Fig. 1.

Considering that the instantaneous voltages in (3) are arbitrary and can contain distortions and harmonics, the instantaneous fictitious imaginary power q' can be separated in its average and alternating components [8]:

$$q' = \bar{q} + \tilde{q} \qquad (4)$$

where, the “bar” represents the average and “tilde” the alternating values.

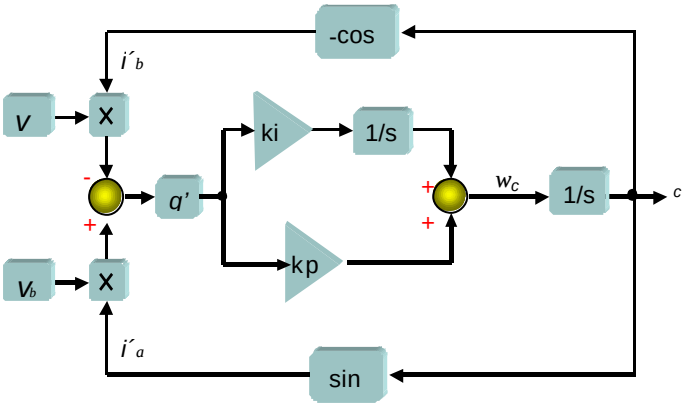


Fig. 1: Block diagram q-PLL.

From Fig. 1 it is possible to see that, if the voltage is distorted or unbalanced, the signal q' will contain oscillating component $\tilde{q}$ that, after passing through the PI controller will produce a w_c with oscillating components. This will produce errors in the phase signal q_c. The idea in this paper is to solve this problem by introducing a filter between the PI controller and the integrator. The objective is to eliminate the effect of the oscillating component in q'.

III. Moving Average Filter

The moving-average filter is represented basically by an integration block, a transport delay block, a subtractration block and a division block, which is shown in Fig. 2. In this figure, the transport delay block output is the input signal value delayed by 1/k of the fundamental period, where k is an integer. The difference between the integrator block output (1) and the transport delay block output (2), represents the input signal integration over the interval [t- T/k,t], where T is the period of the fundamental component of the input signal. Finally, the division block divides the integrated input signal (3) by the integration interval, that is, T/k. Theforore, the output obtained is the moving average of the input signal calculated over the time interval T/k.

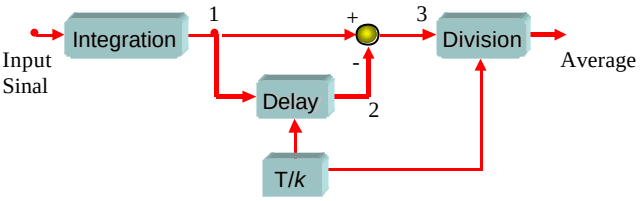


Fig. 2: Block diagram moving-average filter.

In Fig. 2, the output is given by [9]:

$$Moving_{average\ (d\ \text{or}\ q)} = \frac{k}{T} \cdot \int_{t-\frac{T}{k}}^{t} f(t).dt \qquad (5)$$

where $f(t)$ is the signal at the input of the filter.

IV. Improved PLL

The block diagram of the proposed PLL structure can be described as shown in Fig. 3. In this figure, the main modification is the addition of the moving average filter in series with the PI-controller of the conventional q-PLL.

The purpose of the moving average filter is to reduce the influence of harmonics and negative sequences components, present in the voltages v_a and v_b, in the signal w'_c.
In the previous section, it was shown that the filter depends on the value of the constant k to calculate the average correctly. Thus, the value of the constant k of the moving average filter should be carefully chosen.

In Fig 3, all distortions can be present in the voltages at the same time. By choosing k=1 the average of all distortions will be null, except for the fundamental harmonic.

The disadvantage of this method is that the moving average filter will have one cycle of time response. This dynamic response can be as faster as the period of a specific harmonic (n^{th} order) wanted to be removed, by simply making k=n. However, the choice of k=1, does not degrade the dynamic performance of filters for most of the industrial and power system applications.

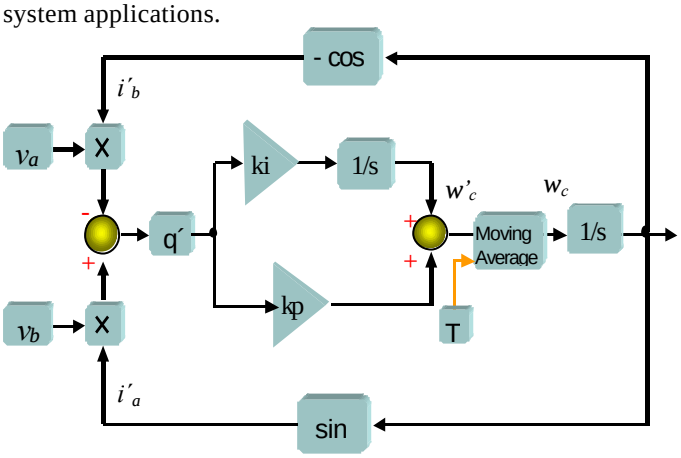


Fig. 3: Improved PLL.

The modified algorithm has the same basic operating principle of a conventional PLL. The proposed PLL is designed to detect phase angle without error even if the system voltage is unbalanced. The tracking error present in the operation of the PLL described in [10], may not be acceptable in some FACTS equipment.

To determine the range of possible values for the parameters of the PI controller, it is necessary to derive a valid model for small perturbations. The mathematical model derived in [10] can be used here for the analysis of the conventional PLL. The linearized model of a conventional PLL is shown in Fig. 4, and its transfer function is given in (6).

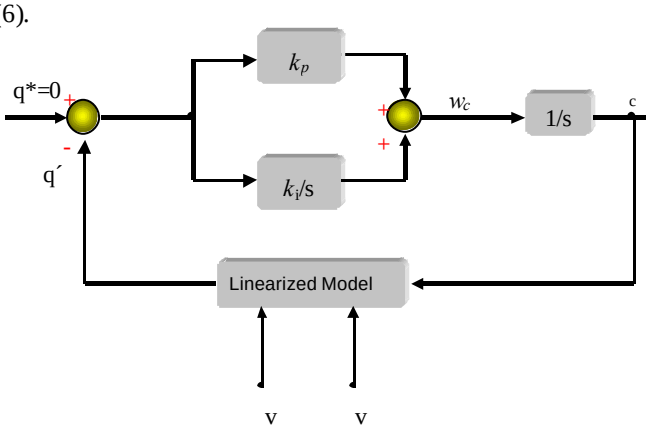


Fig. 4: Block diagram of the linearized conventional PLL.

$$\frac{w_c}{w} = \frac{s(k_p k_o) + k_i k_o}{s^2 + s k_p k_o + k_i k_o} \qquad (6)$$

where $k_o = \sqrt{3} V_o \cos(q_0 \quad q_{co})$

The addition of the moving average filter to this model, leads to the block diagram of the new PLL structure represented in Fig. 5.

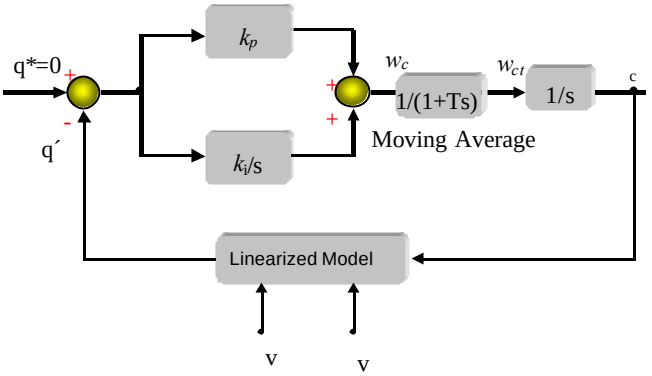


Fig. 5: Block diagram of the PLL with moving average filter.

The transfer function of the moving average filter can be determined by Padé approximation [11]. For the present case, it is considered that the first order approximation is sufficient for the analysis. Therefore, the following two equations will be considered:

$$e^{-sT} \quad \frac{1}{1+sT}. \qquad (7)$$

$$\frac{w_{ct}}{w} = \frac{s(k_p k_o) + k_i k_o}{Ts^3 + s^2(1 + k_p k_o T) + s(k_p k_o + k_i k_o T) + k_i k_o}, \qquad (8)$$

where T denotes the interval of integration of the moving average filter.

As one can see in (8), a pole was added to the transfer function given in (6). This additional pole is, obviously, due to the moving average filter dynamics. Thus, the choice of the controller gains should be different in this case.

Fig. 6 shows the location of the poles and zeros of (8) for different values of the proportional gain.

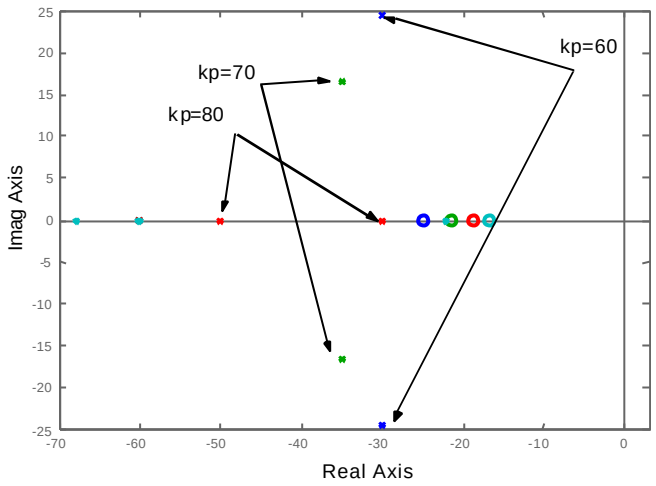


Fig. 6: Poles and zeros location for ki =1500 and different values of kp.

V. RESULTS

The performance of the proposed algorithm was compared, in simulations, with that of a conventional PLL. Three cases are considered here:

a) Balanced three phase voltages, with even and odd harmonics;
b) Unbalanced voltages (no distortion);
c) Frequency deviation.

As the averaging period was taken equal to the fundamental frequency period, the moving average filter needs one cycle to calculate the average correctly. The PI controller gains were chosen to produce a response slower than the moving average filter: kp =60 [rad/Ws], ki=1500 [rad/Ws^2].

For the first case, the hypothetical voltage waveform and its harmonic content are shown in Fig. 7. The voltage waveform contains the 2nd and the 7th order harmonics, each having 10 % of the fundamental component amplitude.

Fig. 8 shows the angular frequency signal $_c$ calculated using the conventional and proposed PLL. It can be observed that both PLL reach the steady state in less than 0.15 s. However, a small oscillation can be observed in the angular frequency obtained with the conventional PLL. The proposed PLL produces a clean frequency signal.

Fig. 9 shows error between the calculated and the actual phase angle for the two PLL algorithms. In this figure it can be verified that both PLL produced a error practically null, when even and odd harmonics are present.

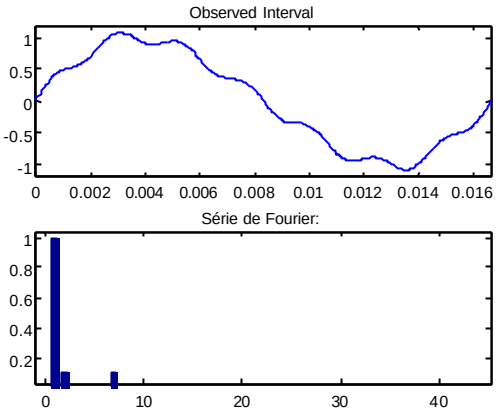
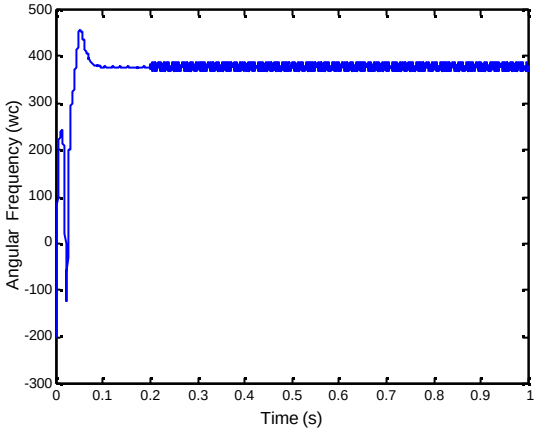
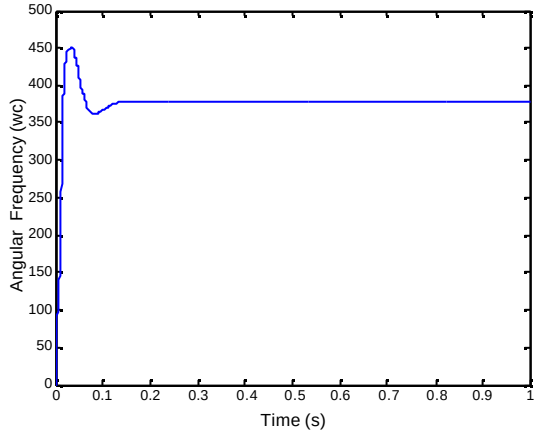


Fig. 7: Voltage v_a and its harmonic content.

In the second case an unbalance is applied at t = 0.5 s due to a voltage sag of 40% in one phase (type voltage sag D [12]).



(a)



(b)

Fig. 8: Three-phase balanced voltages with even and odd harmonics: (a) conventional PLL ; (b) proposed PLL.

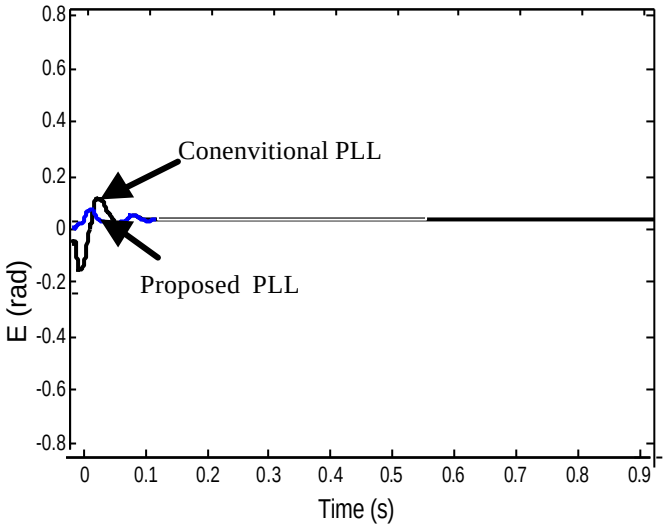
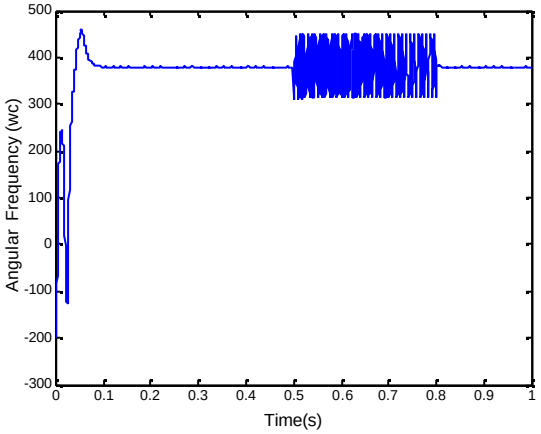
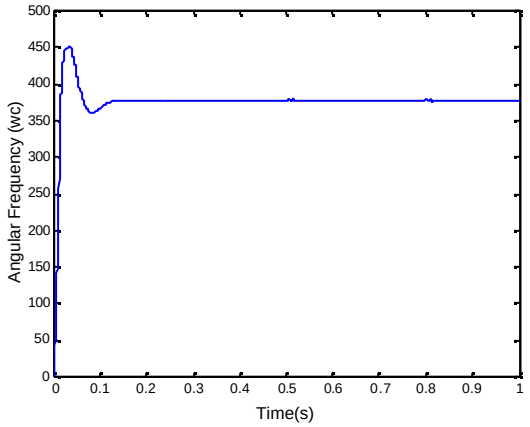


Fig. 9: Detction error (E) with even and odd harmonics in the voltage.

Fig. 10 shows the signal $_c$ calculated by the conventional and the proposed PLL. In this figure it is observed that the new PLL algorithm can detect the angular frequency even when 40% voltage sag occurs in one phase only.



(a)



(b)

Fig. 10: Three-phase unbalanced: (a) conventional PLL; (b) proposed PLL.

Fig. 11 shows that the conventional PLL produced a phase angle with a error considerable. It can be seen that the proposed PLL has a superior performance than the conventional PLL.

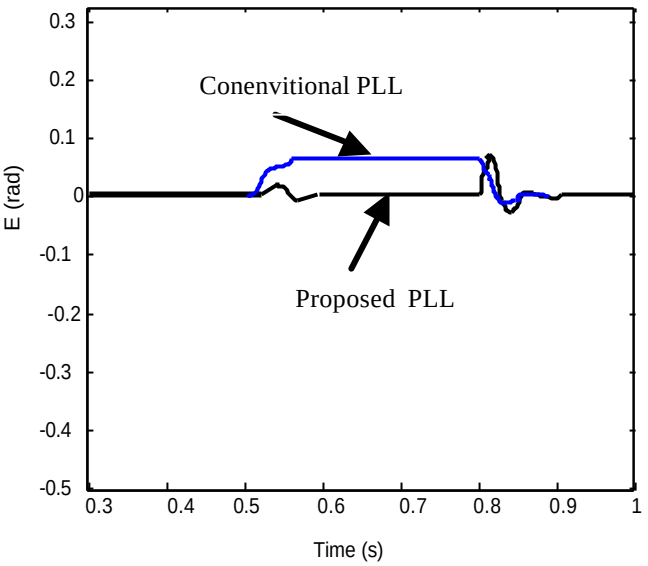


Fig. 11: Detction error (E) with even and odd harmonics in the voltage with unbalanced voltage.

In the last case, a frequency deviation of 10 Hz in the voltage system occurs at t = 0.3 s. Fig. 12 shows that the proposed PLL can track the new frequency without oscillations. It was verified by other simulations not presented here, that the proposed PLL has a very good tracking for frequency deviations up to 40 Hz.

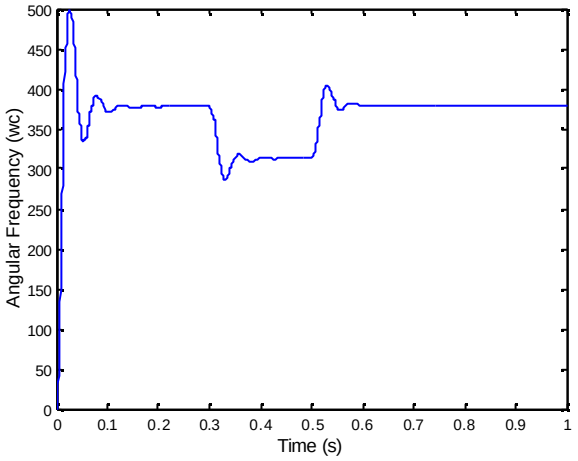


Fig. 12: Signal angular frequency w_c proposed q-PLL with deviation frequency.

VI . CONCLUSION

This work has proposed a new PLL algorithm. The results of digital simulation show that the new PLL structure presents a better performance than the conventional PLL even when the three-phase grid voltages contain harmonics components or

unbalances.

The authors believe that this PLL may be useful for some FACTS applications were the fundamental positive sequence voltage must be accurately detected as in STATCOM, UPFC etc.

VII . REFERENCES

[1] Best, R. E., " Phase Locked Loops – Theory, Design and Applications", McGraw-Hill Book, USA, 1984;

[2] Kaura, V., Blasko, V., " Operation of a phase locked loop system under distorted utility conditions", IEEE Trans. Ind. Apll., vol. 33,pp 58-63,1997;

[3] Chung, S. K., " A Phase Tracking System For Three Phase Utility Interface Inverters", IEEE Trans. Power Electronics, Vol. 15, N0 3, May 2000.

[4] W. Leonard, Control of Electrical Drives, Berlin, Germany: Springer-Verlag, 1985.

[5] Chung, S. K., " A Phase Tracking System For Three Phase Utility Interface Inverters" , IEEE Trans. Power Electronics, Vol. 15, N0 3, May 2000.

[6] F. M. Gardner, Phaselock Techniques, New York: Willey, 1979.

[7] Barbosa, P. G., "Compensador Série Síncrono Estático Baseado em Conversores VSI Multipulso", D.Sc Tese, COOPE/UFRJ, Rio de Janeiro, RJ, Brasil, 2000. (in Portuguese)

[8] Watanabe, E. H. e Aredes, M., "Teoria de Potência Ativa e Reativa Instantânea e Aplicações – Filtros Ativos e FACTS", XII Congresso Brasileiro de Automática – XII CBA, Uberlândia, MG, 15 e 16 de setembro 1998. (in Portuguese)

[9] Oliveira, L. E. L, Silva, L. E. B., " Improving the Dynamic Response of Active Power Filters Based on the Synchronous Reference Frame Method", The 6th Brazilian Power Electronics Conference – COBEP'2001, Florianópolis, SC, novembro 11 a 14 de 2001. (in Portuguese)

[10] Sasso, M. E. et al., " Investigação dos modelos de circuitos de sincronismo baseados na teoria das potências real e imaginária instantânea", XIV Congresso Brasileiro de Automática – XIV CBA, Natal, RN, 02 e 5 de setembro 2002. (in Portuguese)

[11] Franklin, G. F, Powell, D. J., "Feedback Control of Synamic Systems", Addison-Wesley Publishing Company, USA, 1994.

[12] M. H. J. Bollen and E. Styvaktakis, " Characterization of three-phase unbalanced dips (as easy as one-two three)" in proc. 2000 IEEE Int. Conf. on Harmonics and Quality of Power, vol.1,pp. 81-86.