ON DISCRETE CONTROLLERS FOR STATIC CONVERTERS

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***Abstract* – This paper addresses the main issues associated with the analysis and design of discrete controllers for static converters. Aliasing and the limitations of digitally adjusted PWM are first discussed. Then, a procedure to obtain discrete dynamic models of static converters is detailed and a review of the classical discrete analysis and design methods is presented. Finally, three examples are developed to demonstrate the potential of discrete controllers for power electronics applications.**

***Keywords* – Discrete Controllers, Static Converters.**

I. INTRODUCTION

Discrete controllers for static converters have recently received a growing attention from the academia as well as from the industry. This is attributed to fact that discrete controllers have a number of potential advantages over the analog counter parts. Among them are: low sensitivity to parameters variations; (ii) reduced number of passives components; (iii) possibility of implementation of advanced control, protection and calibration algorithms; (iv) flexibility and programmability. In addition, DSP controllers and microcontroller manufactures are making available high performance low cost processors with peripherals suitable for controlling static converters, which include analog-to-digital converters with multiples channels, encoders and PWM generators. The trend toward discrete controllers has even reached the Switching Mode Power Supplies (SMPS) segment where the analog controllers IC are been considered to be replaced by integrated digital controllers [23]. In this context, this paper reviews the main points to be considered in the design of discrete controllers for power electronics applications. It begins by addressing the aliasing in static converters resulted from the sampling of PWM harmonics and then points some limitations of digitally adjusted PWM. A procedure for the derivation of dynamic discrete models is presented and a review on the classical discrete design methods is presented. Finally, three examples are developed to illustrate how discrete controllers are becoming strong candidates to substitute the old analog counterparts.

II. SAMPLING AND ALIASING IN STATIC CONVERTERS

This section addresses the sampling approaches as well as the main issues associated with the aliasing and aliasing mitigation in static converters applications. Fig.1 shows a continuous variable and its sampled version.

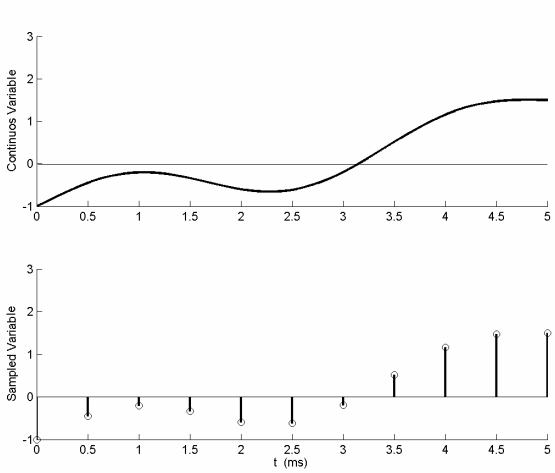


Fig. 1. Continuous and sampled signals. Top: $f(t)$. Bottom: $f^*(t)$

A sampled variable can be expressed as:

$$f^*(t) = f(t)\delta_T(t) = \frac{1}{T_s}[f(t) + 2\sum_{h=1}^{\infty} f(t)\cos(h\omega_s t)] \quad (1)$$

where $\delta_T(t)$ is unity impulse train that has the following Fourier series representation:

$$\delta_T(t) = \frac{1}{T_s}[1 + 2\sum_{h=1}^{\infty}\cos(h\omega_s t)] \cdot \quad (2)$$

There always a loss of information produced by sampling. However the extend of this loss depends on the sampling rate as well as in the sampling instants, since in static converters applications usually the sampling and the switching frequency are equal or related by an integer number. Let us illustrate the impact of the PWM harmonics on the sampled variables from the digitally controlled voltage fed full-bridge converter of Fig. 2.

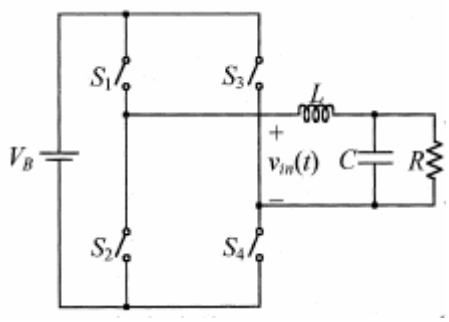


Fig. 2. Full-Bridge PWM converter.

It is considered that sampling frequency and the converter switching frequency are equal and the inductor and the

capacitor voltage are sampled at the zero and the peak of the triangular carrier used to generate the PWM signals. If the modulating signal is selected to result in half the dc bus voltage at the output the capacitor voltage can be expressed as:

$$v_c(t) \approx \frac{V_{cc}}{2} + V_h \cos(\omega_s t) \text{ and}$$
$$i_L(t) \approx \frac{V_{cc}}{2R} + I_h \sin(\omega_s t) \quad (3)$$

where V_h and I_h are the amplitude of the e high frequency components of the output voltage and inductor current resulted from the PWM. By substituting (3) into (1) the sampled voltage and current can be found as:

$$v_c(t)^* = \frac{1}{T_s}[\frac{V_{cc}}{2} + \frac{V_h}{2} + h.o.h]$$
$$i_L(t)^* = \frac{1}{T_s}(\frac{V_{cc}}{2R} + h.o.h) \quad (4)$$

From this example it is evident that the dc component of the sampled voltage has been corrupted since the high frequency component has been shifted to a constant due to the sampling. This phenomenon is known in the signal processing field as aliasing. However, the dc component of sampled current has been preserved after sampling. This is due to the fact that the current high frequency components cross zero at the sampling instants.

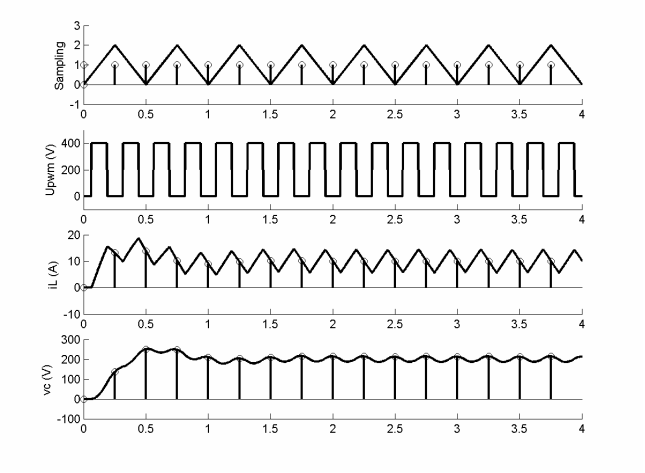


Fig. 3. Main waveforms of full-bridge converter dc-dc converter.

Undesired low frequency components due to aliasing can also be present in the sampled currents and voltages of sinusoidal PWM converters. To illustrate this, let us consider again the digitally controlled voltage fed full-bridge converter of Fig. 2, where the modulating signal now has been selected to produce a sinusoidal PWM pattern as shown in Fig. 4. In this case the PWM harmonics appears in the side bands of the switching frequency. After the sampling the harmonics in the side bands around the switching frequency of the voltage are shifted and appear as low frequency components corrupting the amplitude of the fundamental and introducing an undesired third harmonic in the sampled voltage as seen by comparing Fig. 5 and 6.

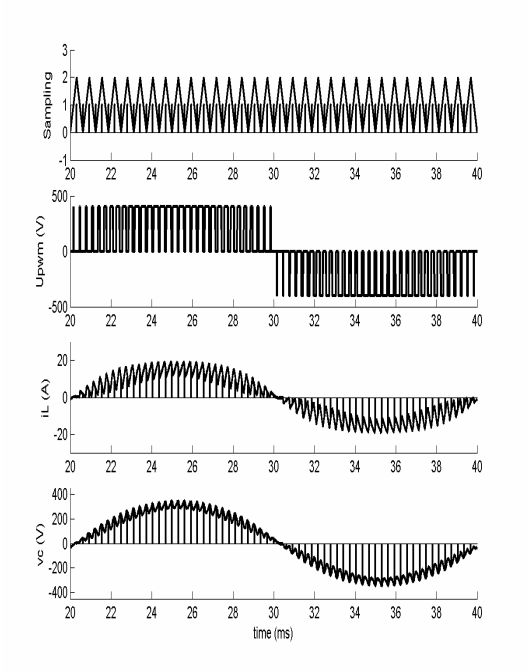


Fig. 4. Main waveforms of full-bridge converter dc-ac converter.

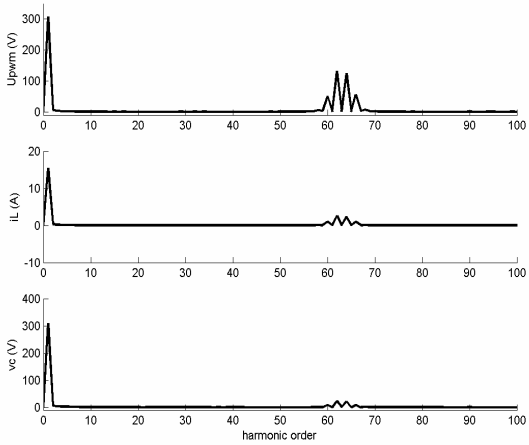


Fig. 5. Spectra harmonic of the continuous variables V_{cc} = 400V, L=3mH, C=5μF,R=20Ω, v_{ref}=311sin(2π50t).

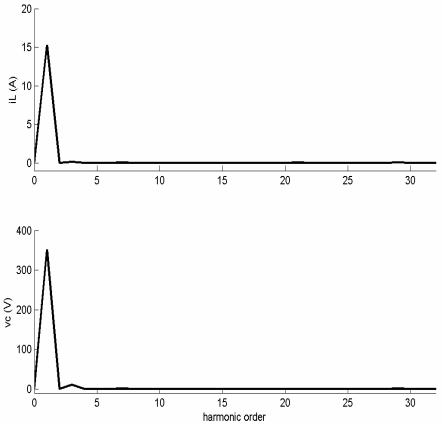


Fig. 6 Spectra harmonic of the sampled variables V_{cc} = 400V, L=3mH, C=5μF,R=20Ω, v_{ref}=311sin(2π50t).

In order to mitigate the undesired effects of aliasing one of the following measures can be taken:

(i) To use analog anti-aliasing low-pass filter before the sampling. This approach attenuates the high frequency content mitigating in this way its impact on the sampled variables low frequency range. These filters introduce additional dynamics in the loop and unusually a trade-off between closed loop bandwidth or stability margins and anti-aliasing performance should be considered.

(ii) To increase the sampling frequency and attenuate the PWM harmonics using digital filters. This approach usually requires a faster analog-to-digital converter as well as increases the computational burden for the implementation when compared with the analog anti-aliasing filter approach, but the reward is the improvement of the stability margins and the transient response. In [1] the PWM harmonics in a multi-sampling digitally controlled dc-dc converter are reduced using a repetitive controller. By making the sampling frequency *N* times the switching frequency it possible to reject the switching harmonics up to *N*/2 order for *N* even and (*N*-1)/2 for *N* odd. On the other hand, in [2] the average value of the state variables of three-phase PWM converter has been used for the implementation of a state feed-back controller. It is demonstrated in [3] that the low frequency components on the averaged sampled state variables are significantly reduced.

III. DIGITALLY ADJUSTED PULSE-WIDTH MODULATION DPWM

Unusually, an analog implementation of PWM is obtained by comparing a continuous modulating signal with a saw-tooth or triangular. Therefore, in an analog implementation there is virtually an infinity number of pulse widths that can be generated, in other words, there is no inherent limit on the possible pulse widths generated. Digitally adjusted PWM are usually implemented as peripheral of DSP and microcontrollers requiring a minimum of CPU burden. The three main blocks of a DPWM implementation are: (i) the time base counter; (ii) the compare logic unity; and (iii) the output unity that can include trip and dead-band actions. The switching frequency of the PWM is defined by the period of the time base counter which in turn depends on the counter clock frequency and counting mode, that is up-down or up mode. The compare unity continually compares the time base counter value with the content of the compare registers. Whenever there is a match between these values an event is generated. Then, the DPWM signals are generated from these events. Finally, the output unity can introduce dead-time in the DPWM signals that is usually required in voltage fed converters. Fig. 7 shows the main signals present in a DPWM implementation.

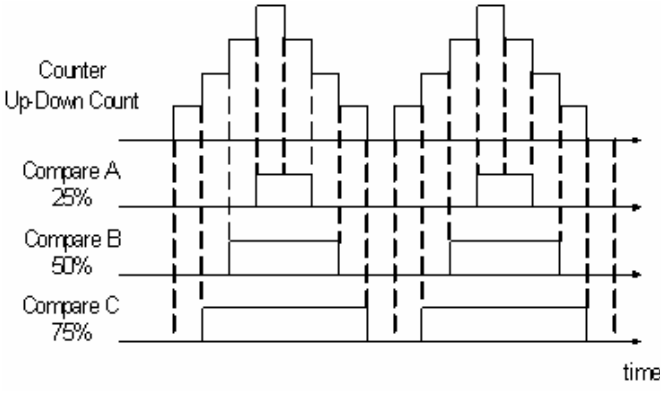


Fig. 7. DPWM main signals.

The resolution of DPWM of Fig. 7 can be defined as:

$$R = \log_2\left(\frac{f_{ck}}{2 f_{sw}}\right) \text{ (bits)}, \quad (5)$$

and in the case that the time base counter is set to operate in the up-mode of counting the DPWM resolution becomes:

$$R = \log_2\left(\frac{f_{ck}}{f_{sw}}\right) \text{ (bits)} \quad (6)$$

where f_{ck} is the time-base counter clock frequency and f_{sw} is the resulting DPWM switching frequency. For medium and high power converters that operate at low switching frequencies to limit the switching losses, there are available off-the-shelf microcontrollers and DSP controllers with high resolution DPWM. In this case a DPWM resolution greater than 10 bits are often achieved and the quantization effects of the DPWM usually are not a concern. On the other hand, to extend the benefits of digital control for switching mode power supply some obstacles must be overcome. Among them is the resolution of the DPWM. In SMPS the switching frequency is high to reduce the volume and size of the transformers and filters as well as to provide the desired transient response. As a result of the high switching frequency the resolution of the DPWM can be significantly reduced. Furthermore, since DPWM is part of the feedback loop, undesired steady-state limit cycles may arise. The minimum number of bits needed to avoid limit cycles due to the DPWM quantization resolution depends on the converter topology, the output voltage, as well as on the ADC resolution. Let us considerer a digitally controlled buck where the ADC input voltage range is from zero to converter input dc bus voltage. Then, if the DPWM resolution is less than the ADC resolution, it is possible that there will be no DPWM width that will produce an output voltage that maps into the ADC bin corresponding to the reference voltage. In this case the controller will oscillate causing an alternation between DPWM widths in an attempt to produce at the output the reference voltage. This alternation between DPWM widths are undesired since its frequency is difficult to predict and may result in additional EMI produced by the converter. Fig. 8 shows a block diagram of a digitally controller SMPS.

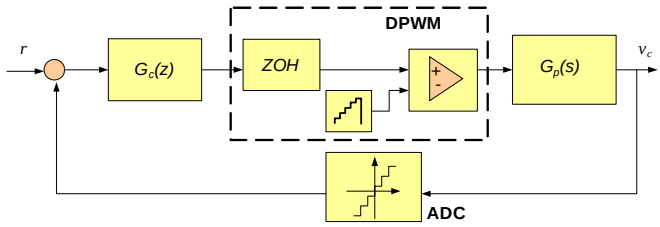


Fig. 8. Block diagram of digitally controlled buck converter.

As an example, let us consider that the closed loop digitally controller buck converter of Fig. 8 produces 1.5 V from a 5V dc bus operating with a switching and sampling frequency of 1MHz. It is assume that quantization effects of the digital compensator computation can be neglected, that is, sufficiently long words are used to compute the duty ratio. In addition, the ADC quantization resolution is assumed to be 8 bits. By using a 9 bits resolution DPWM the output voltage is as shown at the top of Fig. 9. However, if a 6 bits resolution DPWM is used, a steady-state limit-cycle can be observed at the output as seen in the waveform at the bottom of Fig. 9.

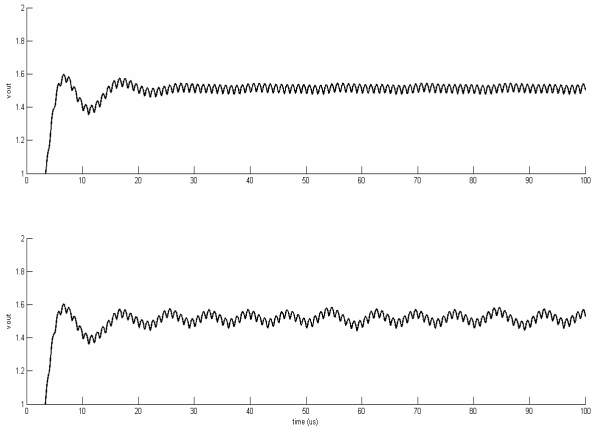


Fig. 9. Buck output voltage. ADC resolution R_{adc}=8 bits.
Top: DPWM with R_{pwm}=9 bits Bottom: DPWM with R_{pwm} =6 bit.

The first step toward eliminating limit cycles in digitally controlled SMPS is to ensure that the quantization voltage interval of the DPWM is finer than one of the ADC. If due technical or cost limitations the DPWM resolution could not be increased one of the following approaches can be used: (i) digital dither [4] (ii) sigma-delta modulation [5].

IV. DISCRETE TIME CONVERTER MODELING

Static converters are usually followed by low pass filters or by a plant with low pass characteristics. As a result, the high frequency harmonics associated with the PWM are significantly attenuated. In this context the control action produced by a discrete controller is usually transferred to the output of the converter assuring that the average value over the switching period is preserved by a PWM or Space Vector Modulation SVM. Let us considerer a voltage fed converter and assume that filter and load can be modeled by a continuous linear time invariant state space equation of the form:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} + \mathbf{F}\mathbf{w} \tag{7}$$

where **x** is the state vector, **u** is a vector that gathers the converter output voltages and **w** is a disturbance input vector. **A**, **B** and **F** are matrices the appropriated dimensions. The solution of this linear state space equation (7) can be expressed as:

$$\mathbf{x}(t) = e^{\mathbf{A}(t-t_o)}\mathbf{x}(t_o) + \int_{t_o}^{t} e^{\mathbf{A}(t-\tau)}\mathbf{B}\mathbf{u}(\tau)d\tau + \int_{t_o}^{t} e^{\mathbf{A}(t-\tau)}\mathbf{F}\mathbf{w}(\tau)d\tau$$

Usually in a discrete controller for static converters the control action is updated at regular intervals of time, synchronized with the switching frequency. In addition, since the PWM ensures that the desired average value over the switching period, and as the high frequency components are attenuated by the filter, it is reasonable to develop an average model for the purpose of the discrete controller design. To derive such a model the above equation will be solved along a sampling period, *T*, where the converter output voltage vector, **u**, and the disturbance vector, **w**, are assumed to be constant equal to their average values in the sampling interval. As a result, the above equation can be written as:

$$\mathbf{x}((k+1)T) = e^{\mathbf{A}T}\mathbf{x}(kT) + \int_{0}^{T} e^{\mathbf{A}(T-\tau)}\mathbf{B}d\tau\mathbf{u}(kT) + \int_{0}^{T} e^{\mathbf{A}(T-\tau)}\mathbf{F}d\tau\mathbf{w}(kT)$$

Due to the low pass characteristic of the filters found in static converters, often the output variables can just be expressed as a function of the state, as a result the following discrete state space equation describes the average dynamic behavior of converter in the discrete time domain.

$$\begin{aligned}\mathbf{x}((k+1)T) &= \mathbf{G}\mathbf{x}(kT) + \mathbf{H}\mathbf{u}(kT) + \mathbf{F}\mathbf{w}(kT)\\ \mathbf{y}(kT) &= \mathbf{C}\mathbf{x}(kT)\end{aligned} \tag{8}$$

where the **G**, **H** and **F** are matrices given by:

$$\mathbf{G} = e^{\mathbf{A}T}, \qquad \mathbf{H} = \int_{0}^{T} e^{\mathbf{A}(T-\tau)}\mathbf{B}d\tau, \quad \mathbf{F} = \int_{0}^{T} e^{\mathbf{A}(T-\tau)}\mathbf{F}d\tau$$

It is desirable that the qualitative properties, of such as the controllability, of the continuous equation (7) be preserved after the discretization. The next theorem gives the necessary and sufficient condition to preserve the controllably after sampling for SISO systems.

Theorem 1

Assume that a SISO dynamic equation (7) is controllable. The necessary and sufficient condition for the discrete-time dynamic equation (8) to be controllable is that $Im[\lambda_i(\mathbf{A})-\lambda_j(\mathbf{A})] \neq 2\pi\delta/T$ for $\delta = \pm1,\pm2,\ldots$ whenever $Re[\lambda_i(\mathbf{A})-\lambda_j(\mathbf{A})] = 0$.

The proof of this theorem is found in [6].

If the input-output dynamic description of the converter is required for the analysis or the design, then it can be easily found by taking z-transform of the discrete state space equation above and expressing the output **y** as a function of the input **u** and the disturbance **w** that is:

$$\begin{aligned}\mathbf{y}(z) &= \mathbf{C}(z\mathbf{I}-\mathbf{G})^{-1}\mathbf{B}\mathbf{u}(z) + \mathbf{C}(z\mathbf{I}-\mathbf{G})^{-1}\mathbf{F}\mathbf{w}(z)\\ \mathbf{y}(z) &= \mathbf{G}_u(z)\mathbf{u}(z) + \mathbf{G}_w(z)\mathbf{w}(z)\end{aligned} \tag{9}$$

Note that $\mathbf{G}_u$ and $\mathbf{G}_w$ are matrix transfer functions whose elements are rational functions of the complex variable z.

Once the discrete dynamic has been derived the next step is the analysis and the design.

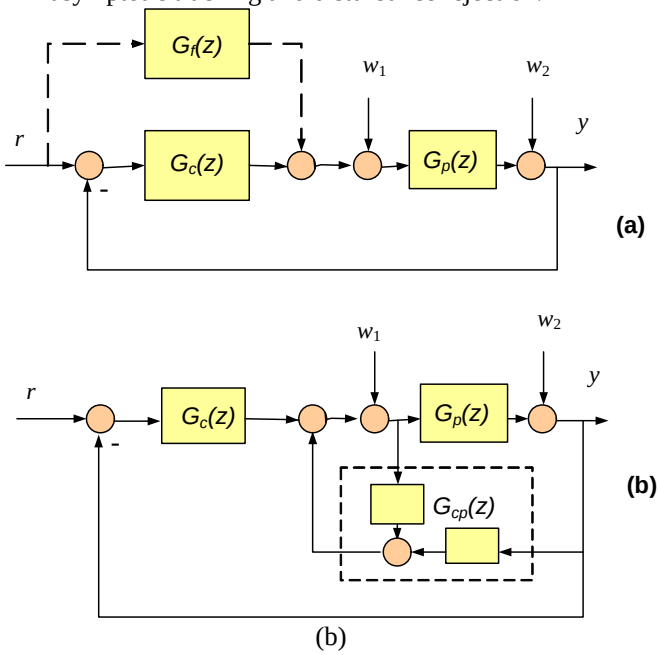
V. DISCRETE TIME CONVERTER CONTROL DESIGN

A. Controller Architectures and Steady State Performance

The control law implementations shown Fig. 10 are generally suitable to solve power electronics control problems. In Fig. 10a the feedforward controller $G_f(z)$ alone can not provide robust reference tracking, however it has been found that it can improve the transient response due to reference changes. In Fig.10b the transfer function $G_{cp}(z)$ can represent, for instance, an estimate state feedback that is introduced to stabilize or to allocate the poles of the plant. The controller $G_c(z)$ can be selected to provide the desired steady-state performance while ensuring the stability of the overall system. The internal model principle [11] gives us some guide lines for the selection of $G_c(z)$. The internal model principle for SISO discrete systems can be summarized by the next theorem [10].

Theorem 2:

Let us consider the feedback system of Fig.10a where the plant is completely characterized by the strict proper transfer function $G_p(z)=N(z)/D(z)$. Let $\phi(z)$ be the least common denominator of the unstable poles of the reference r and the disturbances w. If none of the roots of $\phi(z)$ is zero of $G_p(z)$, then there exist a compensator $G_c(z)$ with a proper transfer function such that the feedback system of Fig. 10a is stable and it can achieve asymptotic tracking and disturbance rejection.



(b)

Fig. 10. Controller Architectures.

The usual form of the controller is $G_c(z)=N(z)/\phi(z)$, however some implementations standout in power electronics applications. For instance, the repetitive controller [12],[2] does not require a significant effort for its implementation and has low sensitivity to quantization errors. As a result, it has been used in many power electronics applications [13-15]. The most popular repetitive controllers are given in rows one, two and three of Table I. The conventional PI controller is shown in row four of Table I. Finally, the proportional resonant controller [16] is given in the row 5 of Table I. The proportional resonant controller has recently been considered for many power electronics applications where it is desired to track a sinusoidal references or where it is desired to reject a disturbances of known frequencies.

Table I
Internal Mode Controllers

	$\frac{N(z)}{\phi(z)}$	*Poles*
1	$\frac{kz^d}{z^N-1}$	At odd and even harmonics,
2	$\frac{kz^d}{z^{\frac{N}{2}}+1}$	At odd harmonics
3	$\frac{kz^d}{z^{\frac{N}{2}}-1}$	At even harmonics and at z=1
4	$Z\left\{k_p+\frac{k_i}{s}\right\}$	At z=1
5	$Z\left\{k_p+\sum_i \frac{k_i s}{s^2+\omega_i^2}\right\}$	At $z=e^{\pm j\omega_i T}$

N is number of samples in the fundamental period.

Once the controller architecture is defined the next step is the controller parameters design.

B. Root-Locus Method

If the discrete transfer-function of the converter has been derived then the discrete controller design can be carried out using the root-locus approach. It is important to note that the rules for the construction of root loci of the z-transfer functions are identical to those of continuous systems. The conditions for absolute and relative stabilities for the discrete systems on the z-plane are conformal to those for the continuous-data systems on the s plane. Let us consider a SISO closed loop system with a proper open loop transfer function $GH(z)=\frac{KN(z)}{D(z)}$ where $N(z)$ and $D(z)$ are coprime. The closed loop system characteristic equation is:

$$D(z)+KN(z)=0 \text{ or } \frac{KN(z)}{D(z)}=-1 \qquad (10)$$

Note that the stability and the modes of the closed loop system are defined by the roots of the characteristic equation. Let us assume that K is positive, then all points in the z plane that satisfy the angle condition

$$\arg\left(\frac{N(z)}{D(z)}\right)=-(2k+1)\pi \quad \text{for } k=0,\pm1,\pm2,... \qquad (11)$$

are root of the characteristic equation for some gain K. The root loci departure with K=0 from the roots of $D(z)$ and arrive at the roots of $N(z)$ or tend asymptotically to infinity as $K\to\infty$. In order to ensure the stability of the closed loop system the roots of the characteristic equation must be inside the unit circle in the z-plane. In addition, a set of constant damping factor lines, that are logarithmic spirals, and natural

frequencies are drawn within the unit z-plane to help to characterize the modes of the closed loop system. As an illustrative example, let us consider the discrete controlled voltage fed grid connected PWM converter with *LCL* filter described in [9]. The open loop transfer function in this case can be expressed as:

$$GH(z) = \frac{KN(z)}{\phi(z)} G_p(z) \qquad (12)$$

where $G_p(z) = C(zI - (\bar{G} - \bar{H}K))^{-1}\bar{H}$ which represents the transfer-function of *LCL* filter with a partial state feedback and $\frac{KN(z)}{\phi(z)} = KZ\left\{\sum_i \frac{s}{s^2 + (\omega_i)^2}\right\}$ is an internal model controller to achieve reference tracking and disturbance rejection. From the Root Loci of Fig. 11 it is possible to see how the high and low frequency poles of the closed loop system changes with the internal mode controller gain, *K*.

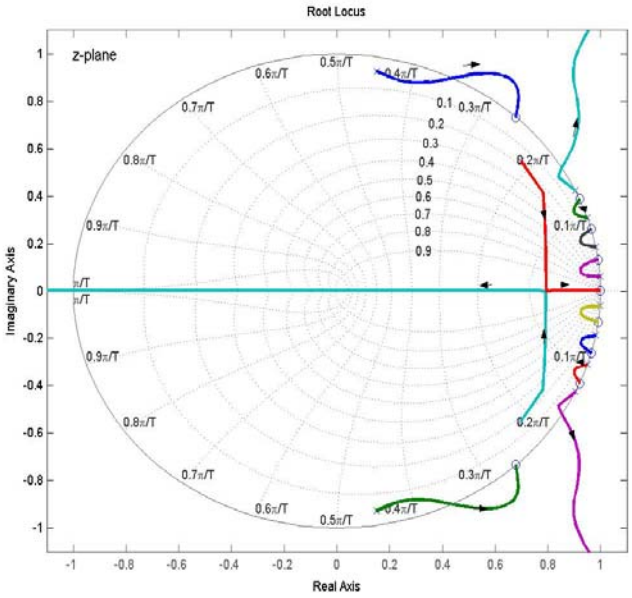


Fig. 11. Root-Loci of a discrete controlled grid connected VSC with *LCL* filter with an internal mode controller with complex po at first, third, fifth and seventh harmonics.

In this case, the root locus method is an invaluable tool develop intuition on the impact of the internal moc controller gain on the closed loop modes.

C. Frequency Response Methods

Frequency response methods, such as Bode Pl Nichols Chart and Nyquist Stability Criterion can be used the analysis and design of discrete controller for sta converters. It is important to keep in mind that wh performing frequency response tests the aliasing should avoided. Let us assume that discrete transfer-function *GH* is given, then a straightforward way to obtain the bo magnitude and phase angle plots are by computing t magnitude and phase of *GH*(z) with $z = e^{j\omega T}$ where sweeps over the interest frequency range. The Nyqu stability criterion for discrete systems is similar to the one for continuous systems, and it is also derived according with the principle of the argument of the complex-variables theory. For the Nyquist path of Fig. 12 , if the open loop transfer-function *GH*(z) is stable except for the poles on the unity circle, which usually is the case in static converters applications, then the number of zeros of the characteristic equation outside the unity circle, that is, the number of closed loop unstable poles, is equal to the number of times the point (-1,j0) of *GH*(z) plane is encircled by the Nyquist plot of the *GH*(z) corresponding to the path of Fig.12.

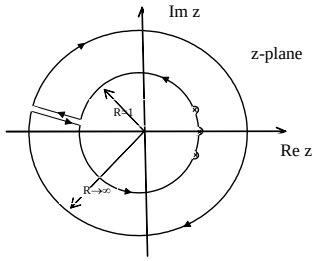


Fig. 12. Nyquist path that encloses the exterior of the unit circle.

Let us consider again the discrete controlled voltage fed grid connected PWM converter with *LCL* filter described in [9]. The open-loop frequency response with a gain *K*=100 is shown in Fig. 13. It is important to mention that the gain and phase margins can be easily obtained from the Nyquist plot as shown in Fig.14. Another important point to be mentioned, is that, in these frequency plots a damping-ratio has been introduced in the complex poles of the internal mode controller, that is ζ=0.01. This brings a number of benefits that are: (i) it increases the robustness of the systems; (ii) reduces the dynamic range of the variables in the implementation, (iii) it simplifies the Nyquist path by avoiding the use of semicircular detours about the poles on the unit circle. However, the damping-ratio should be kept as small as possible otherwise the steady state performance in terms of reference tracking and disturbance rejection can be compromised.

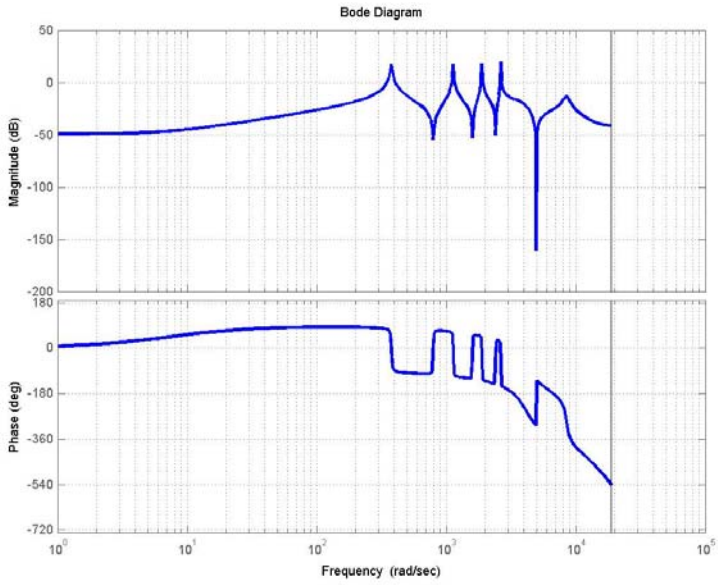


Fig. 13. Open loop frequency response discrete controlled VSC with *LCL* filter [9]. *K=100*.

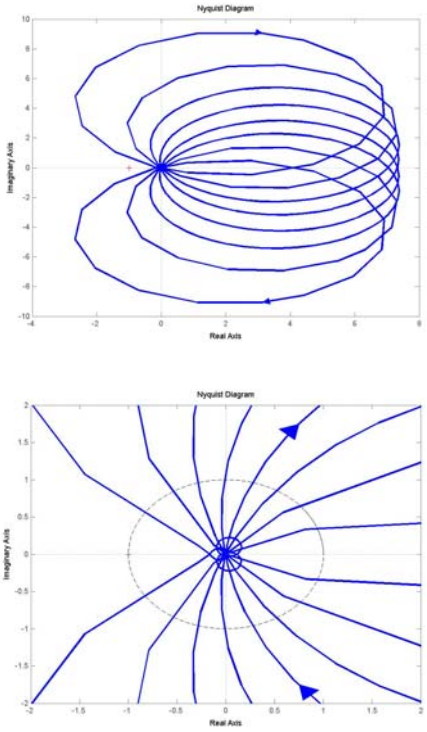


Fig. 14. Top: Nyquist plot for the frequency response discrete controlled VSC with *LCL* filter [9]. Bottom: Zoom of the Nyquist plot at the top.

VI. EXAMPLES OF DISCRETE CONTROL OF STATIC CONVERTERS

This section presents three examples of discrete controllers for static converters.

A. Interleaved PFC Converter

In [17] a discrete controller for three-level boost power factor corrector rectifier has been proposed, Fig 15.

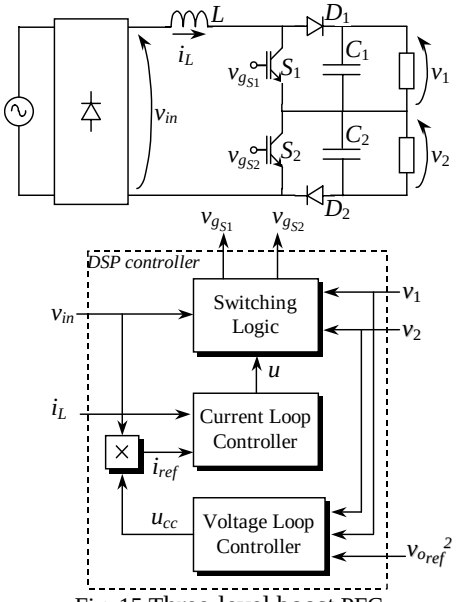


Fig. 15 Three-level boost PFC.

In continuous conduction mode the three-level boost converter has four stages of operation. A control mechanism to balance the capacitor voltages is proposed and a discrete model for the boost inductor current has been derived, that is:

$$i_L(k+1)=\begin{cases} i_L(k)+\dfrac{v_{in}(k)T}{L}-\dfrac{v_o(k)T}{2L}+\dfrac{v_o(k)u(k)T}{2L}, & \text{if } v_{in}<v_1 \\ i_L(k)+\dfrac{v_{in}(k)T}{L}-\dfrac{v_o(k)T}{L}+\dfrac{v_o(k)u(k)T}{L}, & \text{if } v_{in}>v_1 \end{cases} \quad (13)$$

Since most DSP controllers and microcontrollers have multiplication in their instruction sets, it has been proposed the following linearization law:

$$u_L(k)=\begin{cases} \dfrac{v_{in}(k)T}{L}-\dfrac{v_o(k)T}{2L}+\dfrac{v_o(k)u(k)T}{2L}, & \text{if } v_{in}<v_1 \\ \dfrac{v_{in}(k)T}{L}-\dfrac{v_o(k)T}{L}+\dfrac{v_o(k)u(k)T}{L}, & \text{if } v_{in}>v_1 \end{cases} \quad (14)$$

As a result, the boost inductor current can be expressed by the following LTI equation:

$$i_L(k+1)=i_L(k)+u_L(k). \quad (15)$$

From this point a number of control laws could be used. There the authors selected to design the controller in the state space framework. A servo controller with estimated state feedback has been adopted, see Fig. 16. Among the motivation to use such approach are: (i) the gains of the controller are obtained using a systematic procedure, that is DLQR and, (ii) the implementation delay has been compensated by using and predictive state observer. Experimental results demonstrate the good performance and feasibility of the proposed discrete controller.

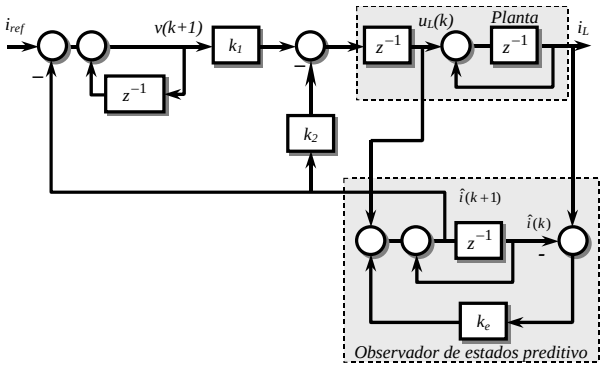


Fig. 16. Block Diagram of a discrete controller for three-level boost power factor corrector rectifier.

B. Single-Phase Inverter

In [18] it is proposed a model reference controller combined with a repetitive controller for single phase UPS, Fig. 17. The model reference controller modifies the structure of the plant so that the closed-loop transfer function becomes equal to a chosen reference model transfer function, whereas the repetitive control action minimizes periodic distortions caused by non-linear load, Fig. 18. An interesting feature of this combination is that the design parameters of the model reference controller can be tuned a priori from simulation of the discrete RMRAC using a modified least-squares adaptation algorithm. The stability analysis reveled that the converter is stable for a large range of load and filter parameters. Experimental result of Fig. 19 illustrates the good performance of the system even under heavy non-linear load.

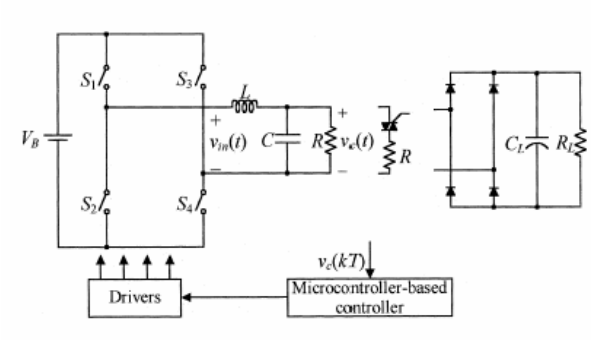


Fig. 17 : Digitally controlled voltage-source PWM inverter.

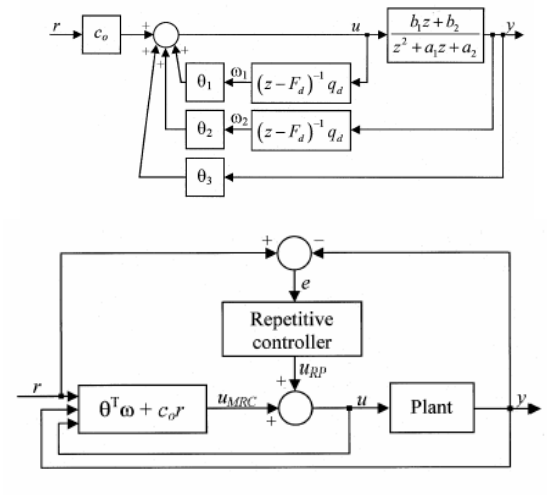


Fig. 18 : (a) Block diagram the model reference controller. (b) Block diagram MRC plus RP controller.

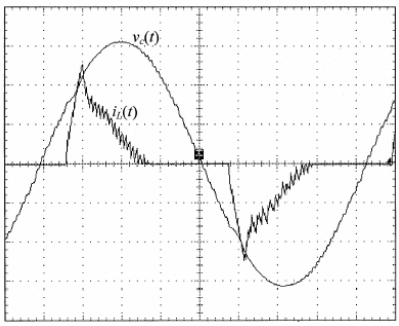


Fig. 19: Output voltage vc(t) (50 V/div) and load current i(t) (10 A/div) fora rectifier-RC load. Time scale: 2 ms/div.

C. Three-Phase UPS with Output Transformer

In [19] a down-sampled discrete-time internal-model-based controller in the synchronous reference frame with a reduced number of poles has been proposed for three-phase inverters with output transformer used in double-conversion uninterruptible power supply, Fig. 20. There, it was demonstrated that the use of a down-sampled rate and fewer poles in the internal model results in a number of benefits, among which are the following: (i) improvement of the transient response; (ii) increase of the stability margin of the closed-loop system; (iii) a straightforward implementation in fixed-point digital signal processor and microcontroller implementation as well as a reduction of the required memory space; and (iv) a simple solution for the saturation of the output transformer. As a result, it was possible to obtain output voltages with reduced total harmonic distortion while ensuring good transient performance for both linear and nonlinear loads.

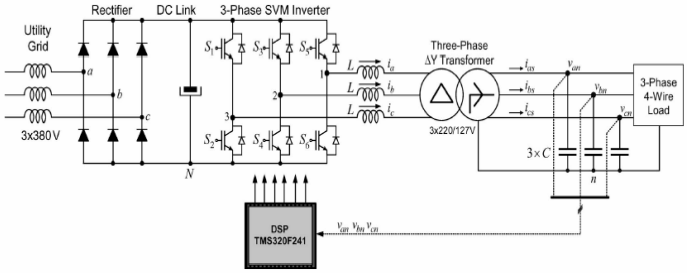


Fig. 20. Discrete Controlled Three-phase PWM inverter, ΔY transformer, filter, and load.

Fig. 21 shows the block diagrams the multi-rate controller. By selecting a smaller sampling frequency of the internal model controller it has been possible to increase the phase margin as shown in Fig. 22. Finally, Fig 23 demonstrates the good performance of the multi-rate controller even under heavy three phase non-linear load.

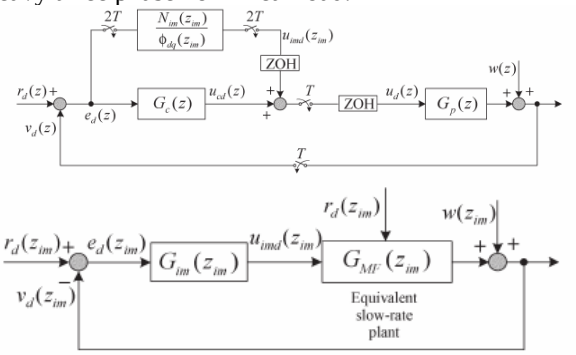


Fig. 21. Block Diagrams of the discrete-time voltage controller in synchronous frame for axis "d." $z = e^{Ts}$ and $z_{im} = e^{Tim\,s}$.

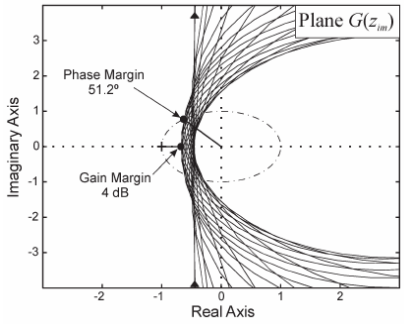


Fig. 22 Nyquist plot of $G(z_{im}) = G_{im}(z_{im})G_{MF}(z_{im})$. $N = 42$, and $T_{im} = 396.82$ µs.

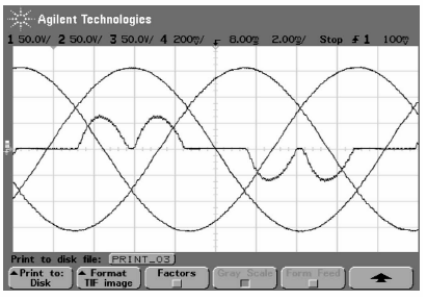


Fig. 23. Experimental result. Load:Three-phase uncontrolled rectifier at 10 kVA. Output phase-to-neutral voltages v_{an}, v_{bn}, and v_{cn}, and load current i_a. THD = 0.8%. Voltage scale: 50 V/div. Current scale:20 A/div.

VII. COMMENTS

In this paper the main issues associated with the analysis and design of discrete controllers for power electronics converters have been addressed. It is important to note that some popular discrete controllers often found power electronics applications have not been mentioned due to the space restriction. Among them is the dead-beat controller [20-22]. Although deadbeat controllers provide minimal time responses and they are simple to implement one should keep in mind that their performance and stability are strongly depend on the knowledge of the systems parameters. On the other side of the controller approach spectrum are the self-tuning and adaptive controllers that usually requires a significant computational burden for their implementations but they make it possible to ensure stability and performance even in the presence of the unavoidable uncertainties associated with a real implementation. As the DSP controllers and microcontrollers manufactures improve the performance of the their processors, as well as reduce their prices, the power electronics applications can benefit from the use of these advanced control methods.

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