IMPLEMENTATION OF THREE-PHASE ACTIVE FILTER FOR COMPENSATION OF HARMONICS AND DISPLACEMENT WITH PHASES CURRENT BALANCING

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Abstract – **Present paper deals with the implementation of parallel three-phase active power filter used to compensate current harmonics, to correct the displacement between voltage and current generated for capacitive or inductive loads and, by the implementation of the control strategy here described, to perform the current balancing for the three phases, minimizing the neutral current. The reasons for the choice of this topology and the adopted control strategy are presented as well as the mathematical analysis, design procedures, simulation and laboratory results. As final stage of the developing a prototype with 10 kW was built.**

Keywords – **Harmonic distortion, active filter, voltage control, inverters, digital control.**

I. INTRODUCTION

Active filter technology consist of measuring harmonic currents of one or more phases of the power grid and generate all harmonic currents components in opposition of phase in relation to those measures.

Active power filters are already used with success for consumers and suppliers of electric energy in many countries. In [1] is shown about use of incorporated active power filters, for the proper manufacturers, the equipment that traditionally originates great harmonic currents. The active power filters can be parallel or series [2, 3, 4]. Filters series are voltage restorers, have the function to eliminate distortions in the voltages of the electrical system. Parallel active filters are current restorers, have the function to eliminate the harmonic currents components. There are also the hybrid filters, that combine the two functions [2, 3]. This work deals with solely the parallel filters, which operate as currents sources in derivation with the electrical system. Its function is to inject in the point of connection of the electrical system with the load (PAC), currents of compensation capable to attenuate or to eliminate harmonic currents originated by non linear loads.

In the described configuration of this paper, the parallel active power filter is capable to inject current in the PAC or to remove current from load to the capacitive bank, since the structure is bidirectional.

II. CONVERTER TOPOLOGY

The inverter used in this project is a voltage fed inverter. Considering the possible topologies for the voltage inverter there are the three legs inverters and the four legs inverters. Fig. 1 illustrates as the second type.

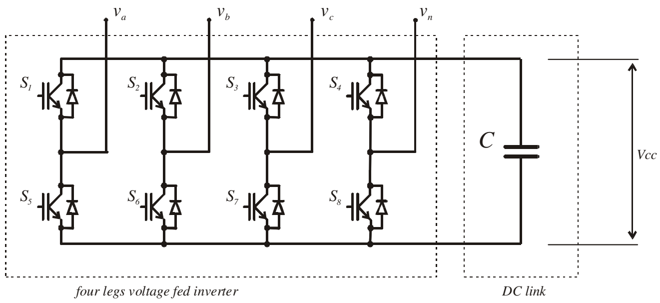

Fig. 1: Voltage fed inverter with four legs.

In [5] can be found a lot of techniques of modulation for these structures. Inverter of three legs is appropriate for balanced three-phase systems, where the voltages supplied for the inverter and currents demanded for the load are balanced. Is possible to use this topology in systems unbalanced through the addition of a neutral conductor to the center of the continuous voltage side (splitting the DC link of Fig. 1 in two capacitors), however this can cause problems of control and stability, a time that is necessary to carry through the balancing of the voltages over the two capacitors in DC link. Moreover, the neutral currents are drained or injected directly in the capacitors, what it requires high values of capacitances. Another disadvantage of this converter, when used with the neutral conductor, is the poor use of the voltage in DC link [6]. The inverters with four legs are not so known, however comes being pointed as the topology most appropriate with respect to applications in unbalanced systems [7]. The existence of an exclusive leg for the neutral conductor becomes possible the independent control of the current of neutral supplied by the inverter. Moreover, the inverter does not require the addition of a conductor to the DC link (continuous voltage), what it means that the capacitor will not be connected directly to the neutral conductor. This becomes possible to reduce the value of the capacitance and still it excuses the necessity of a controller to carry through the balancing of the voltages. A system of current control with this inverter is more robust of what its competitor with three legs.

III. CONTROL STRATEGY

Most part of technical literature about active filters deals with solely its application in balanced three-phase systems. However, the number of electric installations that have a neutral conductor with current phases unbalanced is increasing, which are mainly caused by the significant single-phase load presence [1]. The filter is connected to the electric installation through coupling inductors, for which they circulate currents synthesized for the current controllers, characterizing the active filter as controlled current source. The strategy to produce the correct control is composed two-piece basic: a system of identification of the references and a system of current control (Fig. 2).

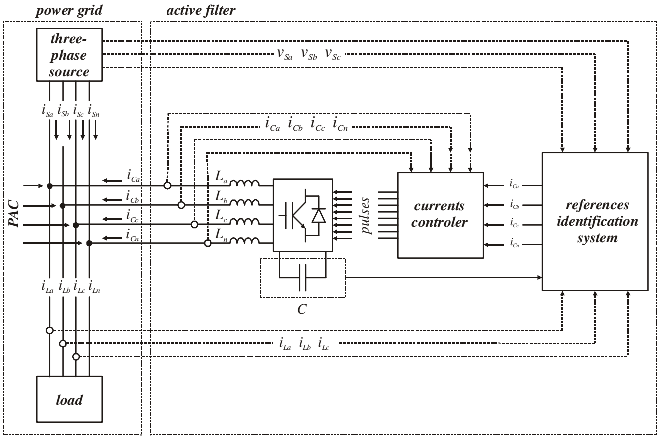

Fig. 2: Control strategy of for active filter.

The function of the references identification system is to determine the compensation currents that must be injected by the active filter in the electrical system. When the active filter is used in systems unbalanced with neutral, the compensator has still the function to determine the compensation currents that become possible the balancing of the phases and the elimination of the neutral current.

A. Current references generation strategy

To reach the proposed objectives of this work was used a compensation strategy based on the sinusoidal currents synthesis, balanced and in phase with the three fundamental grid voltages. This will ensure a current in the PAC with low distortion harmonic and high power factor, additionally minimizing the neutral current.

The synthesis of the filter currents is originated in a PLL (Phase-Locked Loop) that produces three sinusoidal references that are in phase with the three phase voltages, from a grid voltage sample. This PLL is implemented in the DSP program and has the as advantage do not to suffer external interferences that can be there in the grid voltages.

After the PLL references the signal is applied on the proportional and integral controllers (PI) that produce the final signal to a pulse width modulator. The Fig. 3 shows the simplified block diagram of a system of current control. Rigorously each one of the proportional and integral regulators receives the name from controller, but the name of current controller will be given to the complete system, simplifying the adopted nomenclature.

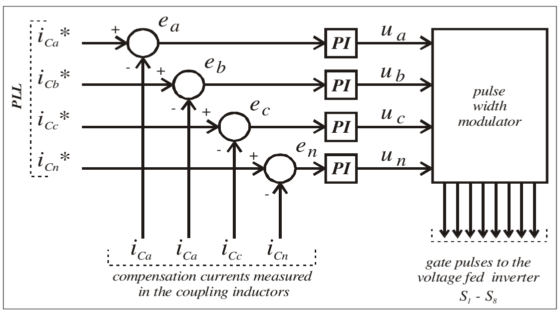

Fig. 3: Current controller of the active filter.

In the block diagram of Fig. 3 four controllers PI exist which generate references currents for a pulse width modulator. This modulator generates the pulses for inverter firing used for the synthesis of current compensation. The voltages signals are generated by controllers PI basing on the errors between measured and reference currents.

These signals are applied the switch of the inverter, in this in case that, IGBT transistors. The system operates in closed loop looking for to do with that the currents in the inductors are next possible to reference currents. Controllers PI operate in the intention to minimize the errors between the references and effectively synthesized currents in the *La* to *Ln* inductors (Fig. 2). In this paper the control of the filter was implemented digitally in processor DSP TMS320F2812, manufactured for the Texas Instruments. Fig. 4 shows more detailed strategy of implemented control in the DSP. The control strategy must synthesize a current (i_F) in the output of the filter, that assures low distortion the current (i_S) in the PAC, considering that the load current (i_C) has distortion of up to 50%. To keep high factor of power, the voltage signal in the PAC is used as reference. The voltage in capacitor C of the inverter is monitored to guarantee the system power balancing.

IV. MATHEMATICAL ANALYSIS

Mathematical analysis contemplated all the procedures for implementation of the control of the three-phase inverter of four legs operating as active filter of harmonics. The requirements of harmonics attenuation until 21st order, reduction of the neutral current (unbalance between the phases) and reduction of the displacement between voltage and current in the three phases had been the main considerations in the design. In the filter, two controllers PI are used: current controller PI of fast response and controller PI of DC link, of slower response. Controller PI of DC link was calculated in function of the described parameters below:

- Value of the DC link capacitor;
- Value of the rms phase voltage;
- End of scale of the sensors of DC link voltage and alternated voltages;
- Value of voltage desired in DC link;
- Analogical-digital converter gain;

Considering the bidirectional inverter for balanced loads, the DC link voltage it must be bigger that the value of line voltage peak. In such a way, to assure the synthesis of the current in the filter, the DC link voltage (V_{DC}) must be 3/2 greater that the peak of the maximum rms phase voltage (Va) [8], that is:

$$V_{DC} \geq \frac{3}{2} Va\sqrt{2}\sqrt{3} \qquad (1)$$

A. DC link Capacitor

The DC link capacitor is responsible for some specific characteristics, such as: to assist in the balance of energy in conditions of transitory in the load, to guarantee one high rate of variation of the output current inverter and, to make possible the current circulation of negative sequence for the inverter. In the case of the topology adopted for the inverter (4 legs), the currents of zero sequence are manipulated by the fourth arm, making that the DC link voltage will be influenced only from the harmonics and components of negative sequence, especially in the basic frequency (bigger power). It is considered that the voltages of the three-phase power grid are balanced and that the fluctuation of DC voltage (ΔV_{DC}) is lesser the total value of DC link voltage ($\Delta V_{DC} << V_{DC}$), where ΔV_{DC} is peak of the DC voltage ripple. The parcel most significant of this ripple is proportional to the oscillation of power in the inverter, which had to currents of negative sequence:

$$P_{neg} = \begin{bmatrix} v_{an} & v_{bn} & v_{cn} \end{bmatrix} * \begin{bmatrix} il_{aneg} & il_{bneg} & il_{cneg} \end{bmatrix} \cong \tilde{P}_{cc} \qquad (2)$$

From (2) it is possible to show that the power of negative sequence has oscillatory characteristic in 2ϖ and can be written as:

$$P_{neg} = \frac{3}{2} Va\sqrt{2} \cdot I_{neg\_pk} \cos(2\varpi t + \phi) \qquad (3)$$

where: I_{neg_pk} is the peak value of negative sequence current, which if desires that to the active filter support. Therefore, the fluctuation of energy peak-peak (ΔE_{pp})provoked by the load is:

$$\Delta E_{pp} = \frac{3Va\sqrt{2} \cdot I_{neg\_pk}}{2\varpi} = \frac{1}{2} C(V_{DC} + \Delta V_{DC})^2 - \frac{1}{2} C(V_{DC} - \Delta V_{DC})^2 = 2C \cdot V_{DC} \cdot \Delta V_{DC} \qquad (4)$$

In such a way, the minimum capacitor to get value for ΔV_{DC} , is:

$$C_{\min} = \frac{3 \cdot Va\sqrt{2} \cdot I_{neg\_pk}}{4\varpi \cdot V_{DC} \cdot \Delta V_{DC}} \qquad (5)$$

B. Coupling inductors design

Coupling inductors, between the inverter and the power grid, must operate in a big band of frequencies, what it must be considered in the design for definition of the constructive characteristics of the inductor and the core material. The specification of the inductance value is made to satisfy criteria and specific functions, such as: to limit the current ripple in the output of the converter, being operated as first-class filter pass-low, without provoking a drop of voltage exaggerated on its terminals. Additionally the inductor does not have to limit the rate of variation of the converter current, what it would limit the performance of the active filter for compensation of harmonic currents of higher order. It must have a commitment between the DC link voltage and the value of the inductor. High values of voltage make possible to get high *di/dt* to cancel the harmonics completely, however this also causes values raised for the current ripple. A chosen time the voltage, must be proceeded to the calculation of the coupling inductors. Diverse papers as [9, 10, 11], establish criteria for the calculation. Thus according [12], the rate of rising (*di/dt*) of the current generated for the active filter must be bigger of what the rate of harmonic currents rising of the load. Considering the Kirchhoff´s Voltages Law, for one of the phases of the system (Fig. 2 and 3), it results:

$$-\sqrt{2}\sqrt{3} \cdot Va - 2La\left(\frac{di}{dt}\right) + V_{DC} = 0 \qquad (6)$$

Soon, a time that if desires that the inductance value allows that the rate of variation of the current of the active filter (*di/dt*), either bigger of what the rate of variation of harmonic currents of the load, becomes:

$$La = \frac{V_{DC} - \sqrt{2}\sqrt{3} \cdot Va}{2\dfrac{di}{dt}} \qquad (7)$$

C. Voltage and current PI controllers

As much for the project of the current controller, how much for the one of voltage, the system is considered according Fig. 4.

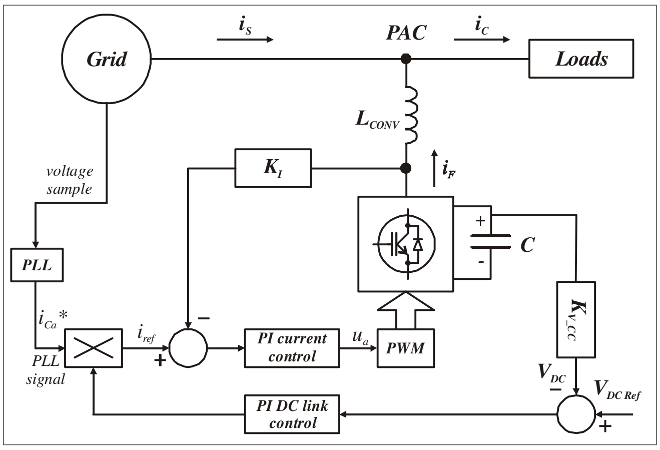

Fig. 4. Block diagram to use in voltage and current controller design.

As it does not have power plant in capacitor C, the system must observe and keep constant this voltage. It is necessary also that the output current of the filter synthesizes the references defined for the compensation strategy. Thus the system can be configured as two subsystems of control: one for the voltage in C and another one for output harmonic currents. It is noticed that the controller of the voltage of capacitor C is responsible for modulating the value of the current reference of the active filter, to keep fixes this voltage. In such a way, the transfer function of the physical system of the voltage control can be represented by the capacitive function $1/sC$, while the transfer function of the system of control of the output current is given by the function $1/sL_{conv}$ [13]. Additionally the gains of the voltage sensors and current must be considered. Finally, depending on the technique of adopted modulation the gain of converter PWM is defined. In the case of the used three-phase inverter, modulating set PWM - converting it is understood, of the point of view of control, as a voltage gain equal to:

$$K_{PWM} = \frac{V_{DC}}{2} = 250 \qquad (8)$$

Fig. 5 illustrates the used basic project for the design of the current controller. It is observed that the current in the output of the active filter is converted in voltage and scaled through the current sensor (block K_{si}) and the conditioning board. To follow then it is converted by A/D converter (block K_{DSP}) into p.u. (per unit) scale.

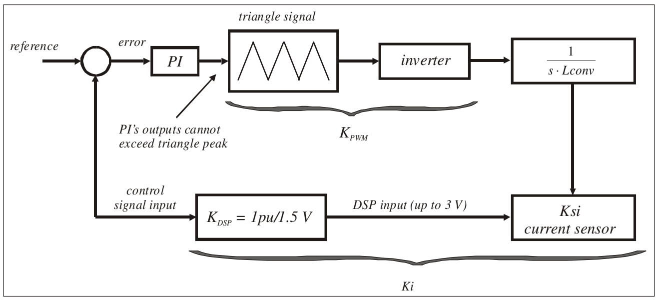

Fig. 5. Blocks diagram of the plant with the current controller.

Considering this design, the transfer functions without (G_{SC}) and with (G_{DC}) controller PI, are express, respectively for:

$$G_{SC}(s) = K_i K_{PWM} \frac{1}{sL_{conv}} = \frac{\varpi_{SC}}{s} \quad (9)$$

$$G_{DC}(s) = G_{SC}(s) PI(s) = \frac{\varpi_{DC}}{s} \quad (10)$$

Soon it is possible to calculate the proportional gain (K_p) and integral gain (K_i) of regulators PI through [14]:

$$K_p = \frac{\varpi_{DC}}{\varpi_{SC}} = \frac{f_{DC}}{f_{SC}} \quad (11)$$

$$K_i = \frac{K_p \varpi_{DC}}{\tan(mf)} T_a \quad (12)$$

where f_{DC} is the frequency of the broadband in Hz and mf is the phase margin stipulated for the system in closed loop with regulator PI. T_a is the period of sampling of the digital system. In general, the band-pass of the current controller of an active filter cannot be low to disable the synthesis of harmonic currents necessary, nor high to become the unstable system or to exceed the criteria of Nyquist stability. How much to the phase margin values between 70º and 85º had been kept.º.

D. DC voltage controller

Considering that the dynamics of the voltage of DC link of the inverter is sufficiently slow, it is relatively easy to get a controller PI who satisfies the conditions of dynamics and stability. The calculation of the gain of the converter seen for the voltage controller is made by the balance of power of the converter. Operating as parallel active filter in condition of steady state the converter does not have to absorb nor to deliver active power. That is the calculated active power in side AC of the converter must be the same one of that one calculated of side DC. In such a way the gains of the PI can be calculated by similar expressions to those used for the current control.

V. DESIGN PROCEDURE

In this section the basic criteria for the dimensioning of the components of the parallel active filter are exposed. The conditions where the active filter is used and that type of load the same is capable to compensate are described. The system is three-phase with neutral conductor. The voltage of phase V_a = 127 V and 60 Hz frequency. The nonlinear loads produce currents with up to 50% of harmonic distortion and unbalance of negative sequence. The loads present a power about 10 kVA, what it results in a current of the order of 26 A. Voltage of DC link is defined in agreement (1) in 500 V, with V_a=127 V + 5%. The capacitor of DC link is calculated according (5), in 3,6 mF, being I_{neg_pk}= 50 A and ΔV_{DC} = 10 V. Considering a derivative of current as 50 kA/s and a DC voltage in 500 V, is gotten, using (7), a value of 1.9 mH.

VI. SIMULATION RESULTS

Diverse simulations had been carried through to test the control strategy and to verify the static and dynamic conditions of the parameters of the filter. To follow the results of a simulation are presented where some problematic situations are considered that can occur with the electric power grid and its loads, also the presence of distorted voltage for the fifth harmonic in the input. The load is composed for a three-phase rectifier without capacitor, a single-phase rectifier with capacitor in the phase A, and an electrical resistance in phase B, representing an unbalanced situation for phase currents. The switching frequency is 12 kHz, the output inductors are of 2 mH and the DC link voltage is 500 V.

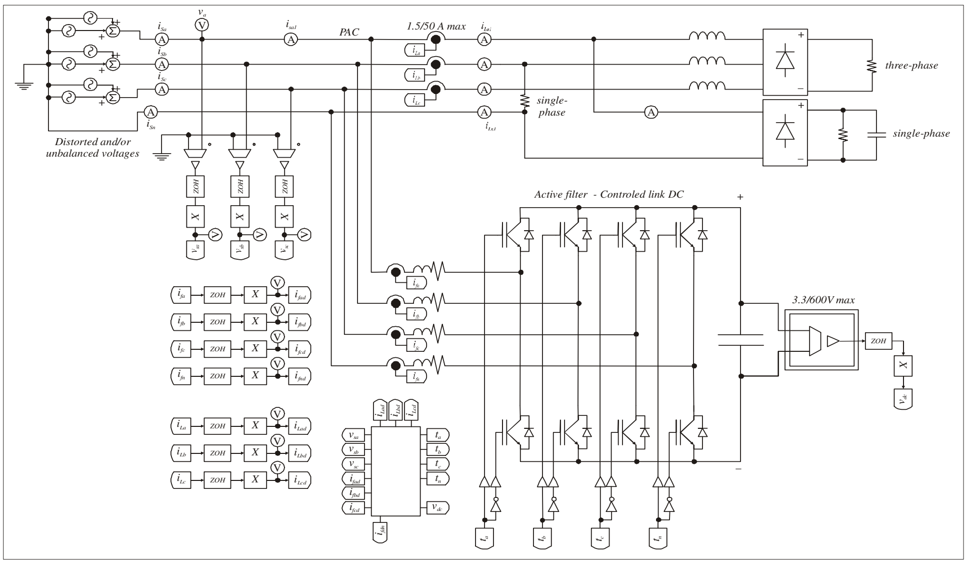

Fig. 6. Simulated circuit showing a set of adverse situations of the load and the power grid.

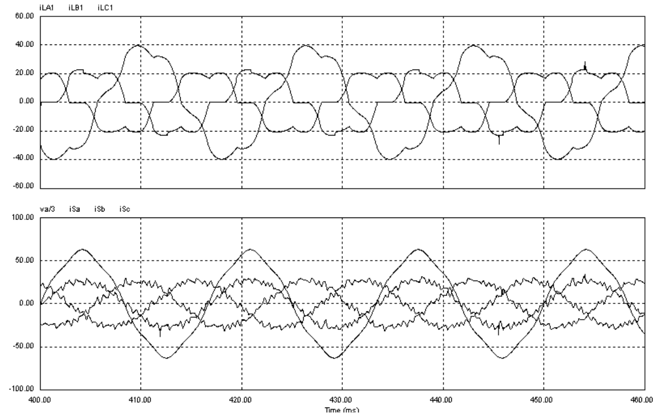

Fig. 7: Loads currents (superior) and source currents with voltage in the phase A (inferior).

It is observed that, although there is an extreme situation that combines harmonic distortion of currents, unbalance and distortion of the input voltage; the output currents are balanced and with reduced harmonic content.

VII. EXPERIMENTAL RESULTS

To follow the results of the operation in laboratory of the active filter for compensation of six loads that compose a sufficiently severe situation of generation of harmonics and unbalanced currents meet. Total load is 11.2 kVA and the diagram of connections is presented in Fig. 8. This loading value got the filter to next to the limits to current protections in the legs of the inverter. The design power of this filter is of 10 kVA.

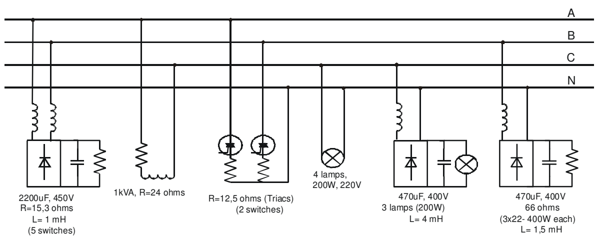

Fig. 8: Loads diagram used for one of the laboratory tests. Nonlinear and unbalanced load – 11.2 kVA.

The measurements had been carried through with a power quality analyzer and an oscilloscope of 4 channels.

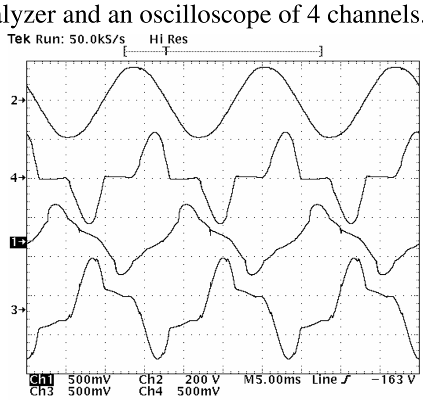

Fig. 9: Voltage in the phase A and load currents in phases A, B, C (10mV/A).

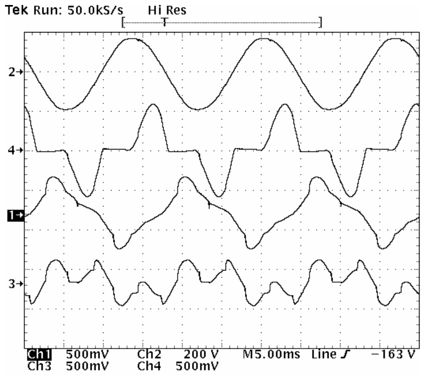

Fig. 10: Voltage in phase A, the load currents in the phases A, B and in neutral current. (10mV/A).

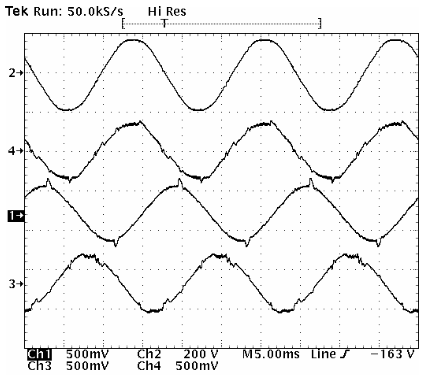

Fig. 11: Voltage in phase A, the load currents in the phases A, B, C. (10mV/A). With the filter in operation.

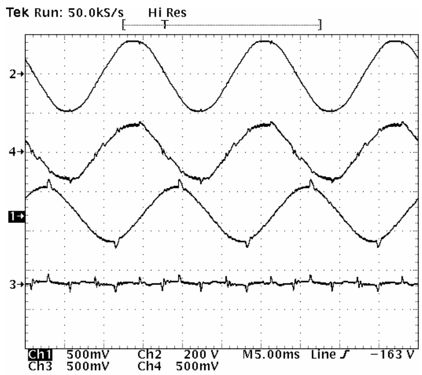

Fig. 12: Voltage in phase A, the source currents in the phases A, B and neutral current. (10mV/A). With the filter in operation.

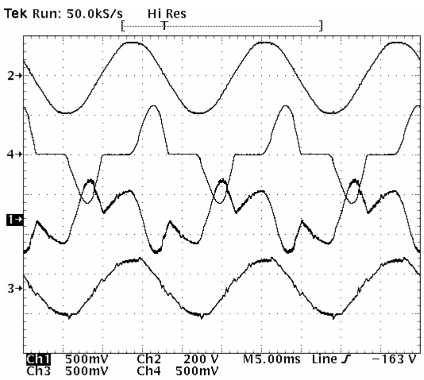

Fig. 13: Voltage, load current, compensation current (filter) and compensated current for source in phase A.

Table 1: Summary of experimental results.

Fases	S (kVA)	FP	Irms (A)	Ipeak (A)	DHT (%)
A – load	3,7	0,59	28,4	55,4	50,1
A – grid	3,0	0,99	23,2	34,6	7,2
B – load	3,1	0,77	24,1	43,3	27,8
B – grid	3,0	0,99	23,5	40,2	7,4
C – load	4,4	0,87	33,8	62,6	38,2
C – grid	3,0	0,99	23,4	35,2	7,8
N – load			16,2	27,4	
N – grid			2,2	7,6	

The Table 1 indicates the apparent power (S), power factor (PF), current (rms), peak current and the current distortion for each one of the conductors of phase and neutral, considering only the load and later the grid (PAC) with the active filter operating. Notice that kVA of the load diminishes in function of the improvement in the power factor (0,99). The current distortion with filter power on, is less than 8%. As much the efficient values, how much the peak are balanced with the compensation. The current of neutral sufficiently is attenuated by the operation of the filter. Notice that the power and consequently, the currents, are distributed between the three phases. Notice that the distortion is considerably reduced, remaining below 15%, even considering distortions up to 76% (Phase A). Errors in the scales of the sensors, as well as low the digital resolution must be considered.

VIII. CONCLUSIONS

This paper presented the design, simulation and practical implementation of a three-phase active filter for compensation of harmonics currents and displacement, with balancing of the current phases.

The built prototype demonstrated very good performance as it could be observed in the experimental results. It must be standed out that the conditions of harmonics generation and unbalancing had been very severe. Even under that conditions the filter minimized the neutral current and reduced the harmonic content to levels that provided the increase of the power factor from 0,50 to 0,99.

An observed important point during the laboratory tests was that the result of the compensation is directly proportional to the operational conditions of the load, as the filter is designed for a defined nominal condition. Thus the study of the load type to be compensated is prerequisite for the correct dimensioning of this filter and its optimization. It is possible to design a filter that covers all the load characteristics, but results will be more expressive if it will be possible to design for a single property load.

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