STABILITY ANALYSIS AND DESIGN OF DISCRETE CURRENT CONTROLLED INVERTERS WITH *LCL*-FILTERS CONNECTED TO THE GRID

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***Abstract*— This paper addresses the design of a robust controller for voltage fed converters connected to the grid through a *LCL*-filter. In this paper the controller design is divided in two steps. The first one is a robust partial state feedback that damps the high frequency modes associated with the *LCL*-filter. The second step deals with the design of an internal model controller to provide reference tracking an rejection of the grid voltage background distortion. Since a state feedback is used, the impact of the sampling approach on the low frequency components is carefully investigated. Finally, experimental results are presented to support the theoretical analysis and to demonstrate the good performance of the proposed robust discrete controller.**

***Keywords*– *LCL* Filter, Grid-Connected Inverters, PWM Converters, Robust State Feedback Sampling Strategies .**

I. INTRODUCTION

With the recent increase of energy demands in many countries around the world, and the concerns with the global warming and greenhouse gases emissions, there is a growing interest on the use of renewable energies sources. Usually, these renewable resources, such as photovoltaic (PV) and wind turbine (WT) systems, have an intermediate voltage DC link from where an inverter is used to exchange power to the grid. For example, in the most modern (WT) systems, an inverter stage is present to avoid the incompatibility of voltage and/or frequency from the generator and the point of commom connection (PCC).

A grid connected inverter need a filter to attenuate the PWM switching harmonics components in the grid-injected currents. In its simplest form this filter is an series inductor. Nevertheless, in high power applications, above several kilowatts, the dynamic performance and cost the filter inductor become unacceptable [1]. As a result, in high power and low switching frequencies converters, the *LCL*-filter become an attractive solution. It is demonstrate in [2] that even with small values of inductance and capacitance, it is still possible obtain satisfactory harmonic attenuation.

The *LCL*-filter has a typical lowpass frequency response, with a resonance peak. Thus, some measure must be taken to avoid oscillations in the resonance frequency. In addition, often, the utilization of wind resources requires that the generation to be located in remote regions, where generally grids with high power transference capacity are not available [3]. Under these conditions, several issues such as limited power transference capability [4], thermal restrictions [5] and instability of the current controller due to uncertainty of the grid impedance at the PCC may became a concern. In the literature, two methods to avoid the *LCL*-filter resonance are generally used: active damping and passive damping. The passive damping consist in a passive device to damp the resonance peak. It may be comprised of a resistor or another passive devices configuration [6]. The main restriction of this method are the additional losses in the passive devices. The active damp consist in a digital compensator in the current control loop [7]. However, active damping generally are designed for a specific grid condition (weak or stiff grid), therefore, when the grid condition change, the zeros and poles of the active damping may turn the system unstable.

This paper derives the design constraints relating the sampling frequency to the *LCL*-filter parameters in order to ensure the controllability of the discrete dynamic equation even with grid impedance variations. Then, a robust partial state feedback is designed to active damp the resonance of the *LCL*-filter. The design of the discrete partial state feedback gains is carried out on the Linear Matrix Inequality (LMI) framework. This ensures robust pole location for a given set of grid impedance. In addition, internal model controllers are used to obtain asymptotic reference tracking and disturbance rejection in order to reduce the impact of grid background voltage distortion. Finally, the main issues related with the sampling of the feedback state variables under the PWM harmonics are discussed. It is shown that a satisfactory steady state performance of the close loop control, depends as well as on an appropriate choice of the sampling strategy.

A numerical example of the robust partial state feedback approach and a resonant controller are present in section II. The overall gains to avoid interaction between the high frequency modes in the resonant controllers modes is numerical developed in Section III. In Section IV the impact of the sampling strategy in the close loop state feedback control is analyse. Finally, experimental results to a DSP controlled grid connected inverter are presented in Section V.

II. SYSTEM DESIGN

The Figure 1 shows the circuit of a three-phase three wire inverter with a output *LCL*-filter connected to the grid. In this paper, the grid impedance will be consider a purely inductive reactance. This is supported by the fact that WT system are

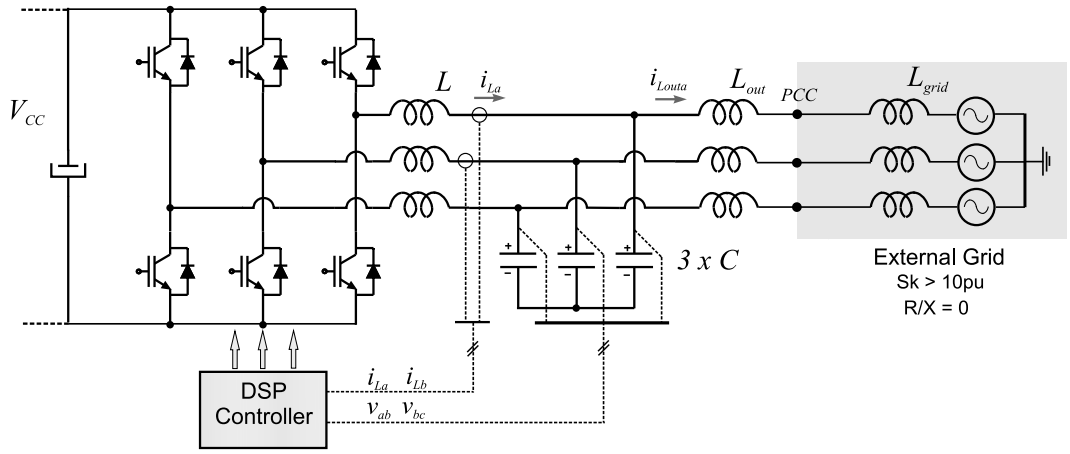

Fig. 1. Three-phase inverter with *LCL*-filter connected to the grid.

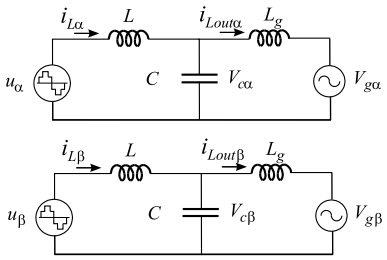

Fig. 2. Equivalent $\alpha\beta$ circuits.

generally connected in distribution grids, hence, the system presents less interaction with residential urban area loads and possibly have no low frequency resonances [7].

To demonstrate the design procedure of the discrete current controller, the control approach developed in [8] will be demonstrate. The three phase circuit is transformed into two single phase decoupled circuits by the well known abc to $\alpha\beta$ transformation. Each of the single phase circuits can be represented by a linear time-invariant dynamic equation given by

$$\begin{aligned} \dot{x}(t) &= Ax(t) + Bu(t) + Fw(t) \\ y(t) &= Cx(t) \end{aligned} \tag{1}$$

where, A= $\begin{bmatrix} 0 & -\frac{1}{L}\frac{V_{base}}{I_{base}} & 0 \\ \frac{1}{C}\frac{I_{base}}{V_{base}} & 0 & -\frac{1}{C}\frac{I_{base}}{V_{base}} \\ 0 & \frac{1}{L_g}\frac{V_{base}}{I_{base}} & 0 \end{bmatrix}$,

$B = \begin{bmatrix} \frac{1}{L}\frac{V_{base}}{I_{base}} \\ 0 \\ 0 \end{bmatrix}$, $C = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}$ and $F = \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_g}\frac{V_{base}}{I_{base}} \end{bmatrix}$

and x is state vector selected as $[i_L/I_{base} \quad v_C/V_{base} \quad i_{Lout}/I_{base}]$, u is the normalized inverter output voltage, w is the normalized grid voltage, y is the normalized boost inductor current. All the states variables in $\alpha\beta$ coordinates are show in Figure 2. Note that the impact of the DC bus voltage on the loop gain can be eliminated by dividing the control action u by the DC voltage.

When considering a implementation in a DSP or microcontroller, it is convenient to analyse the dynamic behaviour of the system in the discrete-time domain. The discrete time system representation with $w(t) = 0$, is given by

$$\begin{aligned} x(k+1) &= Gx(k) + Hu(k) \\ y(k) &= Cx(k) \end{aligned} \tag{2}$$

where

$$G = e^{AT_s} \qquad H = \int_0^{T_s} e^{A(T_s-\tau)}Bd\tau$$

In addition, (2) can be modified to include the delay present in the discrete controller implementation, which results

$$\begin{aligned} \bar{x}(k+1) &= \bar{G}\bar{x}(k) + \bar{H}u(k) \\ y(k) &= \bar{C}\bar{x}(k) \end{aligned} \tag{3}$$

where $\bar{G}$=$\begin{bmatrix} G & H \\ 0 & 0 \end{bmatrix}$, $\bar{H} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix}$, $\bar{C} = \begin{bmatrix} C & 0 \end{bmatrix}$. Note that $\bar{x} = [x \quad u_d]$ is the new state vector and u_d the variable that has been included to represent the time delay of the digital implementation.

Table I shows the filter and setup parameters. The control objective can be state as to design a partial state feedback controller to guarantee high frequency stability in a given range of grid impedances and not interact with the low frequency current controllers.

TABLE I
SETUP PARAMETERS IN ABSOLUTE AND P.U. VALUES

Setup parameters			
LCL-filter	Boost inductance L	1.25mH	26.7%
	Grid side inductance L_{out}	0.500mH	
	Filter capacitor C	70μF	6,4%
	Maximum grid side inductance L_g	0.500mH	S_k=Infinite
	Minimum grid side inductance L_g	0.830mH	S_k= 20
PWM inverter	Sampling frequency	6kHz	
	Switching frequency	6kHz	
	Type of controller	3th, 5th, 7th	
	Type of modulation	Space Vector	
Voltage	Grid voltage	$127V_{rms}$	
	DC inverter voltage	$450V$	
	Rated power	$6.6kW$	
Sensors position	AC voltage sensors	on the capacitors	
	AC current sensors	on the converter side	
Base Values	Voltage Base	$127V_{rms}$	Line
	Current Base	$30A_{rms}$	Values

A. High Frequency Current Controller Design

The first design step is guarantee that the controllability of the dynamic equation is not lost in the discretization. In [8] is demonstrate that the controllability is preserve if

$$f_s > \frac{1}{\pi}\sqrt{\frac{L+L_g}{LL_gC}}. \tag{4}$$

Once this condition is fulfilled, it is possible to active damp the oscillatory modes of the *LCL*-filter with a discrete controller. Observe that the condition (4) is satisfied for the parameters presented in Table I.

The Linear Matrix Inequalities (LMI) theory presented in [9] and applied to grid connected inverters with *LCL*-filters in [8], assures robust pole location for systems with parameter uncertainties.

To apply the LMI theory in the discrete-time equation (3), a model as a function of the uncertain parameter L_g inside a define interval ΔL_g is derived as

$$\bar{x}(k+1) = \bar{G}(\alpha)\bar{x}(k) + \bar{H}u(k) \tag{5}$$

where α represent the number of equally spaced points in ΔL_g.

The desired partial state feedback gain vector K has been selected as:

$$u(k) = K\bar{x}(k)\ ,\ where\ \ K = \begin{bmatrix} k_{11} & k_{12} & 0 & k_{14} \end{bmatrix} \tag{6}$$

Note that $k_{13} = 0$, therefore it is not necessary to measure the grid current for the impementation of the control law. Let

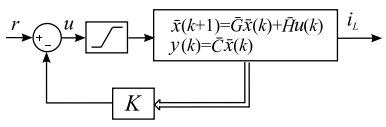

Fig. 3. State-feedback diagram.

a circle $\mathcal{C}$ centered in $d = 0$ with radius $r = 0.95$ inside the unity radius circle, as the desired region to allocate all poles

TABLE II
MATRIXES SET TO COMPUTE THE LMI CONDITION.

α	$\bar{G}(\alpha)$	$\bar{H}$	L_g
1	$\begin{bmatrix} .85 & -.47 & .14 & .54 \\ .46 & .49 & -.46 & .14 \\ .36 & 1.17 & .64 & .07 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}$	$500e-6$
2	$\begin{bmatrix} .85 & -.48 & .15 & .54 \\ .47 & .55 & -.47 & .15 \\ .30 & .98 & .70 & .06 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}$	$582e-6$
3	$\begin{bmatrix} .85 & -.49 & .15 & .54 \\ .48 & .60 & -.47 & .15 \\ .26 & .85 & .70 & .05 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}$	$665e-6$
4	$\begin{bmatrix} .85 & -.49 & .15 & .54 \\ .49 & .63 & -.49 & .15 \\ .22 & .75 & .78 & .04 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}$	$830e-6$

TABLE III
SET $\mathcal{Q}$ OF ALL GAINS THAT SATISFY THE LMI CONDITION.

K	Vector	K	Vector
1	[-1.9 0.8 0 -0.5]	7	[-1.8 0.9 0 -0.6]
2	[-1.9 0.9 0 -0.6]	8	[-1.8 0.9 0 -0.5]
3	[-1.9 0.9 0 -0.5]	9	[-1.8 0.9 0 -0.4]
4	[-1.9 1.0 0 -0.6]	10	[-1.8 1.0 0 -0.6]
5	[-1.8 0.8 0 -0.6]	11	[-1.8 1.0 0 -0.5]
6	[-1.8 0.8 0 -0.5]		

of (3) with the state feedback (6). If there exists a symmetric positive definite matrix $P \in \mathbb{R}^{4\times4}$ such that

$$\begin{bmatrix} rP & (\bar{G}_i + \bar{H}K)'P - dP \\ P(\bar{G}_i + \bar{H}K) - dP & rP \end{bmatrix} > 0, \quad i = 1, \ldots, \alpha \tag{7}$$

then the state feedback with gains K guarantee that all the poles of the dynamic equation (3) are allocated inside the circle $\mathcal{C}$ for any value in ΔL_g.

Table II presents the matrixes $\bar{G}(\alpha)$ for the interval ΔL_g when $\alpha = 4$.

A compact set $\mathcal{S}$ of candidate gains K is defined as

$$\mathcal{S} = \{ \begin{bmatrix} k_{11} & k_{12} & k_{14} \end{bmatrix} \in \mathbb{R}^3 : -1.9 \le k_{11} \le -1.7, \\ 0.8 \le k_{12} \le 1, -0.5 \le k_{14} \le -0.3 \}.$$

The interactive test in the LMI condition can be satisfied for more than one vector gain that belongs to $\mathcal{S}$. By testing the elements of $\mathcal{S}$, with a increment of 0.1 in each entry, k_{11}, k_{12} and k_{14} in each interaction, the possible feedback gains are given in Table III. The positive definite matrixes P have been omitted due the space restriction.

B. Low Frequency current controller design

Since the partial state feedback does not provide good steady-state performance, that is, reference tracking and rejection of the grid voltage background distortion, the use of internal model controller is a good alternative to improve

the quality of the grid currents [10]. The discrete controller structure used to mitigate the background harmonic distortion is given by

$$G_c(z) = \frac{N(z)}{\phi(z)} = \mathcal{Z}\left\{\sum_{i=1}^{N} k_i \frac{s}{s^2 + (i\omega_0)^2}\right\} \qquad (8)$$

where i is the compensated harmonic order.

In the discretization of the controller (8), the zero-pole matched approach is applied for ensure the same frequency response of the discrete controller is similar to the continuous controller counterpart. The overall system control loop, with the internal model controllers and the partial state feedback, is shown in Figure 4.

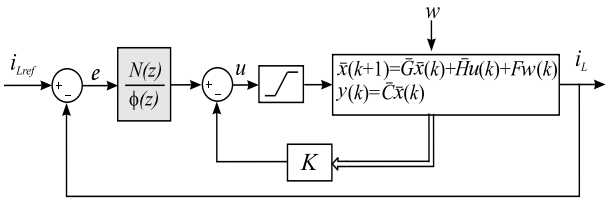

Fig. 4. Proposed closed-loop control for the converter with *LCL*filter connected to the grid.

III. Gains Design

So far, a set of vector gains $\mathcal{Q}$, that provide robust high frequency stability has been found, as well as a resonant controller structure has been selected to provide reference tracking and disturb rejection. The problem now is to select one vector gain belonging to $\mathcal{Q}$ that, even with the inclusion of the internal model controllers, still provides an acceptable behaviour for the overall system.

A procedure to verify the angular contribution of the overall system in each pole of the low frequency controller is described in [8]. By computing the departure angle of the root locus in each resonant pole, for a feedback vector gain K in $\mathcal{Q}$, is possible verifying if all root locus are pointing towards inside the unity radius circle. As a result, by finding a vector gain K that ensures all departure angles of the root locus point toward inside the unit circle in all grid conditions, it is possible to ensure the stability of the closed loop poles associated with the resonant controllers for some gain k_i.

An angle margin can be obtained by the difference of the departure angle of each pole, and the bounds of the unity radius circle at the considered resonant pole. The angle margins for weak and stiff grid conditions with the vector gains given in Table III are showed in Figure 5 for the $7th$ harmonic controller. Note that the weak grid condition is more critical in terms of stability for all values of vector gains of $\mathcal{Q}$.

Figure 6(a) shows the root locus diagram when $K = [-1.8 \quad 0.9 \quad 0 \quad -0.4]$, the ninth vector of $\mathcal{Q}$. By selecting $k_i = 250$, gain margin of 2.55 and 1.54 are obtained for stiff and weak grid respectively. The instability occurs if the gain k_i became greater than $k_i = 635$, note that the angle margin is

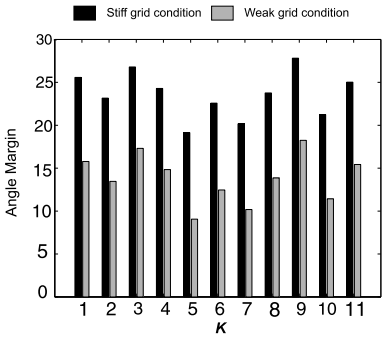

Fig. 5. Angle margin to stiff and weak grid condition of each gain of $\mathcal{Q}$ of the $7th$ resonant controller

27°. Figure 6(b) shows the root locus for weak grid condition and indicate the maximum gain for guarantee the stability. In this case the angle margin decrease to 17°. The limit stability gain is now $k_i = 385$.

Hence, the departure angle analysis define the gains to guarantee the stability in the high and low frequency modes. Note that, in weak grid conditions, the high and low frequency modes may interact with each other. The filter parameters of Table II have been intentionally set high to demonstrate this possible interaction, as well as to show that the proposed control design approach is valid even in this condition.

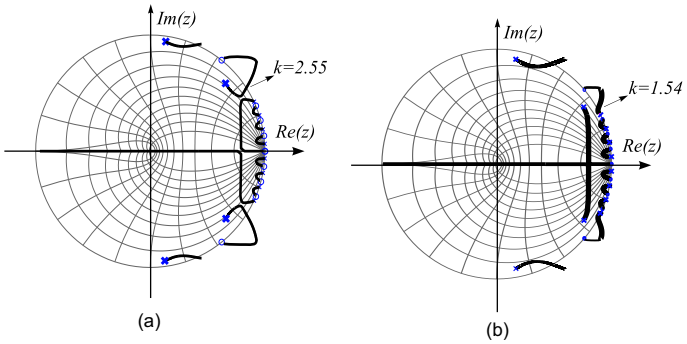

Fig. 6. Root-locus of the designed system, (a) for stiff grid condition and (b) for weak grid condition.

IV. Sampling Strategy Impact

This section address the issues associate with different sampling approaches, since the proposed controller implementation feeds back the sampled state variables which may be corrupted by the PWM harmonics. There always a loss of information produced by sampling. However the extend of this loss depends on the sampling rate as well as in the sampling instants. If the harmonic spectrum of the sampled state has components above a half of the sampling frequency, then the aliasing phenomenon [11], will appear and undesired low frequencies may be introduced in the *LCL*-filter states.

To demonstrate the impact of the sampling strategy on the low frequency harmonics, let us consider the inverter of Figure 1 with the filter parameters of Table IV. These filter

TABLE IV
FILTER PARAMETERS

Parameters	Value
Nominal current	$30A_{RMS}$
Nominal Voltage	$127A_{RMS}$
Capacitance	6.4%
Boost Inductor	20%
$L_{out}min$	7%
$L_{out}max$	15%

parameters are smaller (in pu values) than the consider in Table I, hence, most significant PWM harmonics appear in the *LCL*-filter states and the impact of the sampling strategy is more evident.

Let assume that the *LCL*-filter states are sampled with the strategy described in Figure 7. Note that just one sample and one control law update are present in each carrier period used to generate the PWM.

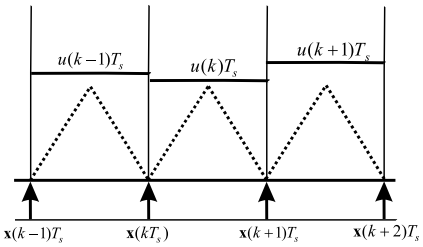

Fig. 7. Sample instant and control law update in function of the virtual carrier.

The capacitors voltage and the output currents are shown in Figure 8. It is also indicated by $*$ the instants when the capacitor voltage is sampled. Since there are harmonics in the sidebands of the switching frequency due to the PWM, and in this case in the sideband of the sampling frequency as well, this harmonics are shifted to the low frequency range in the sampled voltage. In addition, since the capacitor sampled voltage is fed back with the gain k_{12}, this in turn results in undesirable low order harmonics in the inductors currents, as seen in Figure 8

In order to avoid the aliasing in the sampling process, one alternative is increase the sampling frequency. Figure 9 shows a sampling strategy that process two samples and two control law updates in a carrier period. Figure 10 shows the sampling voltage and the resultant output currents. This sampling strategy mitigate the aliasing effect by using a larger sample frequency and sampling the variables in the beginning and middle of the the carrier period. In this case high frequency components around the switching frequency are present in the sampled voltage, and have not been shifted to the low frequency range. As a result, the quality of the grid currents have improved significantly as shown in Figure 10.

V. EXPERIMENTAL RESULTS

The experimental results have been carried out using the setup with the parameters of Table I in a fixed point DSP-controlled based. This results are reported in order to show the

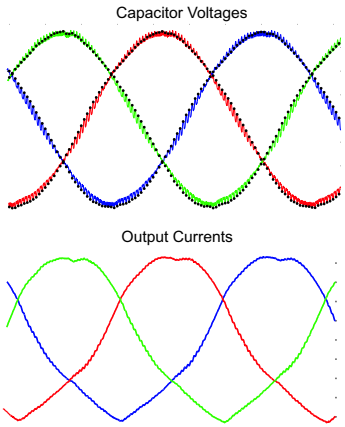

Fig. 8. Capacitor voltage and the instants of sampling and resulting current in L_g.

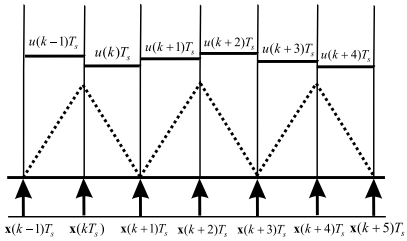

Fig. 9. Two samples and two control actions in each commutation period.

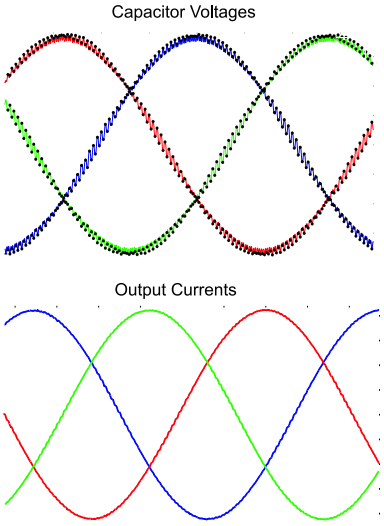

Fig. 10. Capacitor voltage and the instants of sampling and resulting current in L_g.

performance of the robust state feedback control. The design value for the grid side inductance are based in the IEEE 1547 standard, that recommends a minimum short circuit impedance ratio $S_k = 20$ to connect a distributed generation in the grid. The grid impedance are considered $L_g = 0$, $S_k = \infty$ for stiff grid condition, otherwise for weak grid condition $S_k = 20$. The sampling strategy used in this results are the one showing in Figure 7. This system become unstable as predicted analytically when $L_g >$ 925μH. The low bound for

instability is L_g<250μH. The inductance upper bound value to ensure stability, in this case, is defined by the departure angle of the $7th$ harmonic controller. On the other hand, the inductance lower bound value is define by the pole allocation. For the experimental results,the internal model controllers are introduce in the fundamental, third, fifth and seventh harmonics with gains equal to $k_i = 250$.

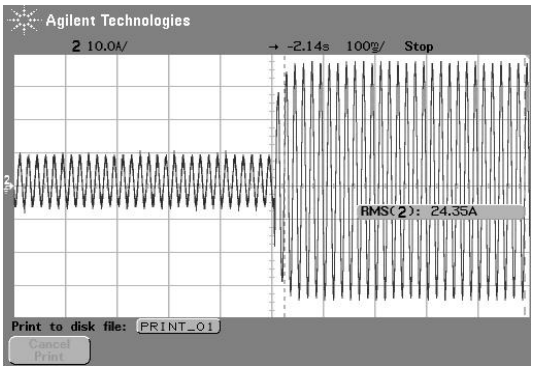

Fig. 11. Boost inductor current transient response to a step change in the reference. Vert:10A/div, horizontal: 100ms/div

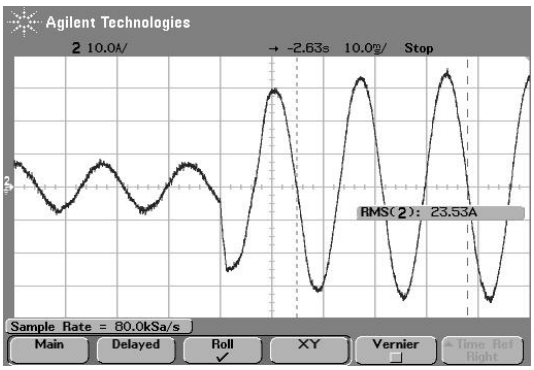

Fig. 12. Boost inductor current wave form and transient response. Vert:10A/div, horizontal: 10ms/div

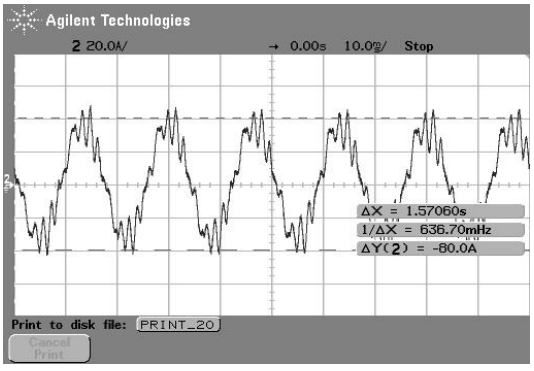

Fig. 13. Boost inductor current in the high inductance limit. Vert:20A/div, horizontal: 10ms/div

Figure 11 shows the transient response due a step applied in the boost inductor current reference from $5A$ to $25A$. In this case when L_g=750μH. Figure 12 shows a zoom in the same current transient. It is possible to see the good quality of the grid current as well as the fast transient response. Figure 13 shows the grid current for L_g= 1000μH, which is a value beyond the defined interval ΔL_g. It is possible to see a low frequency oscillation around the 7^{th} harmonics, which is in agreement with the theoretical analysis..

VI. CONLUSION

This paper demonstrates that by using a discrete current controller designed in the LMI framework, it is possible to provide robust pole allocation using fixed feedback gains for a given interval of grid inductance without requiring the use of self-tunning or adaptive approaches. Moreover, is possible include low frequency controllers and design gains that avoid instability due the interaction of the high and low frequency modes. In closed loop digitally controlled PWM converters, attention should be paid to the sampling strategy. The PWM harmonics can corrupt the sampled variables, introducing unwanted low frequency components by aliasing. This problem growing in importance when the harmonic content of the feedback variables increases, however, if the state variables are sampled at their average values, or the sampling frequency is made at least twice the switching frequency, the aliasing effect is mitigated.

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