# A NOVEL INTERLEAVED BOOST CONVERTER WITH HIGH VOLTAGE GAIN FOR UPS APLICATIONS

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***Abstract* – This work introduces a novel interleaved boost converter whose voltage gain is greater than that of the conventional topology. High efficiency is expected since voltage rating across the semiconductors is reduced. This converter is suitable to applications where large voltage step-up is demanded, such as renewable energy systems based on battery storage and UPS systems.**

***Keywords* – Interleaved converters; high voltage gain.**

## I. INTRODUCTION

The use of batteries and photovoltaic panels as primary source in autonomous electric systems has become more and more common. To transfer the energy from conventional batteries (12 Vdc or 24 Vdc) to typical rms ac voltages (127 $V_{RMS}$ or 220 $V_{RMS}$), it is necessary to step up the battery voltage using a front end dc/dc converter to supply the inverter. The boost converter is strongly suitable for this purpose. However, for appreciable difference between the output voltage and the input voltage, the boost converter must operate with duty cycle (D) greater than 0.95, which is very difficult to obtain due to operational limitations. To obtain the desired voltage, boost converters are connected in cascade, or isolated dc/dc converters with high transformer turns ratio are used instead, even though efficiency is reduced.

To overcome this drawback, solutions using step-up converters capable of operating with high voltage gain ratio were proposed in the literature as in [1]-[3].

In [3] and [4], the use of an interleaved boost converter associated with an isolated transformer was introduced, using the high frequency ac link. Despite of the good performance of such topology, it uses three magnetic cores.

An interleaved boost converter with high static gain employing multiplier capacitors connected in series was proposed in [5]. This converter presents low input current ripple and low voltage stress across the switches. However, high current flows through the series capacitors at high power levels.

In [6]-[8] converters with high static gain based on the boost-flyback topology are introduced. These converters present low voltage stress across the switches, but the input current is pulsed and there is the need of an LC input filter.

The step-up switching-mode converter with high voltage gain using a switched-capacitor circuit was proposed in [9]. This idea is only adequate for the development of low power converters. However high voltage stress across the switches result, and many capacitors are necessary.

From the converter presented in [9], this paper introduces an interleaved boost converter with high output voltage. The proposed converter increases the conventional boost gain about three times using magnetic coupling, as discussed below.

Recently other converters have been proposed. In [10] and [11] the three-state switching cell is shown. In [12] a voltage doubler rectifier is employed as the output stage of an interleaved boost converter with coupled inductors.

## II. PROPOSED CONVERTER

In order to achieve greater output voltage than that of the converter presented in [12], this work proposes the circuit shown in Figure 1. This circuit is magnetically coupled to the conventional interleaved boost converter ($L_1$ with $L_{B1}$, and $L_2$ with $L_{B2}$), as seen in Figure 2.

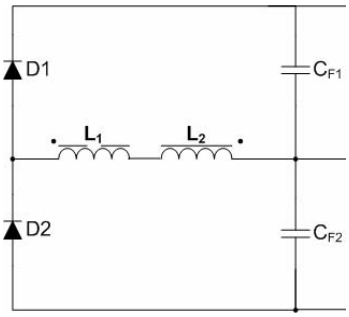


Fig. 1. Magnetically coupled cell.

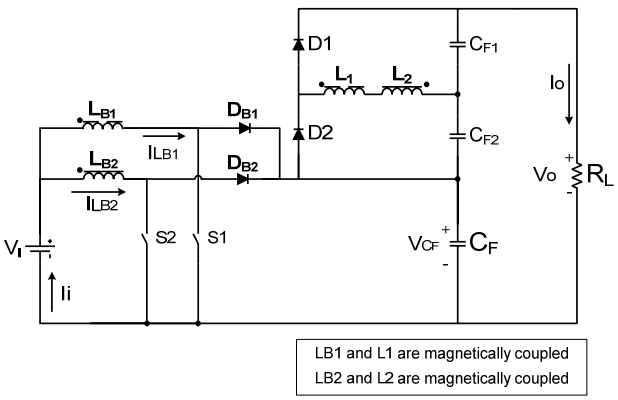


Fig. 2. Proposed high voltage gain converter.

It can be seen in Figure 2 that the number of semiconductor devices is the same as that of the traditional interleaved boost arrangement, although two coupled inductors (L1 and L2), two diodes (D1 and D2), and two capacitors ($C_{F1}$ and $C_{F2}$) are added. As a result, the output voltage is higher.

*A. Operating Principle*

For the theoretical analysis, it will be considered that the input voltage ($V_I$) and output current ($I_O$) are ripple free and all devices are ideal.

A switching cycle of the interleaved boost converter shown in Figure 2 is divided in four stages as shown in Figure 3 to 6. In Figure 7, the main waveforms of the operating stages are presented.

The operating stages or intervals shown in Figures 3 to 6 are described as follows:

**First Stage**: Interval [$t_0$, $t_1$]. This stage begins when switch S1 is turned off, while switch S2 remains turned on. Previously to this stage, both switches are turned on. At instant $t_0$, the capacitor $C_{F2}$ starts charging through the path formed by $D_2$, $L_2$, $L_1$, and $C_{F2}$.

Before switch S1 is turned off, the voltage across switch S1 is equal to the voltage across capacitor $C_F$. Before instant $t_1$, current $i_{LB1}$ reaches zero causing switch S1 to be turned on in ZCS mode.

The first stage finishes when switch S1 is turned on.

The differential equations that describe this stage are:

$$V_{CF} + L_{B1}\frac{di_{LB1}}{dt} - V_i = 0 \quad (1)$$

$$V_{L1} = V_{LB1}\cdot n_1 \cdot k_1 \quad (2)$$

$$L_{B2}\frac{di_{LB2}}{dt} - V_i = 0 \quad (3)$$

$$V_{L2} = V_{LB2}\cdot n_2 \cdot k_2 \quad (4)$$

$$V_{CF2} = V_{L1} + V_{L2} \quad (5)$$

Where:

$V_{CF}$ - voltage across filter capacitor $C_F$;
$L_{B1}$ and $L_{B2}$ - boost inductances;
$iL_{LB1}$ and $i_{LB2}$ - currents through $L_{B1}$ and $L_{B2}$, respectively;
$V_{LB1}$ and $V_{LB2}$ - voltages across $L_{B1}$ and $L_{B2}$, respectively;
$V_{L1}$ and $V_{L2}$ - voltages across $L_1$ and $L_2$, respectively;
$V_i$ - input voltage;
$n_1$ and $n_2$ - transformer turns ratios;
$k_1$ and $k_2$ - magnetic coupling coefficients.

**Second Stage**: Interval [$t_1$, $t_2$]. At instant $t_1$ switch S1 is turned on in ZCS mode and switch S2 remains turned on. The energy is stored only in inductors $L_{b1}$ and $L_{B2}$ and is not transferred to the load. This stage, represented in Figure 4, finishes when switch S2 is turned off. The equations that represent this stage are:

$$L_{B1}\frac{di_{LB1}}{dt} - V_i = 0 \quad (6)$$

$$L_{B2}\frac{di_{LB2}}{dt} - V_i = 0 \quad (7)$$

**Third Stage**: Interval [$t_2$, $t_3$]. The stage begins when switch S2 is turned off. The voltage across switch S2 before this transition is equal to the filter capacitor voltage. Energy transfer from inductor $L_{B2}$ to capacitor $C_F$ occurs through the loop formed by $L_{B2}$, $D_{B2}$, $C_F$, and Vi. After the inductor discharge current $i_L$ becomes null, allowing the turning on of switch S2 in ZCS mode. The relevant differential equations are:

$$V_{CF} + L_{B2}\frac{di_{LB2}}{dt} - V_i = 0 \quad (8)$$

$$V_{L2} = V_{LB2}\cdot n_2 \cdot k_2 \quad (9)$$

**Fourth Stage**: Interval [$t_3$, $t_4$]. It begins when switch S2 is turned on in ZCS mode. Both switches are turned on, and differential equations are the same as those of the second stage. This stage finishes when switch S1 is turned off.

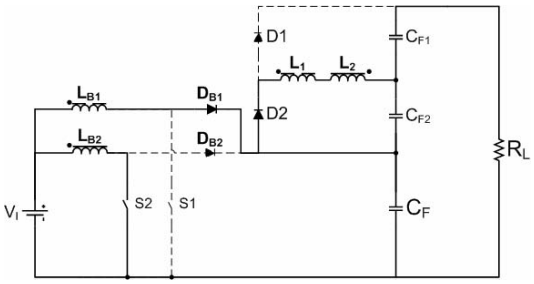

Fig. 3. First stage.

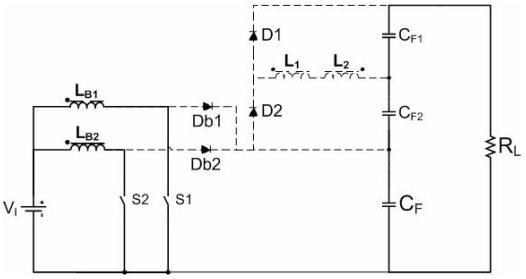

Fig. 4. Second stage.

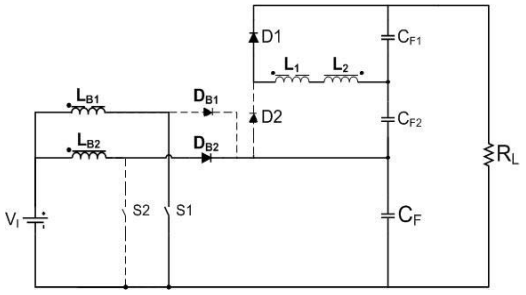

Fig. 5. Third stage

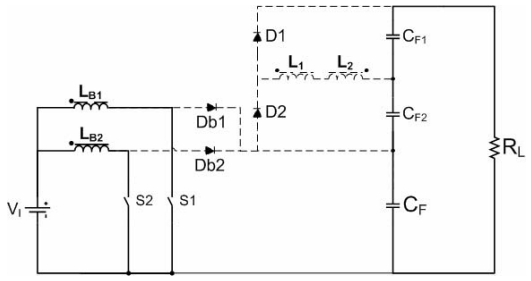


Fig. 6. Fourth stage

In Figure 7, the main waveforms representing the operating stages are presented.

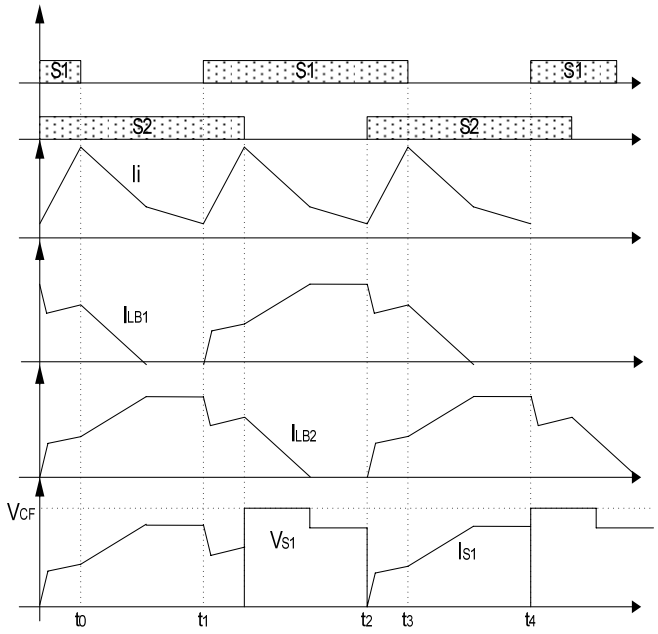


Fig. 7. Main theoretical waveforms.

As in Figure 7, the maximum voltage across the switches is Vcf. Thus, for unity turns ratio of each coupled inductor, the voltage across the switch is lower than half the output voltage. In the same figure it can be noticed that this converter operates softly with ZCS turning on.

From the equations developed in this section and the analysis of Figures 3 to 7, the expression representing the static gain *G* can be obtained as (9)

$$\frac{V_O}{V_I} = \frac{(2 \cdot n \cdot k + 1)}{(1 - D)} \tag{10}$$

Where:

k - magnetic coupling coefficient;

*n* - transformer turns ratio.

$$n = \sqrt{\frac{L_{Bx}}{L_X}} \tag{11}$$

## III. SIMULATION AND EXPERIMENTAL RESULTS

Figures 8 and 9 show some simulation results. It can be seen that the input current of the converter is in continuous current mode. Switches S1 and S2 can operate in ZCS mode due to the leakage inductance and the discontinuous current mode (DCM) during the first and third stages. Although the inductors operate in DCM, the input current remains in continuous mode, as seen in Figure 8. The table I shows the simulations parameter set.

TABLE I
SIMULATION PARAMETERS AND SPECIFICATIONS

| $V_i$ | $V_0$ | $f_s$ | $L_{B1}$ , $L_{B2}$ | $L_1$ , $L_2$ |
|---|---|---|---|---|
| 24V | 200V | 25kHz | 30µH | 30µH |

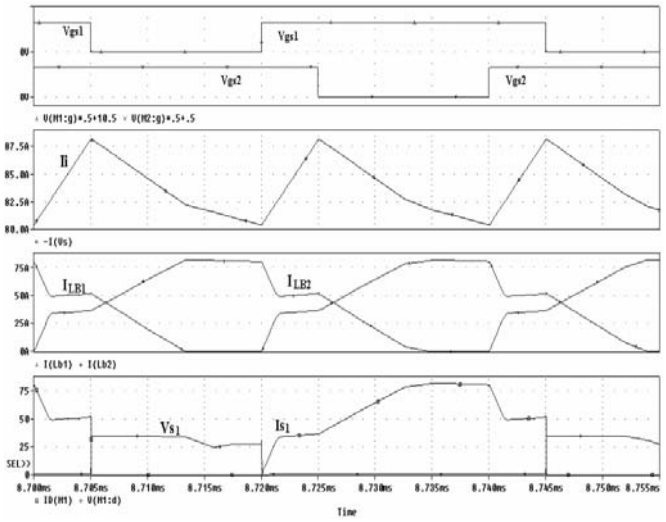


Fig. 8. Main waveforms.

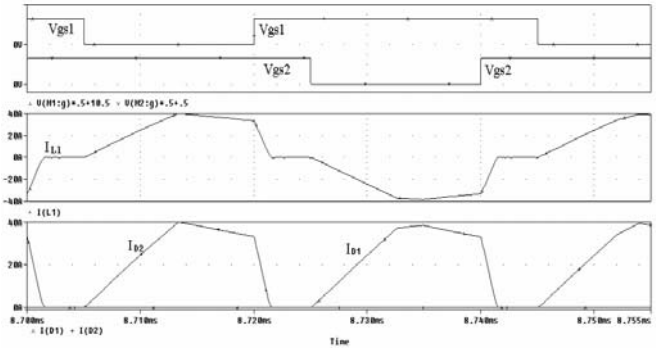


Fig. 9. Main waveforms.

In order to evaluate the performance of the simulated converter, a prototype with the same specifications and parameters given in Table I was implemented. Ultrafast diodes MUR460, switches MOSFET's IRFP4710 and three capacitors rated at 470µF/250V are employed.

Figure 10 shows the measured drain-to-source voltage across switch S1 in the channel 1, L1 and L2 inductors voltage in the channel 3 and the currents through the primary side of the coupled boost inductor Lb1 in the channel 2.

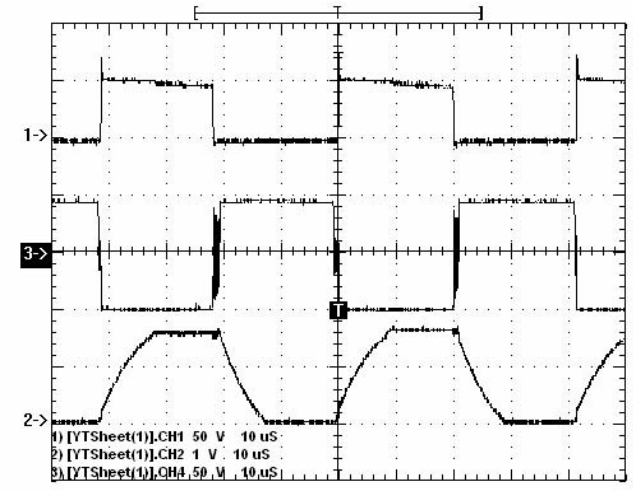


Fig. 10. Waveform Experimental Results.
Ch 1 - Drain-to-source voltage across switch S1(50V/div);
Ch 3 - L1 and L2 inductors voltage (50V/div);
Cha 2 - Currents through of the boost inductor Lb1 (50A/div);

Figure 11 shows the Lb1 inductor current (channel 1) and L1 inductor current (channel 2) in the oscilloscope.

Figures 12 and 13 show the current waveforms of the inductor Lb1, L1 e L2.

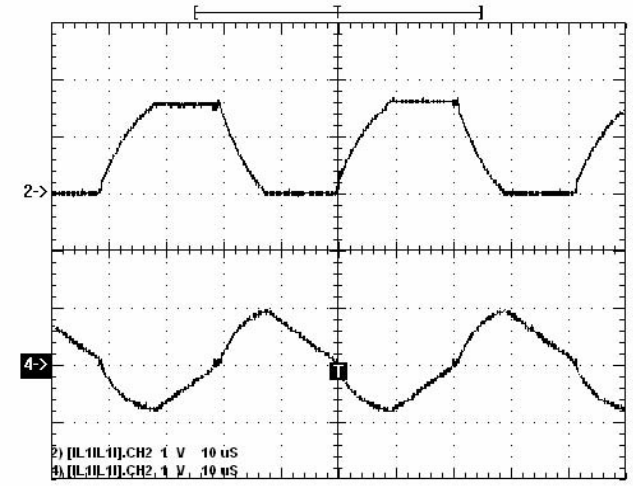


Fig. 11. Lb1 inductor Currents (50A/div) in the Channel 1 and L1 inductor Currents (50A/div) in the Channel 2.

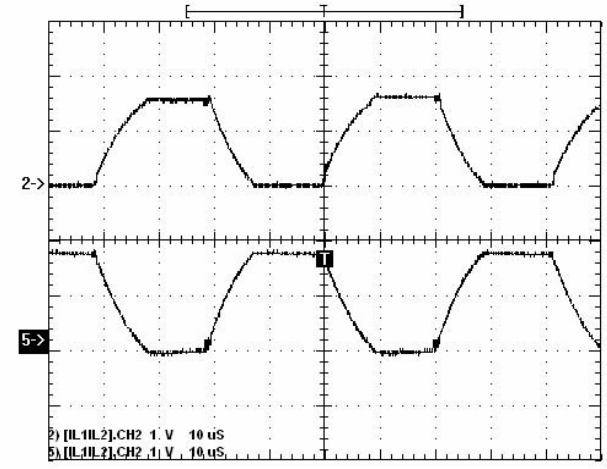


Fig. 12. Lb1 and Lb2 inductor currents, respectively. (50A/div).

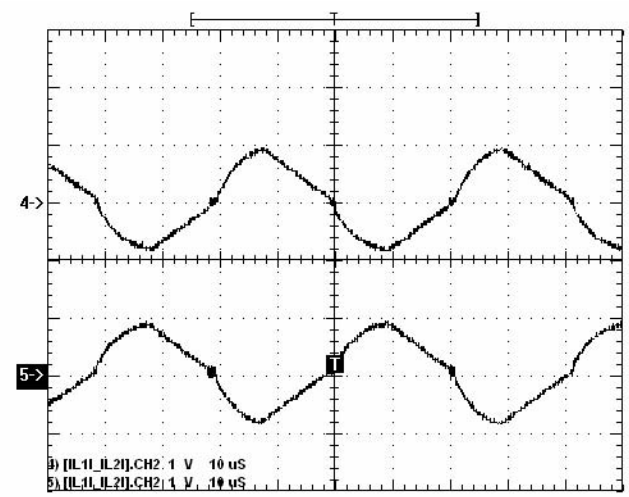


Fig. 13. Currents through inductors L1 (upper) and L2(lower).
Cha 2 - Currents through of the boost inductor Lb1 (50A/div);

Figure 14 shows the experimental waveforms on the switch correspondent to those from Figure 8. One can see the experimental results are closed to the simulation ones.

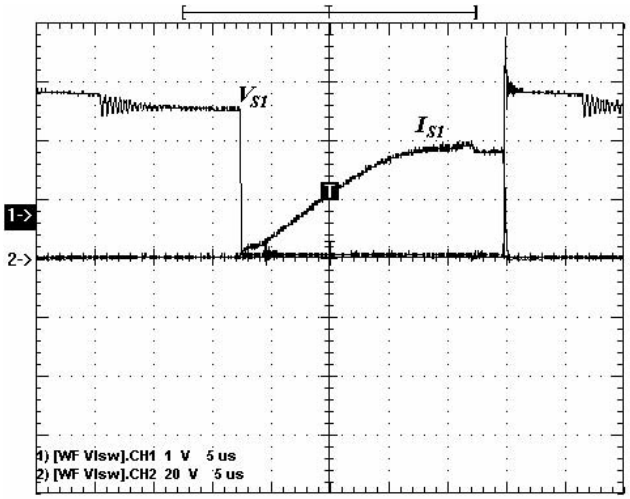


Fig. 14. Voltage (20V/div) and Current (50 A/div) on the switch S1.

Figure 15 presents the efficiency of the converter as a function of the output power, which is above 90% along the power range. The proposed converter using MOSFET's with reduced on-resistance is supposed to present greater efficiency, since conductions losses would be minimized.

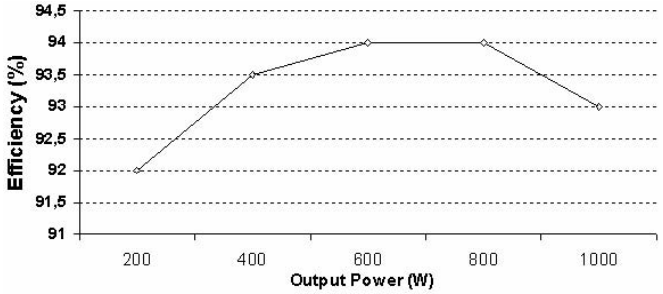


Fig. 15. Efficiency curve of proposed converter.

## IV. CONCLUSION

An interleaved boost converter with high voltage gain for UPS applications has been presented in this paper.

Although this converter has additional passive components, such as two extra diodes, two extra inductors, and two extra capacitors if compared to conventional interleaved boost topology, it operates with reduced voltage across the switches and voltage gain three times greater than that of the traditional arrangement.

The output voltage was limited in 150 V due to the switches used in the prototype. The drain-to-source breakdown voltage of the IRFP4710 device is 100 V.

The high voltage gain of this topology allows it to supply a VSI converter with high efficiency, for instance.

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