A THREE PHASE ZVS ACTIVE-CLAMPING VOLTAGE SOURCE INVERTER

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***Abstract* – This work presents a three phase zero voltage soft-switching active-clamping voltage source inverter. From half load to rated load, commutation under ZVS condition is satisfied, and a quasi ZVS commutation is guaranteed under all other load current. The topology has the feature of being modulated by any conventional pulse-width-modulation strategy employed in the hard-switching inverters. The maximum voltage applied in all switches is clamped and limited in a reduced value and it does not produce excessive current stress. Operation description and theoretical analysis are presented as well as simulation and experimental results taken from a 7.5kVA laboratory prototype.**

***Keywords* - Active voltage clamping, low current and voltage stress, three phase inverter, zero voltage switching.**

I. INTRODUCTION

In the output of a voltage source inverter, excellent voltage and current waveforms are expected, and a minimal harmonic content is considered.

To achieve a minimal harmonic content and to reduce the audible noise in voltage source inverters it is desirable operate at high switching frequencies.

However, when the switching frequency increases, the efficiency and reliability of the PWM converter deteriorate significantly. Some efforts have been made to reach this aim and various topologies were proposed to achieve soft switching in voltage source inverters [1-9].

A great contribution to this area is the Undeland Snubber [1]. It is a passive topology and it is not able to regenerate the commutation energy directly.

The resonant pole inverter (RPI) [2] provides zero voltage switching (ZVS) in all switches, but it has an excessive resonant current that also circulate in the load.

The rugged inverter (ARDPI) [3] combine the advantages of PWM strategy and soft switching techniques, but needs excessive resonant current to get soft commutation. The resonant current required must be at least twice the load current value.

The auxiliary resonant pole inverter topology (ARPI) [4] gives a good improvement regarding to this problem (theoretically). However it requires modification in the PWM strategy. In practice this topology needs a resonant current about twice the load current value.

Another philosophy was proposed in the auxiliary resonant commutated pole inverter (ARCPI) [5, 6, 7]. In this topology the resonant pole is connected in parallel with the load. This type of circuit has a complex control strategy and the resonant current assumes large values that are reflected to the main switches increasing their current stress.

In this work a three phase topology of a pulse-width-modulation zero-voltage-switching active-voltage-clamping voltage source inverter is proposed. The proposed inverter combines the goals of soft switching commutation in all active switches, high frequency capability, conventional PWM strategy and no excessive additional voltage or current stress. A digital circuitry is being developed to drive the switches and improving the performance of the system. It is possible to implement scalar or vector control.

In the main switches, ZVS commutation is achieved from half load to rated load, and a quasi ZVS commutation is guaranteed under all other load current conditions. This characteristic allows the converter operating with a high efficiency in a wide range load and it prevents the converter operating with excessive circulating energy.

The commutation of the auxiliary switches is ZVS under all load condition. The auxiliary switches are designed to conduct only 10% of the rated main switches current. It prevents the converter operating without excessive voltage or current stresses.

Experimental results prove that the design methodology is effective, and the soft-switching circuit is well suited for voltage source inverter applications.

II. CIRCUIT DESCRIPTION AND OPERATION

In Fig. 1 is shown the proposed Zero-Voltage-Switching Pulse-Width Modulation Active-Voltage-Clamping Voltage-Source Inverter (ZVS-PWM-AVC-VSI). This topology is the three phase version of the ZVS-PWM-AVC Voltage Source Inverter, shown in Fig. 2a [8]. In the Fig. 2b is shown the switch model used in the proposed inverter. In reality the adequate switch to use is dependent on the application. For motor adjustable speed drives it is recommended the use of IGBT and for uninterruptible power supply the use of MOSFET.

Each the phase leg of the inverter consists of two main switches, two auxiliary switches, two diodes, two resonant capacitors, two resonant inductors and two clamping capacitors. All the body diodes and parasitic capacitors of the semiconductors are incorporated in the circuit operation.

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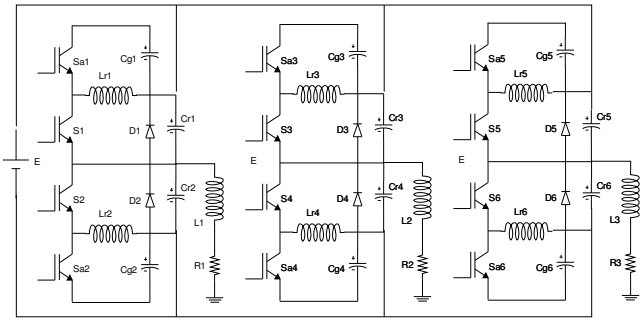
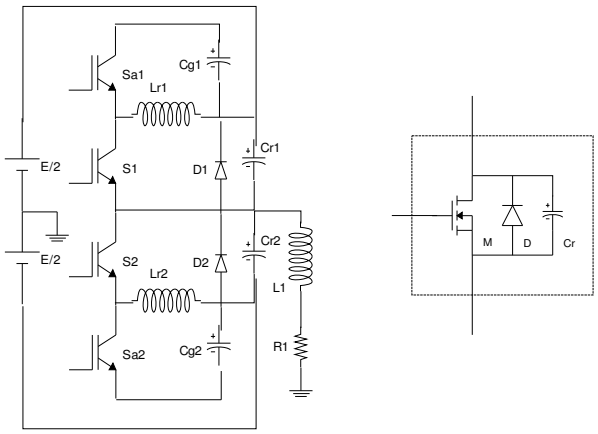


Fig. 1. The proposed Three Phase ZVS-PWM-AVC-VSI.



a) topology b) switch model

Fig. 2. Mono phase version of the ZVS-PWM-AVC Voltage Source Inverter and switch model.

The topological stages for one equivalent inverter leg in one period of commutation are shown in Fig. 3, and the main theoretical waveforms are shown in Fig. 4.

Each phase leg of the proposed inverter presents nine stages of operation in one period of commutation, explained as follows.

First Stage (t_0, t_1): in this stage the main switch *S2* is conducting. The current through *Lr1* is equal to the load current and the current through *Lr2* is equal to zero. During this stage energy is transferred to the load.

Second Stage (t1, t2): at the instant t1, switch S2 is turned-off and the resonant capacitors Cr2 and Cr5 are linearly charged. The voltage across Cr1 varies from zero to E+vg1 and the voltage across Cr5 varies from zero to E. The resonant capacitors Cr1 and Cr6 are discharged and the voltages across their terminals vary from E+vg1 and E to zero, respectively. The current iLr1 remains constant and equal to the load current.

Third Stage (t2, t3): when the voltage across Cr2 equals E+vg1 the voltage across Cr1 becomes null, and diode D1 starts to conduct. Simultaneously the voltage across Cr5 becomes equal to E, the voltage across Cr6 becomes null, and diode D6 starts to conduct the load current. The inductor Lr1 demagnetizes through the clamping capacitor Cg1 via D1. During this stage switch S1 must be gated on, so that in the next stage soft commutation is achieved.

Fourth Stage (t3, t4): when iLr1 becomes zero, diode D1 is blocked and switch S1 starts to conduct without commutation losses. Current iLr1 changes its direction and increases linearly in a negative sense.

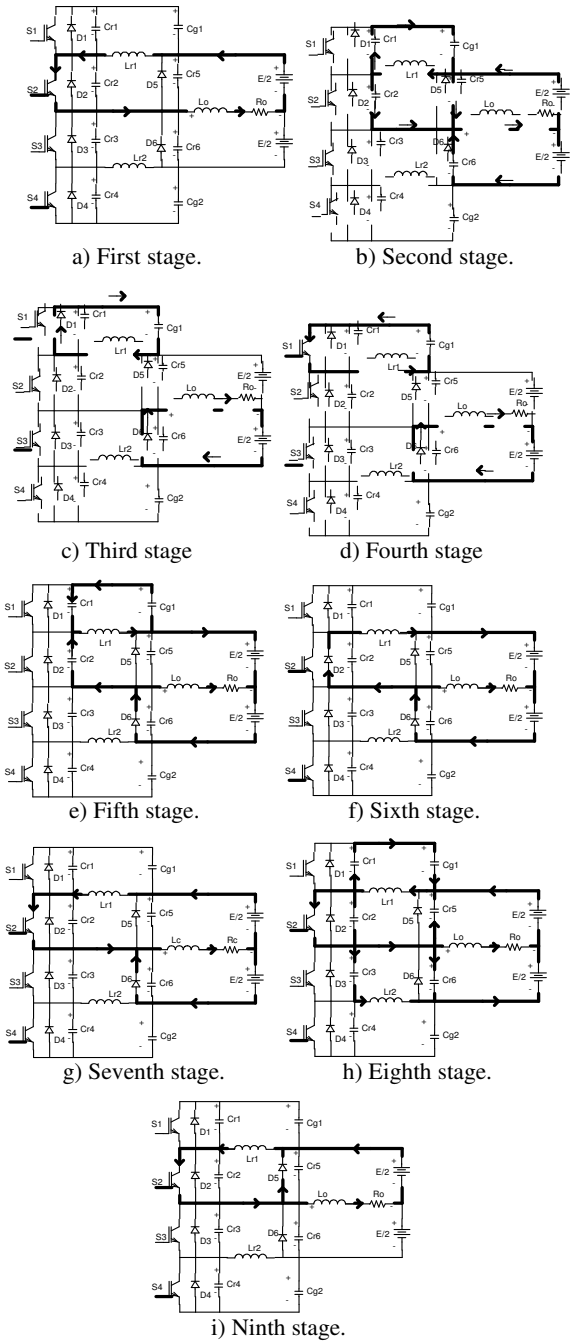


Fig. 3. Topological stages for one switching period.

Fifth Stage (t4, t5): at the instant t4, the switch S1 is blocked. Capacitor Cr1 is charged and capacitor Cr2 is discharged linearly, while the current through Lr1 remains constant and equal to the load current. The voltage across Cr1 increases from zero to E+vg1, while the voltage across Cr2 decreases from E+vg1 to zero.

Sixth Stage (t5, t6): when vCr2 becomes equal to zero, diode D2 starts to conduct the current iLr1. In this stage Lr1 is demagnetized through E and its energy is recovered.

Seventh Stage (t6, t7): at the instant t6 the current through Lr1 becomes null and diode D2 is blocked. Switch S2 starts to conduct without commutation losses. The current through Lr1 increases sharply, fed by E via S2 and D6.

Eighth Stage (t7, t8): when iLr1 becomes equal to the load current, the current in diode D6 becomes null, blocking

it. A resonance involving Lr1, Cr1, Cr3, Cr5 and Cr6 begins. The current through Lr1 increases in a sinusoidal fashion as shown in (1). The voltages across Cr1 and Cr5 decrease from E+vg1 to vg1 and from E to zero, respectively. The voltages across Cr3 and Cr6 increase from zero to E.

$$i_{Lr1}(t) = i_{Lr1}(t7) + \frac{E}{Zn}\sin(w_o t) \quad (1)$$

Where:

$$Zn = \sqrt{\frac{Lr}{4Cr}}$$

$$w_o = \frac{1}{\sqrt{4LrCr}}$$

$$Lr = Lr1 = Lr2$$

$$Cr = Cr1 = Cr2 = ... = Cr6$$

Ninth Stage (t8, t9): when the voltage across Cr6 equals E, the voltage across Cr5 becomes null and diode D5 starts to conduct. The current through Lr1 decreases as a consequence of the resistive elements present in the loop formed by S2, Lr1 and D5. When the current through Lr1 becomes equal to the load current, the first stage of operation restarts and one switching period is completed.

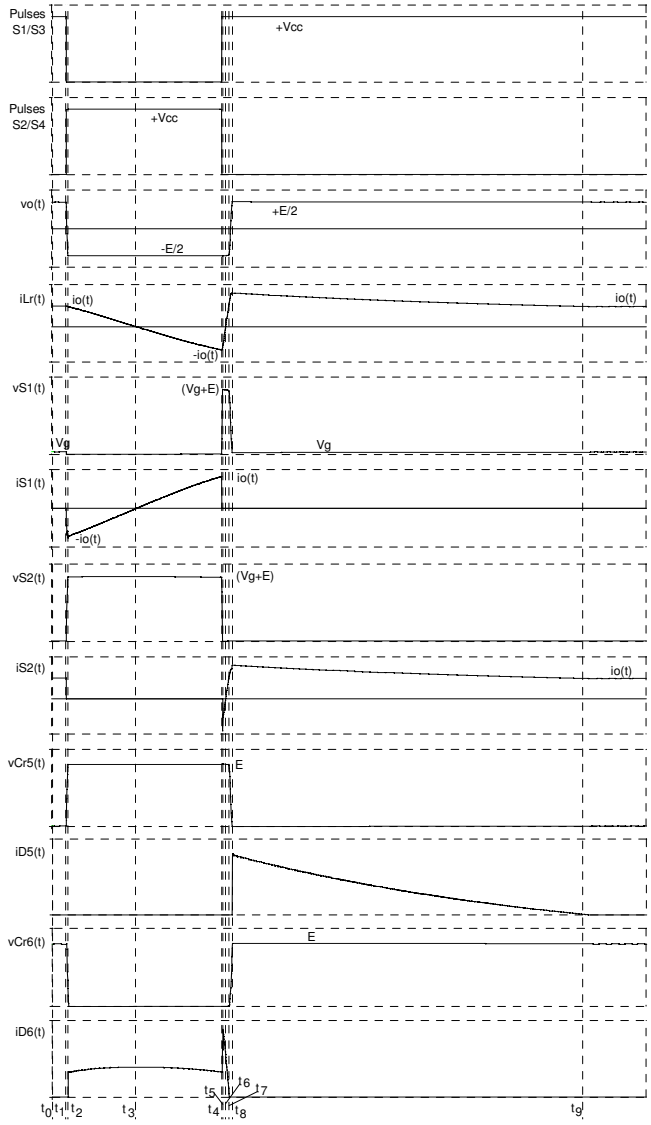


Fig. 4. The main theoretical waveforms in one switching period.

III. THE CLAMPING ACTION

The maximum active switches voltage is the sum of the DC bus voltage (E) and the maximum clamped voltage. The clamped voltage can be easily controlled by an appropriate combination of resonant parameters (Cr and Lr). The resonant parameters also control the soft commutation range.

The normalized clamped voltage $\overline{v_{g1}(t)}$ is expressed by (2). The normalized maximum clamped voltage is given by (3) and it is graphically represented by Fig. 5.

$$\overline{v_{g1}(t)} = \frac{v_{g1}(t)}{E} = \frac{ma\ sin(w\,t)}{\gamma\,\pi\,fn\,[1 - ma\ sin(w\,t)]} \quad (1)$$

$$\overline{v_{g1_{max}}} = \frac{v_{g1_{max}}}{E} = \frac{ma}{\gamma\,\pi\,fn\,(1-ma)} \quad (2)$$

Where: ma is the amplitude modulation ratio

$$\gamma = \frac{Zo}{Zn}$$

$$fn = \frac{fr}{fs}$$

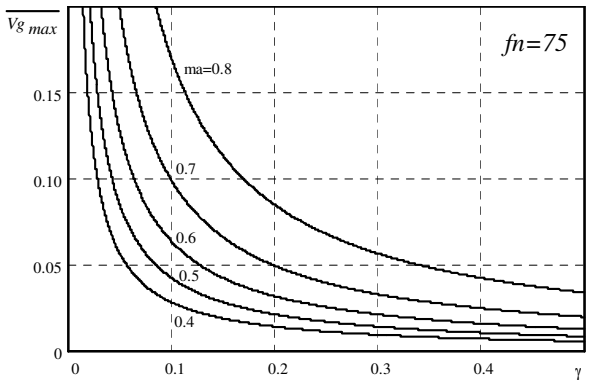


Fig. 5. Normalized maximum clamping voltage.

IV. COMMUTATION ANALYSIS

Soft commutation is achieved when the following expression is satisfied (3). The range for main switches soft commutation is graphically represented by Fig. 6. Auxiliary switches commutations are ZVS under all load condition.

$$w\,t \geq a\,sin\left(\frac{2\,\gamma}{ma} + \frac{2}{\pi\ fn\,(1-ma)}\right) \quad (3)$$

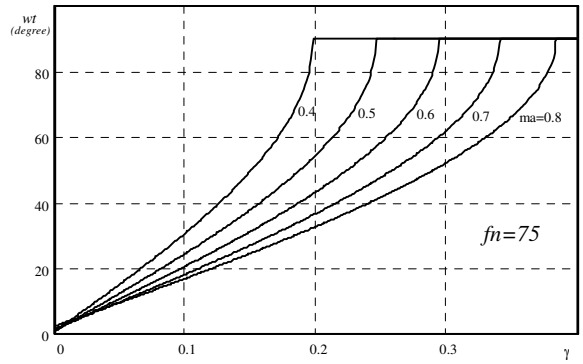


Fig. 6. Main switches soft commutation range.

V. OBTAINED RESULTS

A laboratory prototype of a 7.5kVA zero-voltage-switching pulse-width-modulated three phase voltage-source inverter with active voltage clamping (ZVS-PWM-VSI-AVC) has been built. The previous results were obtained with the inverter operating under conventional sinusoidal pulse-width modulation and using IGBT like main and auxiliary switches. The design characteristics per phase are given as follows and represented by the equivalent circuit shown in Fig. 7.

$Vo_{rms} = 120V$ (output rms voltage)

$Io_{rms} = 21A$ (output rms current)

$fo = 60Hz$ (output frequency)

$fs = 20\ kHz$ (switching frequency)

$ma = 0.8$ (amplitude modulation ratio)

$Lo = 4.8mH$ (load inductance)

$Ro = 5.4\Omega$ (load resistance)

The equivalent DC bus has a medium point and its total voltage is equal to $E = 440V$. Choosing $fn = 75$ and the soft commutation range between 20^o and 160^o and with the aid of Fig. 6, $\gamma = 0.12$ is obtained. Hence:

$$Zn = \sqrt{\frac{Lr}{4\,Cr}} = \frac{Zo}{\gamma} = 49.02\Omega$$

$fr = fs\ fn = 1.50\ MHz$ (resonant frequency)

$$Lr = \frac{Zn}{2\,\pi\,fr} = 5.2\mu H$$

$$Cr = \frac{Lr}{2\,Zn^2} = 0.5\ nF$$

$$Cg = \frac{1}{4\,\pi^2\,Lr\,fs^2} = 12\ \mu F \text{ (clamping capacitance)}$$

$$v_{g_{max}} = \frac{1}{\pi\,\gamma\,fn\,(1-ma)}\frac{ma}{} = 54V$$

$$i_{Lr_{max}} = \frac{ma\,E}{2\,Zo} = 39\ A$$

With the calculation made above the relevant devices specifications could be made and are given below.

S1 and S4 – STGP7NB60H – ST Microelectronics
S2 and S3 – IRG4PC50U – International Rectifier
D1–D4 – MUR460 – Motorola
D5 and D6 – HFA15TB60 – International Rectifier
Lf – 633 µH (output inductance filter)
Cf – 22 µF (output capacitance filter).

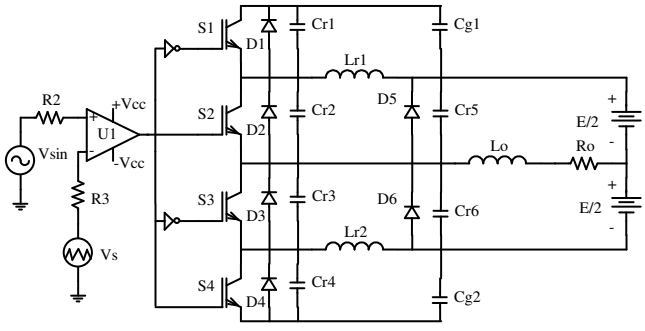


Fig. 7. The experimented inverter.

The following figures show the main obtained results. Fig. 8 shows the filtering voltage across and current through the load in one phase of the inverter output. The inductive load nature causes the phase shift between the both curves.

The clamping voltages across Cg1 and Cg2 are shown in Fig. 9. It could be seen that the voltage is clamped in 48V.

The resonant current through Lr1 is shown in Fig. 10 for one load period and in Fig. 11 for one switching period. The maximum value of the resonant current is limited to 39A.

Fig. 12 shows the voltage across and the current through the auxiliary switch S1. It can be seen that despite of the IGBT tail current, the commutations are lossless.

In Fig. 13 it is shown the voltage across and the current through the main switch S2. A detail of the turn-on process in the main switch is shown in Fig. 14. This figure proves that the turn-on process of the main switch S2 is entirely lossless at rated load.

Fig. 15 shows the three line currents in the three phase load and Fig. 16 shows the three line voltages without any filtering.

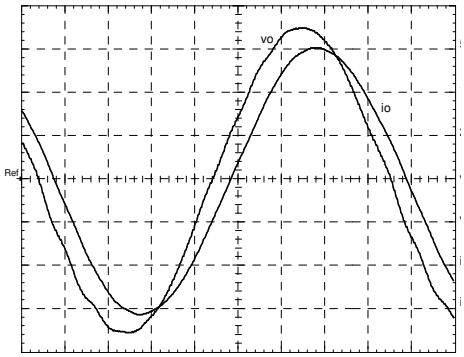


Fig. 8. Voltage across and current through the load (50V/div; 5A/div; 2ms/div).

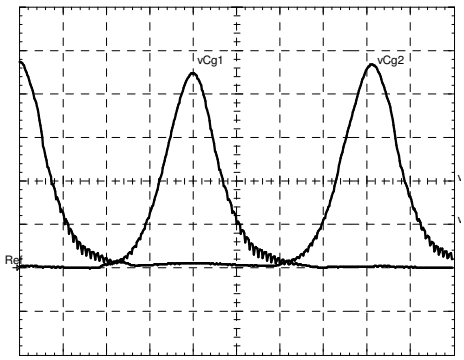


Fig. 9. Clamped voltages in Cg1 and Cg2 (10V/div; 2ms/div).

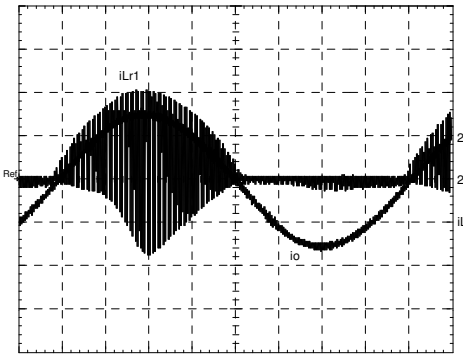


Fig. 10. Current through Lr1 superposed with the load current (10A/div; 2ms/div).

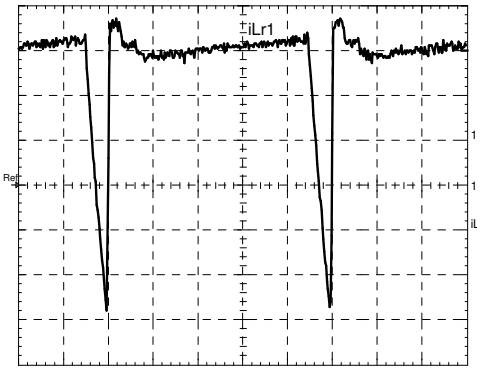


Fig. 11. Detail of Lr1 current during one switching period (10A/div; 10µs/div).

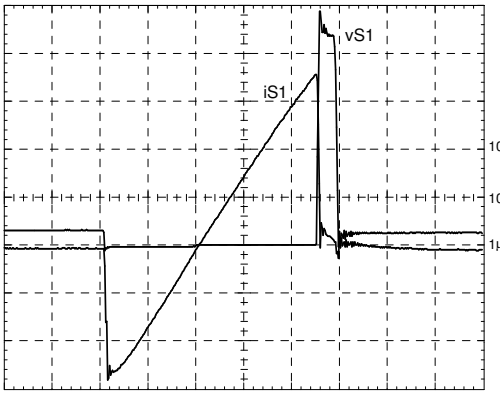


Fig. 12. Voltage across and current through the auxiliary switch S1 (100V/div; 10A/div; 1µs/div).

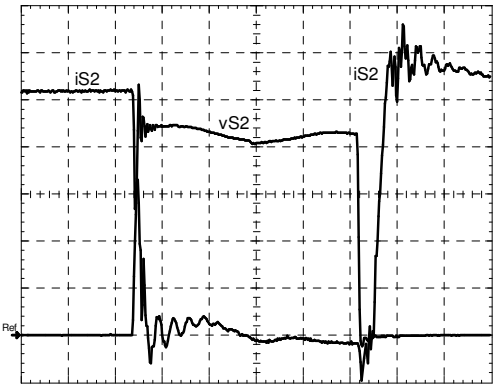


Fig. 13. Voltage across and current through the main switch S2 (100V/div; 5A/div; 1µs/div).

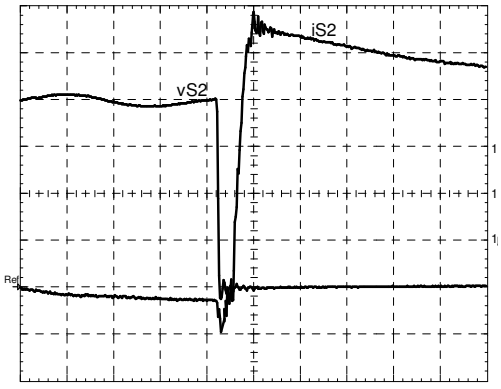


Fig. 14. Detail of the main switch S2 turn-on process (100V/div; 10A/div; 1µs/div).

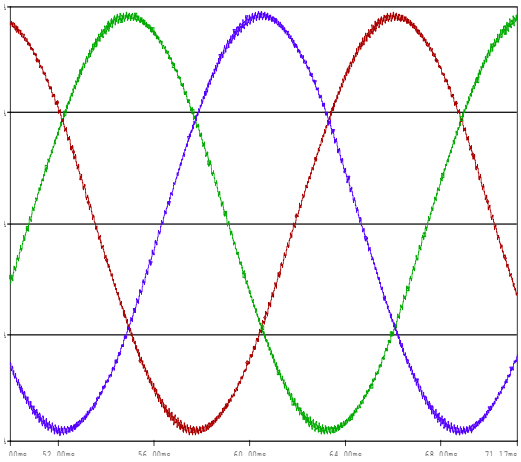


Fig. 15. The three line currents applied to the load.

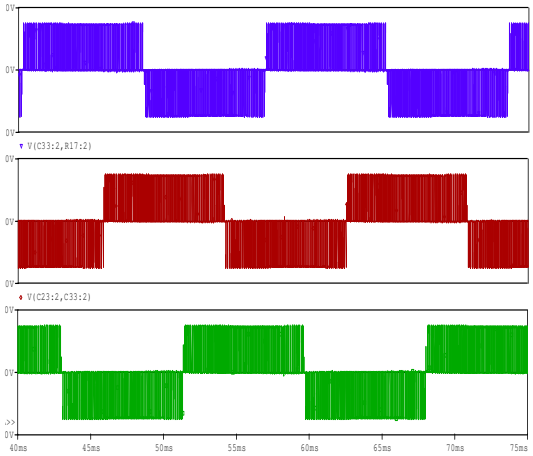


Fig. 16. The three line voltages applied to the load with any filtering.

VI. CONCLUSION

In this paper a three phase zero-voltage-switching pulse-width modulation voltage-source inverter with active-voltage clamping (3Φ ZVS-PWM-VSI-AVC) was presented and analyzed. Experimental results obtained from a laboratory prototype indicate that it is suitable for voltage source inverter applications. Some characteristics of this inverter are better than the characteristics of other topologies applied to obtain inverter soft switching. The new inverter topology combines the advantages of a soft-commutated converter using the zero-voltage-switching technique in a wide range of load current and those of a conventional pulse-width modulation. The current and voltage stress was limited to 30% of the load current and 11% of the DC bus, respectively. The authors are implementing a digital drive to substitute the analogical one.

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