THREE LEVEL FORWARD CONVERTER WITH ZVS BOOST CLAMPING

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***Abstract* – This work presents the study of a three level forward converter with boost active clamping, soft switching (ZVS - Zero Voltage Switching) and constant frequency PWM (pulse width modulation). The main advantages of this topology are high efficiency and lower voltage stress on the switches when compared to forward converters with two level boost clamping.**

Keywords – DC-DC converters, Forward, soft switch, PWM, three levels, ZVS.

I. INTRODUCTION

The use of resonant converters with ZVS has the main objective of reducing switching losses, which allows operation at higher frequencies. However, the main disadvantages of resonant converters [2, 3] are copper losses and higher voltages across the switches. Also, the wider the load variation in these converters, the larger the amount of reactive energy required to maintain the ZVS commutation. The larger amount reactive energy increases the voltage of the auxiliary DC bus. This work focuses on reducing the voltage across the active switches and proposes a structure with a large number of levels.

The two level forward converter with ZVS boost clamping presented in [1] has a significant voltage elevation on the active switches, about 180% of input voltage. This is the reason to elevate to three levels the converter.

The converter proposed has a similar circuit of the reference [6]. However, the forward with clamping boost (forward_boost) has different features in relation to buck with clamping boost (buck_boost) [6].

An initial study of DC-DC multilevel converters with soft commutation (ZVS), active clamping and constant frequency PWM was carried out. The objective of this work is the study of the DC-DC forward converter with three level boost active clamping. Compared to the ZVS two level forward converter [1], shown in Fig. 1, the main advantage of three level topologies is the 50% reduction of the voltage applied across the active switches. References [2, 3] studied several families of two level DC-DC ZVS PWM converters with active clamping that was extended to the three levels in [6, 7]. These converters present characteristics similar to classic PWM converters as the amount of reactive energy consumed by them decreases. In the same way, [1] study the two level forward_boost converter, that was extended in the present work to the three level forward_boost converter with the same features, but applying half of the voltage on the switches.

The forward converter was chosen due to the possibility of using it in applications where the input voltage is relatively high and it is necessary to spread the voltage stresses among the active switches. When low switching losses and low emissions of electromagnetic noise are requirements, it is desirable to operate the converter with ZVS. However, resonant converters increase the voltage of the auxiliary DC bus in relation to the input voltage.

Reference [4] also has presented three level forward converter, which aimed to reduce the voltage across the transistors, but these topologies operate with dissipative commutation.

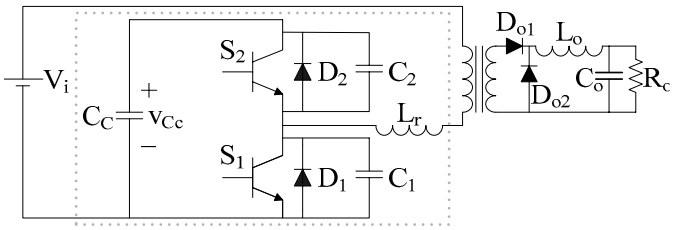

Fig. 1 – Forward with two level ZVS boost clamping.

II. FORWARD CONVERTER WITH THREE LEVEL BOOST CLAMPING

Fig. 2 shows the commutation cells of the forward converter with three level boost clamping.

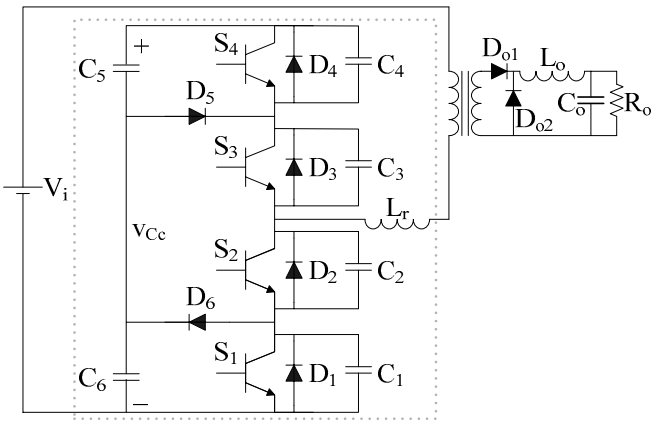

Fig. 2 – Forward converter with three level ZVS boost clamping (forward_boost).

For the initial study of the two and three level topologies, the following considerations are made:

- The converter operates in steady state;
- The switches are considered ideal;
- The converter output inductor is large, thus the load can be represented by a constant current source;
- Inductor L_r stores enough energy to complete the charge and discharge of the resonant capacitors (C_1, C_2, C_3 and C_4 = C_r) and polarize the diodes in parallel with the switches;

- The auxiliary bus capacitance, C_c ($C_c \approx (C_5+C_6)/2$), is much larger than C_r. Thus, the capacitor of the auxiliary DC bus can be represented by a constant voltage source.

To facilitate the converter analysis, Fig. 2 can be redrawn as shown in Fig. 3.

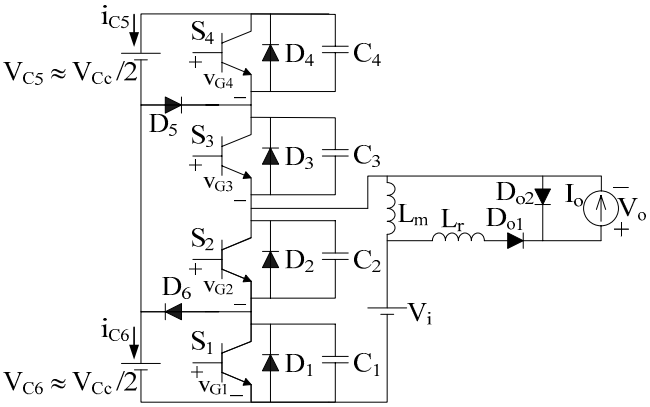

Fig. 3 – Redrawn forward converter with boost clamping.

A. Operation Stages

Fig. 4 shows the drive signals, the currents and the voltages of the switches, considering that the voltages across capacitors C_5 and C_6 are balanced and that at t_4 the voltage across capacitor C_1 reaches $V_{Cc}/2$ and at t_{10} the voltage across capacitor C_4 reaches $V_{Cc}/2$. Even if the conditions above are not satisfied, the converter will operate with ZVS, but with a little difference in the waveforms and operation modes.

The necessary condition for zero voltage switching (ZVS) is to drive each switch when the capacitor in parallel with the switch is discharged. In other words, to avoid dissipative commutation, or hard switching, the drive signals for switches S_1 and S_2 (V_{G1G2}) should start between t_{11} and t_{12} and for switches S_3 and S_4 (V_{G3G4}) should start between t_5 and t_6.

The converter's operation stages presented in Fig. 4 take into consideration the abovementioned restrictions.

Fig. 4 presents the converter's main waveforms, from which each of the converter operation intervals are described.

1st Stage [t_1-t_2] – Switches S_1 and S_2 are conducting. The current through inductor L_r is positive, constant and equal to I_o. Diode D_{o2} is not polarized.

2nd Stage [t_2-t_3] – Switch S_1 is turned off, but S_2 is still conducting. The current is divided among resonant capacitors C_1, C_3 and C_4. In other words, the current through inductor L_r is equal to I_o of which 2/3 circulates through C_1 and 1/3 through C_3 and C_4. The voltage across capacitor C_1 increases from zero to V_x, which is lower than $V_{Cc}/2$, and the voltages across C_3 and C_4 decrease from $V_{Cc}/2$ to ($V_{Cc}/2 - V_x/2$). Voltage V_x depends on the interval between the turn off of switches S_1 and S_2.

3rd Stage [t_3-t_4] – Switch S_2 is turned off and the current through the four resonant capacitors is $I_o/2$. When the voltage across capacitor C_1 reaches $V_{Cc}/2$ the 4th stage begins.

4th Stage [t_4-t_5] – A division of current occurs like in the second stage. The next stage starts when the voltages across capacitors C_3 and C_4 reach zero.

5th Stage [t_5-t_6] – Diodes D_3, D_4 and D_{o2} are polarized. D_3 and D_4 conduct the current through inductor Lr.

6th Stage [t_6-t_7] – The resonant inductor current becomes negative and switches S_3 and S_4 start to conduct.

7th Stage [t_7-t_8] – The output diode D_{o1} is blocked.

8th Stage [t_8-t_9] – In this stage S_4 is turned off and the voltage across C_4 increases from zero to V_x, which is lower than $V_{Cc}/2$, and depends of the interval between the blocks of S_3 and S_4. When switch S_3 turns off the 8th stage begins.

9th Stage [t_9-t_{10}] – The current through the four resonant capacitors is $I_o/2$. This stage ends when the voltage across C_4 reaches $V_{Cc}/2$.

10th Stage [t_{10}-t_{11}] – In this stage diode D_5 is polarized and the voltage across C_3 continues to increase until it reaches $V_{Cc}/2$.

11th Stage [t_{11}-t_{12}] – Diodes D_1 and D_2 are polarized and conduct the resonant inductor current.

12th Stage [t_{12}-t_1] – This stage begins when the resonant inductor current becomes positive. Switches S_1 and S_2 conduct the resonant inductor current, which increases until reaches I_o, initializing the first stage of the operation again.

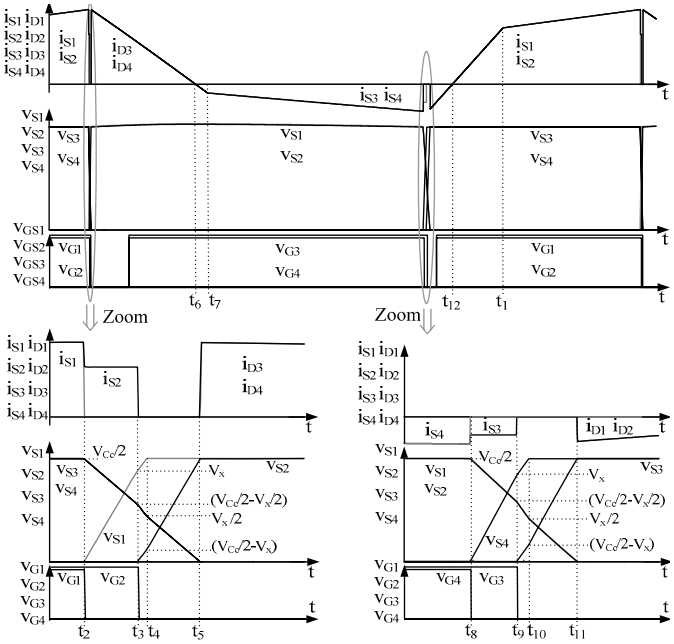

Fig. 4 – Main waveforms of the forward converter with three level ZVS boost clamping.

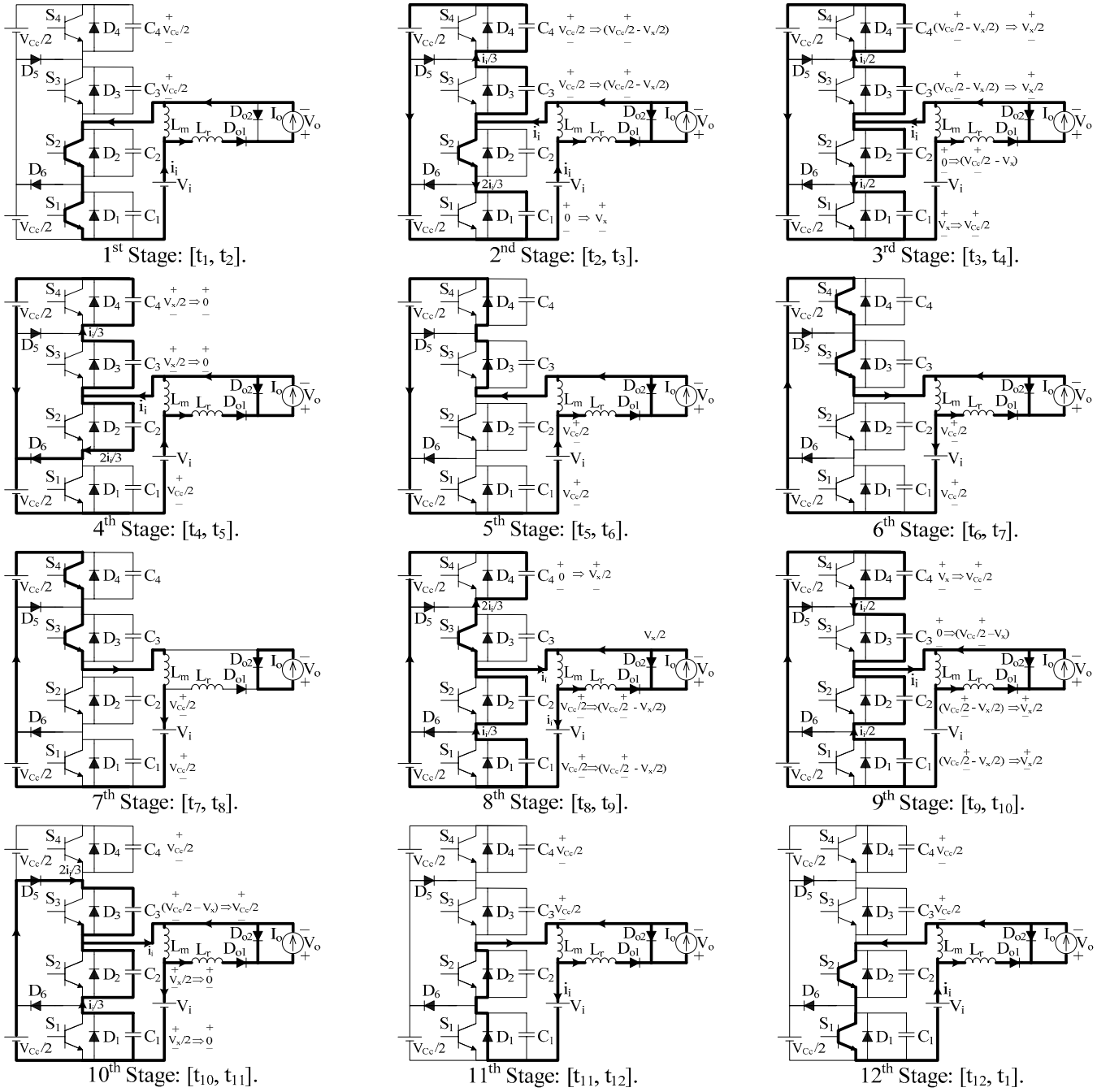

Fig. 5 – Operation stages of the forward converter with three level ZVS boost clamping.

B. Static Transfer Characteristic

To simplify the calculation of the static transfer characteristic, the very short intervals between t_2 and t_5 and between t_8 and t_{11} are ignored. For the analysis, Fig. 4 is redrawn, as presented Fig. 6.

In this figure duty cycle "D" is defined as the interval between the turn off of switches S_3 and S_4 and the turn off of switches S_1 and S_2. This is feasible because the switches do not need to be driven complementarily.

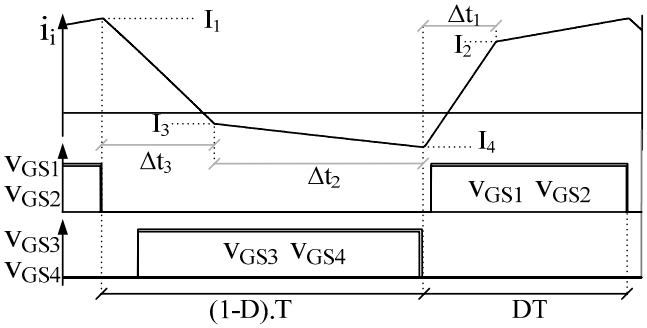

Fig. 6 – Simplified waveforms of the forward converter with three level active boost clamping.

Using these approximations, the static transfer characteristics of the forward converter with two and three level boost clamping are the same.

The input voltage is transferred to the output only during the interval from t_1 until t_2. This way, the equation (1) calculates the output average voltage.

$$V_o = f_s \int_0^{\Delta t_2} V_i \, dt = f_s V_i \Delta t_2 \qquad (1)$$

The intervals Δt_1, Δt_2 and Δt_3 are defined by (2).

$$\Delta t_1 = \frac{I_o L_r}{V_i} \quad \Delta t_2 = \frac{D}{f_s} - \Delta t_1 \quad \Delta t_3 = \frac{I_o L_r (1-D)}{D V_i} \qquad (2)$$

The variables L_n, β and q are defined by (3), (4) and (5).

This normalized inductance, L_n, is dimensionless and was defined as a function of the input voltage, output current and commutation period, as presented in (3).

$$L_n = L_r \frac{I_o}{V_i T_s} \Rightarrow \text{Normalized inductance.} \qquad (3)$$

$$\beta = \frac{V_{Cc}}{V_i} = \frac{1}{1-D} \Rightarrow \text{Relationship between auxiliary DC bus voltage and the input voltage.} \qquad (4)$$

$$q = \frac{V_o}{V_i} \Rightarrow \text{Relationship between output voltage and the input voltage,} \qquad (5)$$

Replacing Δt_2 from (2) in (1) is obtained (6).

$$q = \frac{V_o}{V_i} = D - L_n \qquad (6)$$

Fig. 7 presents the static transfer characteristic of the forward converter with three level boost clamping for different values of duty cycle "D".

β is calculated substituting (4) into (6).

$$\beta = \frac{V_{Cc}}{V_i} = \frac{1}{1-q-L_n} \qquad (7)$$

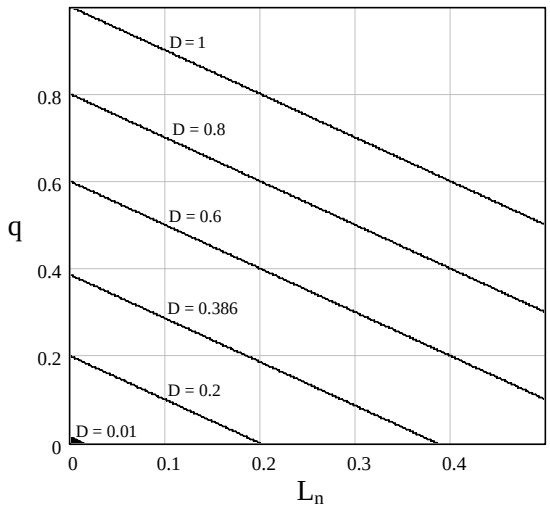

Fig. 7 – Static transfer characteristic.

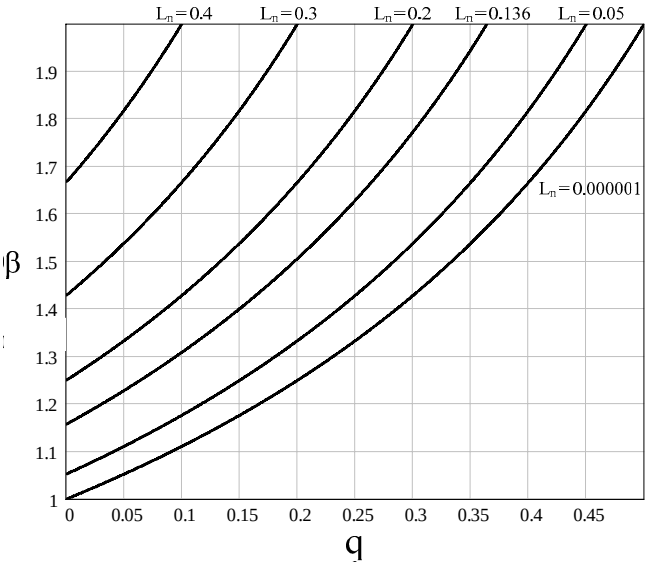

Fig. 8 – Normalized voltage of the auxiliary bus.

Equation (7) is used to plot β for different values of normalized inductance L_n, showed in Fig. 8.

The highest voltage across switches S_1 and S_2 of the forward converter with two level clamping is equal to the auxiliary DC bus voltage V_{Cc}. For the converter presented in Fig. 3 but with three level clamping, the highest normalized voltage applied to the switches is equal to $V_{Cc}/2$. From Fig. 8, the smaller the normalized resonant inductance (L_n), the lower the voltage across the auxiliary bus is.

C. Design

The following specifications were considered for designing the circuit components:

V_i = 300V ⇒ Input voltage
f_s = 20kHz ⇒ Switching frequency
V_o = 75V ⇒ Output voltage
R_o = 16Ω ⇒ Output resistance
ΔV_o = 0.1% ⇒ Output voltage ripple
ΔI_o = 25% ⇒ Input current ripple
ΔV_{Cc} = 0.3% ⇒ Bus voltage ripple
C_r = 2.2nF ⇒ Resonant capacitance C_r (C_1, C_2, C_3 and C_4)
L_m = 6.3mH ⇒ Measured transformer magnetizing inductance
n = 1 ⇒ Transformer relation

In order to choose an adequate value for the resonant inductance, some drive adjustments should be made. The drive signals of switches S_1 and S_2 can be applied right after resonant capacitors C_1 and C_2 discharge, but these drive signals should be applied before the current of inductor L_r becomes positive in order to avoid dissipative commutation. For a better safety margin for the drive circuitry, an inductance of 500 µH was chosen. The minimum inductance

for this design is approximately 200 µH, but this value would be difficult to adjust for a considerable load variation and the converter would end up operating without ZVS.

$L_r = 500\ \mu H \Rightarrow L_n = 0.156$

The duty cycle is calculated isolating D from (6).

$$D = \frac{V_o}{V_i} + L_n \quad \Rightarrow \quad D = 0.406$$

The output power and the output current resistor are calculated by

$$P_o = \frac{V_o^2}{R_o} = 351W$$

$$I_o = \frac{V_o}{R_o} = 4.7\,A$$

The input inductance can be calculated from the current variation in interval t_5 until t_1.

$$L_o = \frac{V_o.\left[\frac{(1-D)}{f_s} + \Delta t_1\right]}{I_o \Delta I_o} \Rightarrow L_o = 2.4mH \Rightarrow \boxed{L_o = 2.5mH}$$

The output capacitor is calculated as in the case of a traditional forward converter.

$$C_o = \frac{V_i}{\pi^3.L_o.\Delta V_o.V_o.f_s^2} \Rightarrow C_o = 129\mu F$$

Due to the current capability specified by the capacitor manufacturers, $\boxed{C_o = 470\mu F}$ was chosen.

Integrating the current through capacitors C_5 and C_6 and using the design specifications and voltage ripples across these capacitors (ΔV_{Cc}), the capacitances are calculated.

$$C_5 = C_6 = \frac{(1-D)I_1^2 \Delta t_3}{V_i \Delta V_{Cc}(I_1 + I_2)}$$

$$C_5 = C_6 = 4.2\mu F \Rightarrow \boxed{C_5 = C_6 = 4.4\mu F}$$

From (7) the average voltage of the auxiliary DC bus is defined as:

$$\overline{V_{Cc}} = \frac{V_i}{(1-D)} \Rightarrow \overline{V_{Cc}} = 505\,V$$

D. Experimental Results

The experimental results of the forward converter with three level boost clamping using the design presented in Fig. 9, are presented in Fig. 10 and Fig 11.

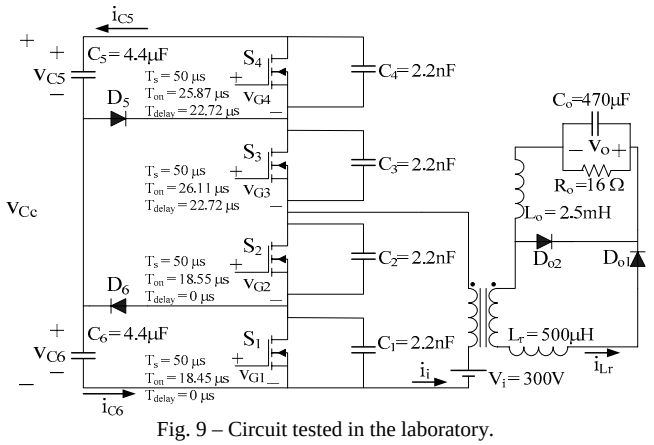

Fig. 9 – Circuit tested in the laboratory.

The prototype tested in the laboratory presented V_o = 75.3V, P_o = 354.4W, $\Delta I_o \approx 0.25 I_o$ and ΔV_o is much smaller than 0.1% because the output capacitor is oversized.

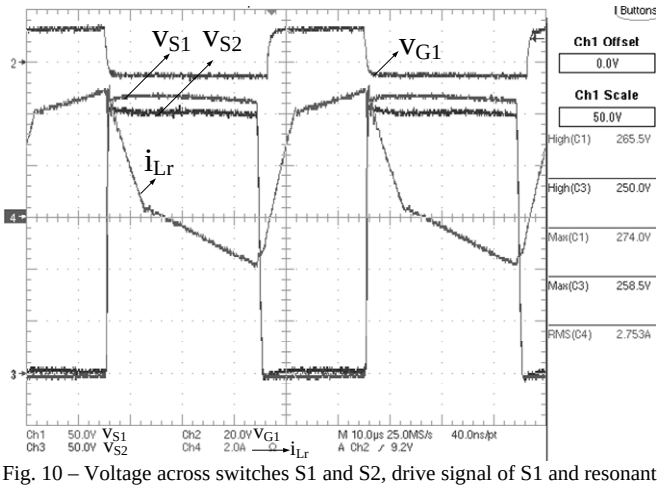

Fig. 10 – Voltage across switches S1 and S2, drive signal of S1 and resonant inductor current.

In Fig. 10 maximum voltage is observed across the switches. The measured maximum voltage was equal to 274V (91% of V_i).

It was noted during the tests under rated power that all of the transistors operate with zero voltage switching (ZVS). The designed converter operates with ZVS from 100% to 25% of the rated power. Below 25%, only turn-on occurs under the zero voltage condition and the additional losses are significant. In Fig. 11 is shown a considerable efficiency sensibility with the conduction losses.

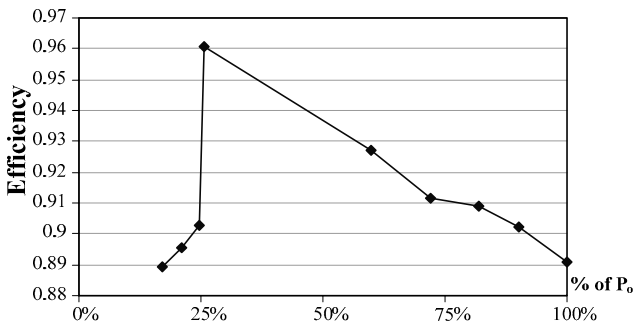

Fig. 11 – Efficiency with load variation.

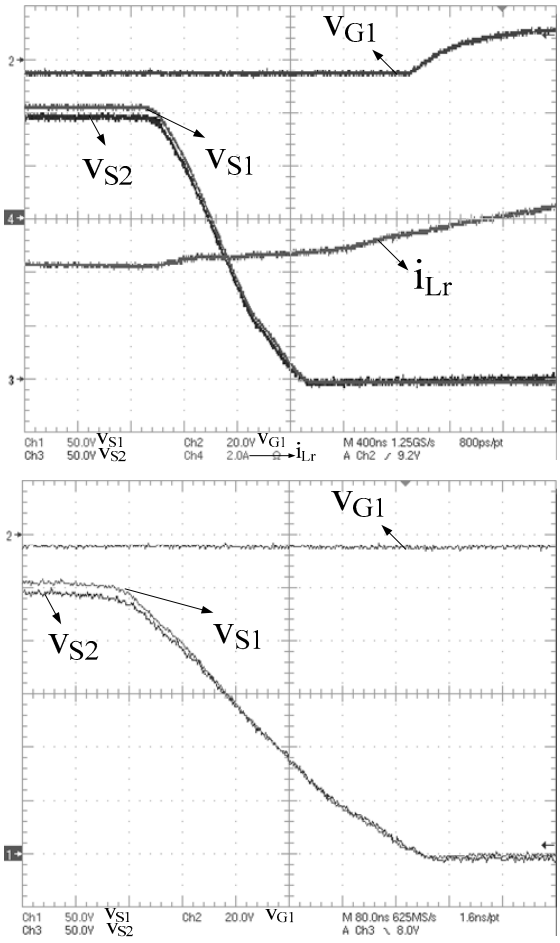

Fig. 12 – Zoom in the turn off transient with zero voltage across the transistors *(P =Po)*.

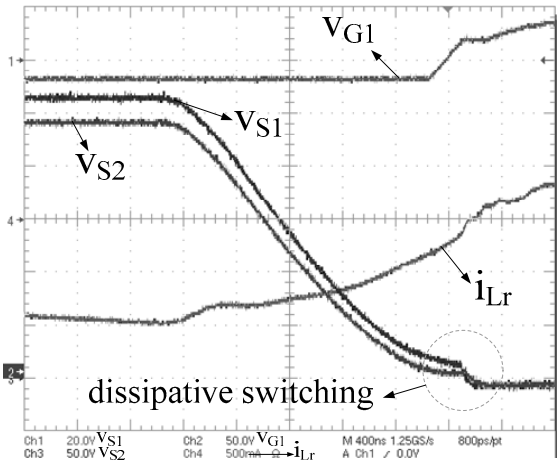

Fig. 13 – Voltage zoom on S_1 e S_2 in the turn off transient with transition non ZVS (P = 0.17.Po).

The commutation details in the switches with nominal power are shown in Fig. 12. Fig. 13 shows the time interval where dissipative switching occurs.

In this design the voltages across capacitors C_5 and C_6, which define the voltage across the switches, are balanced over a wide input voltage range, from zero to V_i.

It was observed that, if the resonant capacitance were reduced, the load range, under which ZVS would occur, increases. However, this would make it difficult for the voltages across C_5 and C_6 to converge to values close to the input voltage.

III. Conclusion

The forward topologies with ZVS have the advantage of reduced commutation losses when compared to a traditional forward converter. Therefore, they operate with higher efficiency at higher frequencies.

Comparing the proposed topology with the forward converter with two level ZVS boost clamping [1], the proposed topology presented a 50% voltage reduction across the switches. However, the three level converter has two additional bidirectional switches and capacitors to compose the auxiliary DC bus. For the two level converter, the voltage across the single bus capacitor is stable because this capacitor is subjected only to the bus voltage, which has a constant average value in steady state. For three or more level converters only the sum of the voltages across the bus capacitors is always stable in steady state, but the average voltage in steady state across each of these capacitors depends on the drive circuit parameters.

Acknowledgment

The authors gratefully acknowledge CNPq (Brazilian National Council of Research) and INEP (Power Electronics Institute - Federal University of Santa Catarina).

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