A SELF-CONTROLLED SINGLE-PHASE VOLTAGE-DOUBLER BOOST USING FPGA

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***Abstract* – This paper presents a strategy for controlling the input current of a single-phase voltage-doubler boost PFC (power factor corrector) implemented by FPGA. A sample of the input voltage is not necessary since it is naturally used as the reference current. This way, the model is more accurate, presenting fewer simplifications and taking better advantage of the natural characteristics of the converter, when compared to classic control, with better results, and many advantages, by simply using a proportional compensator. Some of the advantages of this strategy include greater robustness and simplicity, less susceptibility to noise and a smoother turn-on characteristic. The FPGA used in the project is an ALTERA® Cyclone II EP2C35F672C6, presented on the kit DE2, which is a low-cost FPGA with low-consumption at a great speed.**

***Keywords* – FPGA, Self Control, PFC**

I. INTRODUCTION

The boost converter is commonly used as the input stage of high power factor switch-mode power supplies, performing the AC-DC conversion and receiving the name of single-phase boost PFC. On the classical control strategy the current drained from the mains is controlled by imposing a sinusoidal reference, following the shape of the voltage waveform, independent of the load, and therefore, guaranteeing low current total harmonic distortion and a high power factor.

To this end, the control methodology proposed by Unitrode [1] is traditionally employed, in which an internal current control loop and an external loop to control the average value of the output voltage are used.

For the current loop, it is necessary to generate a convenient reference, either by artificially generating a sinusoid or by sampling the input voltage, since it's desired unity power factor. The voltage loop actually controls the energy provided by the mains to the load by determining the amplitude of the reference current. In practice, in order to obtain good results, it is necessary to use at least a proportional-integral (PI) compensator for the current loop. The voltage loop uses at least an integrator in order to guarantee a zero steady-state error.

Applying digital control to this converter requires the processing time for this stage to be minimum, since the following stage (DC-DC) [4] also needs to be controlled, making possible the use of a higher switching frequency, which is the primary factor for optimizing the converter, consequently reducing its weight, volume, cost, etc.

The self-control strategy, proposed in this article, arises from a more convenient analysis of the boost converter, in which the current feedback is implemented by means of the power stage, using the voltage source as the reference [2] and [3] (similar to [5], [7] and [8]). The great advantage of this control strategy is that the model obtained is much closer to reality, without including any major simplifications.

The models obtained are identical, both for the strategy presented in this work and the traditional strategy presented in [1]. However, with self-control, the model contains fewer simplifications because the effect of the input voltage is now taken into consideration in the analysis, being possible to obtain a power factor close to unity, with low current distortion by only using a proportional feedback, as suggested by both models, although the traditional strategy calls for at least a PI compensator.

There are many advantages to the proposed self-control strategy, being some: it is no longer necessary to sample the input voltage or generate an artificial current reference by any other form; a proportional compensator is used, making the system more robust and reducing processing stress when using digital control, among other advantages that will be presented.

II. TOPOLOGY AND MODELLING

The topology of the voltage-doubler rectifier used is shown in Fig. 1 [9]. Its main characteristics are:

The utilization of two diodes commuted in high frequency constituting the rectifier stage; common capacitive center point; bi-directional switch in current with single command; blocking voltage in the switches is equal to half of the total DC-link voltage (V_{C1}+V_{C2}).

This converter behaves as if composed of two boost (I and II) type converters operating in a complementary manner, since each half cycle of the AC-mains voltage will have the combination of a diode and a switch. In the half cycle where the boost diode (D3 or D4) remains blocked, the connected load on this output is supplied exclusively by the capacitor.

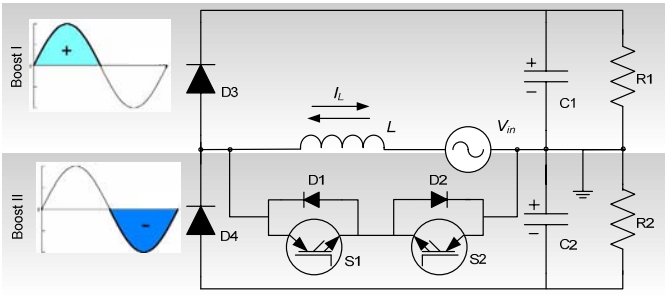


Fig. 1. Single phase boost PFC converter.

The operating stages of this structure can be divided into four, being two for each half cycle of the AC-mains voltage.

A. During the positive half cycle of the input voltage, switch S2 remains turned off

Switch S1 is turned on, initiating the energy accumulation stage of L. On the output stage, each capacitor (C1 and C2) provides energy to the load. Switch S1 is turned off, inductor L and source V_{IN} provides energy to the capacitor C1 and its associated load, through diode D3.

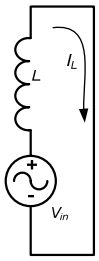
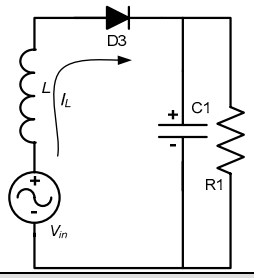
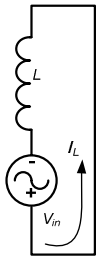
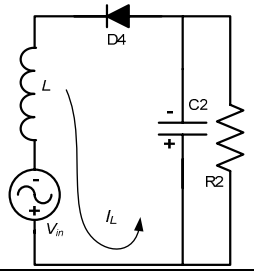
These two stages occur in switch frequency during positive half cycle. The duration of each stage is proportional to the duty cycle.

B. During the negative half cycle of the input voltage, switch S1 remains turned off

Switch S2 is turned on, initiating the energy accumulation stage of L. At the output DC-link, each capacitor is responsible for providing energy to its associated load. Switch S2 is turned off, source V_{IN} and inductor L provide energy to the capacitor C2, through diode D4. These energy transfer and accumulation cycles occur in switch frequency that is proportional to the PWM period.

Using the same command signal for the two switches, the operating stages are present in Table I:

TABLE I
Operations stages

Positive half cycle	
Switches are on	Switches are off
	
Negative half cycle	
Switches are on	Switches are off
	

Adopting the same command signal for the two switches, the voltage on the inductor is given in Table II:

TABLE II
Voltage inductor

Conditions	**$I_L(t) > 0$**	**$I_L(t) < 0$**
$S_1 = S_2 = ON$	$V_L(t) = V_{IN}(t)$	$V_L(t) = V_{IN}(t)$
$S_1 = S_2 = OFF$	$V_L(t) = V_{IN}(t) - V_{C1}(t)$	$V_L(t) = V_{IN}(t) + V_{C2}(t)$

In the initial analyzes of the current loop, the symmetry is admitted in the output voltage and it is despised sweats undulation, so that:

$$V_{C1}(t) = V_{C2}(t) = cte. = V_O \tag{1}$$

This way it is obtained exactly the same model presented for single-phase boost PFC in [10], being applied the self-control, where the current direction will be imposed by the polarity of the input voltage - what is desirable to maintain the current in phase with the input voltage, except for the load angle [10], being controlled only the module of the current:

$$V_L(t) = V_{IN}(t) - [1 - D(t)] \cdot \begin{cases} +V_O \; if \; I_L(t) > 0 \\ -V_O \; if \; I_L(t) < 0 \end{cases} \tag{2}$$

To compensate this nonlinearity, when implementing the self-control, it is used the sample of the rectified value of the current, instead of itself, to define the duty cycle:

$$\begin{aligned} 1 - D(t) &= |k_I \cdot I_L(t)| \\ D(t) &= 1 - |k_I \cdot I_L(t)| \end{aligned} \tag{3}$$

or:

$$1 - D(t) = \begin{cases} +k_I \cdot I_L(t) \; if \; I_L(t) > 0 \\ -k_I \cdot I_L(t) \; if \; I_L(t) < 0 \end{cases} \tag{4}$$

So it is obtained the equivalent system:

$$V_L(t) = V_{IN}(t) - k_I \cdot I_L(t) \cdot V_O \tag{5}$$

Or:

$$\frac{dI_L(t)}{dt} = \frac{V_{IN}(t) - K_I \cdot V_O \cdot I_L(t)}{L} \tag{6}$$

In Fig.2, the expression 6 is represented in form of block diagram.

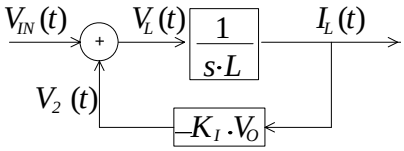


Fig. 2. Block diagram representation of the single-phase voltage-doubler boost PFC converter using the current self-control strategy.

This way the analysis is the same of the single-phase boost PFC, including the optimized displacement angle between voltage and current - the load angle, which for this topology guarantees the non-deformation of the current when crossing zero, since the inductor is on the AC side.

Observations:

- The system is naturally stable, with a pole in the origin (or little to the left if considering the parasite resistances) but with proportional feedback;
- As well as for the classical single-phase boost PFC, relevant ripple in the output capacitors voltage can be reflected as deformations in the input current;
- Asymmetries in the output voltage will be reflected in the semi-cycles of the input current, which could have DC component, that is a characteristic of this topology. However, this control strategy presents a natural feedback for the output voltages balancing, guaranteeing its balance in steady-state, unless the loads is permanently unbalanced.

III. CURRENT SELF-CONTROL STRATEGY

In the traditional input current control strategy [1], the input voltage $V_{IN}(t)$ is treated as a disturbance, not considering it in the modeling of the system.

The self-control strategy [10] proposed for the current loop, not only considers the effects of $V_{IN}(t)$, but also uses it as a part of the current loop, instead of treating it as a disturbance and despising his effects. Since unity power factor is desired, the current drained from the mains should have the same shape as the voltage, in this case sinusoidal. The implementation of the system's feedback is proposed in a way that voltage $V_{IN}(t)$ is treated as the reference and no longer as a disturbance.

The block diagram representation of this proposed strategy is presented in Fig. 2. It should be noted that inductor voltage $V_L(t)$ is naturally defined by $V_{IN}(t)$-$V_2(t)$, and the current is given by the integration of this voltage, so the proposed strategy consists only of making controlled voltage $V_2(t)$ an image of the current. Actually, $V_2(t)$ is being feedbacked and controlled. However, since $V_2(t) = k_I \times I_L(t)$, $I_L(t)$ is effectively being controlled.

Implementing this control strategy is very simple, as shown by Fig. 3. Since the model is now more complete and accurate, the effect of $V_{IN}(t)$ is no longer disregarded, being used as a reference instead, a proportional controller is enough to guarantee that the current will follow the shape of the voltage, since the dynamic model is an integrator, as shown in Fig. 2.

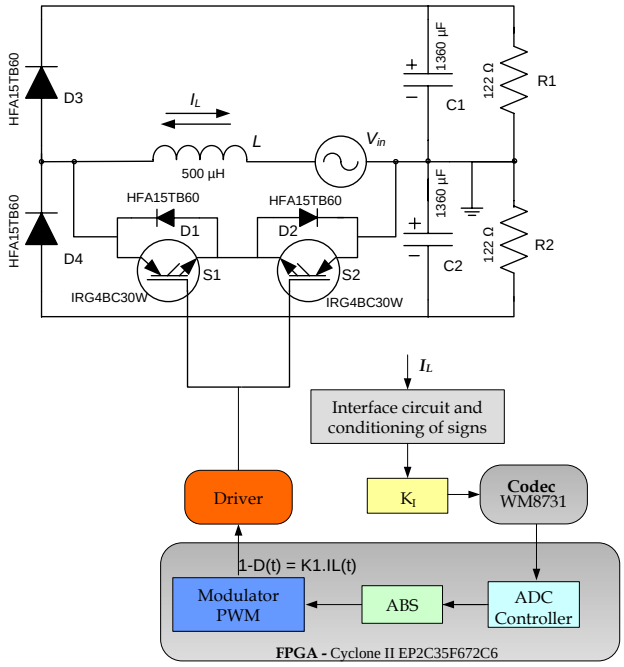


Fig. 3 - Block diagram representation of the single-phase voltage-doubler boost PFC converter using the current self-control strategy.

IV. SIMULATION RESULTS

In order to confirm the principle of the self-control strategy presented here, some simulations were performed using software. Fig. 4 shows the input voltage and current for a sinusoidal supply voltage. In the same figure, it is shown the output voltage across C1 and C2, see Fig 3.

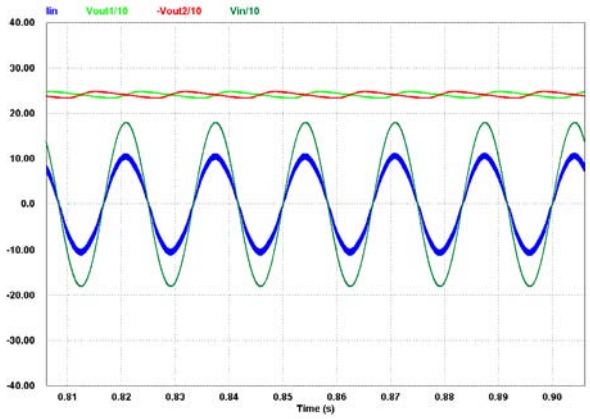


Fig. 4 Input voltage and current and output voltages for a sinusoidal voltage using the self-control strategy.

V. IMPLEMENTED PERIPHERAL

To synthesize the peripheral needed in the project, like the PWM modulator and CODEC control, it was used the hardware-implemented basic peripherals that are available on this FPGA. These peripherals were included on the design of the FPGA, making it capable to do dedicated tasks faster, like multiplication, just like a DSP. The main basic blocks that were used are:

- *18x18 Multipliers*: There are 35 18x18 multipliers, which can be used as 70 9x9 independent multipliers too. These multipliers are capable of implementing common DSP functions such as finite impulse response filters (FIR) and fast Fourier transforms (FFT).
- *Digital PLL*: 4 Digital PLLs, with phase increment resolution of 125ps, and maximum output frequency of 400MHz.

The controller was designed using the Verilog HDL and VHDL languages and the block schematic diagram at the Quartus® II software. In Fig. 5 is shown the top-level entity, which represents all the controller hardware and its sub-modules. The basic peripherals were used to implement these sub-modules, which are the controller basic functions.

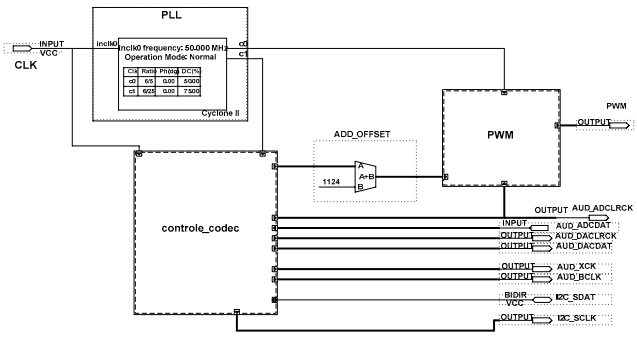


Fig. 5. Self-control implemented in the software Quartus® II.

A. *PWM Modulator*

The block responsible to do the PWM modulation, shown in Fig. 6, is divided in two sub-modules, one of them used to a numerical adjust and the other to make the modulation of the carrier waveform.

The first block, using multipliers and Verilog routines adjusts the value from A/D to fit into the range of the PWM, to obtain the correct modulation.

The second block is composed, basically, by: a flip-flop, triggered by a pulse in the beginning of each sample cycle of the A/D controller, that stores the PWM duty cycle value; a comparator, to obtain the modulation by comparing the carrier with the duty cycle value; an up/down counter, made using Verilog HDL and clocked by a 60MHz clock, which counts up until reach 625 and then counts down to 0, making a triangular waveform, with 48kHz. This waveform is compared to the value in the flip-flop by a comparator block in both up and down cycles, at 96 kHz, improving the controller efficiency. The output of the comparator is the triangular PWM waveform, used to control the switches off the converter.

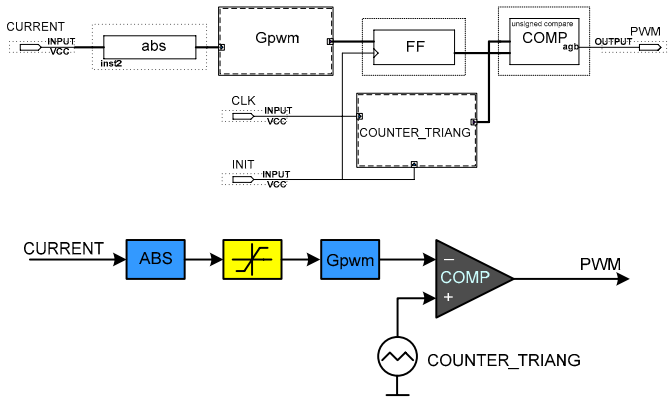


Fig. 6. The PWM modulator implemented in the software Quartus® II.

B. *A/D Converter Controller*

The analog/digital conversion was achieved by using the WM8731 of Wolfson Microelectronics, an audio CODEC (enCOder/DECoder) available in ALTERA® DE2 development kit. The WM8731 has 24-bits sigma-delta ADCs with adjustable word length and sampling rate and two independent input channels, which can be used in DSP applications. In this project it was used a 16-bit word length and a 96 kHz sampling rate.

In order to control and configure the CODEC it was created a general module in the FPGA (CODEC CONTROL), which consists in two distinct submodules (Fig. 7): CONFIG INTERFACE, to configure the CODEC internal registers by an I2C bus and DATA INTERFACE, to control the data transmission from the ADCs through a 3-wire bus. This module works as a master to the CODEC, and treats the received data for further processing by the other modules.

There are four modes to operate the WM8731: left justified, right justified, I2S and DSP mode. For this project the DSP mode was chosen, in which the data transfer is made according to Fig. 8.

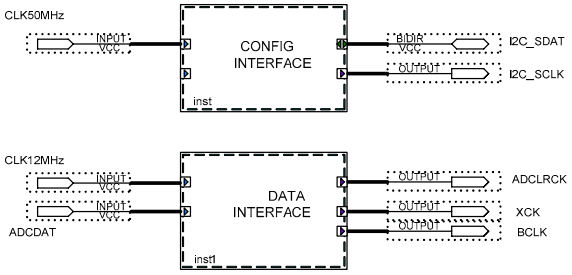


Fig. 7. Codec control submodules, as implemented in the Quartus® II.

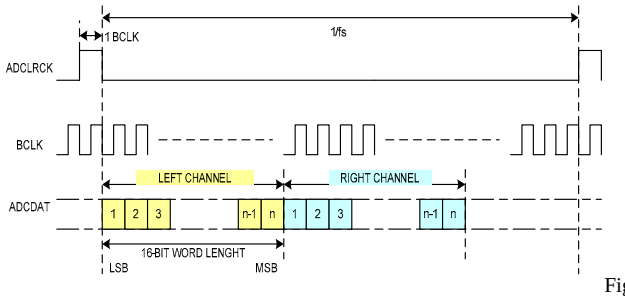


Fig. 8. Data transfer on DSP mode.

A pulse in ADCLRCK starts the serial transmission of the last sample from the ADCs. BCLK is a 12MHz master clock generated by the DATA_INTERFACE submodule and ADCDAT is the serial data line. Each bit (starting with the MSB) is available at the rising edge of BCLK following an ADCLRCK transition low; right channel data immediately follows left channel data. All data transmission is made within 32 BCLK rising edges. ADCLRCK is set every 125 BCLK pulses, to ensure a 96 kHz incoming samples rate. These actions are performed by the DATA INTERFACE sub-module through two state machines (fig 9).

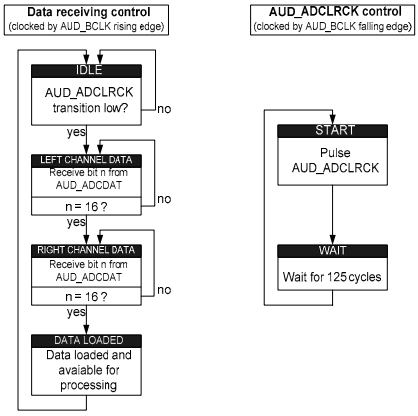


Fig. 9. Data interface State Machines.

VI. EXPERIMENTAL RESULTS

A prototype for the single-phase voltage-doubler boost PFC converter was implemented, applying the self-control strategy to the control loop by means of a FPGA ALTERA® Cyclone II EP2C35F672C6. The characteristics of the implemented prototype were:

- Output power: 1kW;
- Peak input voltage (sinusoidal) 180 V;
- Output voltage: 450V;
- Line frequency: 60Hz;
- Boost inductor: 500 µH.

The line voltage presented a 2.58 % total harmonic distortion, having obtained a 3.78% THD for the current. Fig. 10 shows the waveforms of the input voltage and current and the output voltage in steady-state.

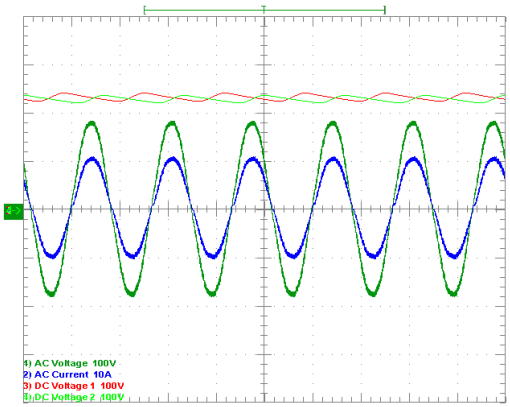


Fig. 10. Steady-state input voltage with current and output voltages.

Fig.11 and Fig.12 show the harmonic analysis of the voltage and current waveform. The calculated power factor in this case was 0.998.

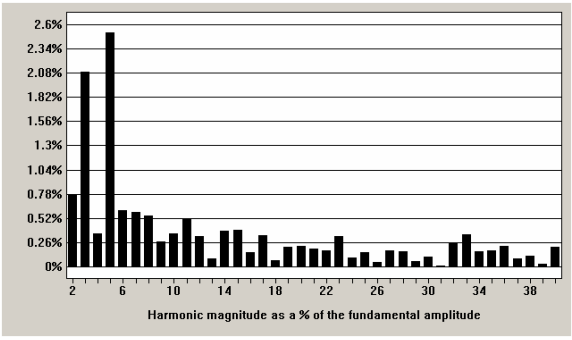


Fig. 11. Harmonic analysis of the current waveform.

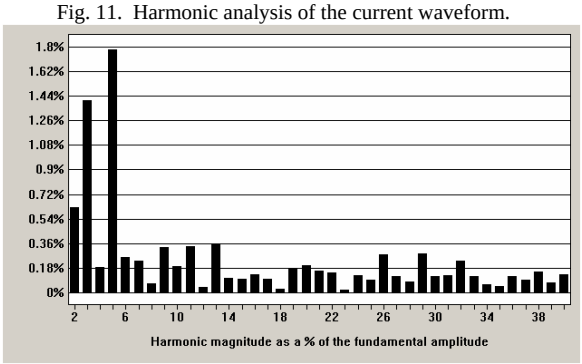


Fig. 12. Harmonic analysis of the voltage waveform.

VII. CONCLUSION

The single-phase boost PFC converter, using the classic control strategy, requires that a sinusoidal reference for the current is created, by using a sample of the input voltage or an external sinusoid. On the other hand, the self-control strategy proposed eliminates the need of this reference, making the current following the shape of the input voltage.

Besides this, the classic control strategy does not include the input voltage in its model, treating it as a disturbance. Since the model is not very accurate, it is necessary to use different compensators from those designed for this model, where a proportional compensator should have been enough to guarantee a good quality for the current. However, it is necessary to use at least a PI (proportional-integral) compensator, in which the integrator should guarantee the positioning of a set point to annul the disturbance of the input voltage, yet still demanding adjustments in the prototype due to the imprecision of the model.

The self-control strategy uses a precise model and not an approximated small-signal one. It does not treat the input voltage as a disturbance but conveniently uses it as the reference. Therefore, a proportional compensator guarantees good results, making the system robust, less susceptible to noise, besides being easy to reproduce on an industrial scale since it does not require adjustments once built.

This paper has proposed the use of FPGA-based control for a voltage doubler rectifier, taking into consideration the power factor correction. The final result is a high power factor converter.

The proposed strategy, besides all of the advantages presented that effectively improve the dynamics of the system, allows not only the use of simpler signal processors or even microcontrollers and FPGA, but also brings about the development of a new simpler and cheaper dedicated integrated circuit, making implementation and reproduction on an industrial scale easier and increasing robustness.

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