A TWO STAGE DC-AC CONVERTER WITH WIDE INPUT VOLTAGE RANGE

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***Abstract* – This work presents the analysis, design, simulation, and experimental development of a single-phase inverter with high frequency transformer isolation and for a wide input voltage range. The high frequency input current ripple is mitigated by the use of a small input LC filter, and the low frequency current component injected by the inverter is attenuated by the voltage loop controller. The proposed topology can be used in dc voltage-sourced applications such as renewable energy and battery systems.**

***Keywords* – DC-AC Convertion, High Frequency Isolation, Wide Input Voltage Range Operation.**

I. INTRODUCTION

Inverters are particularly one of the most significant and studied class of static power converters. Typical applications are distributed generation, ac motor drives, and UPS systems. Several topologies are available in the literature, which can be classified according to the following categories:

- Number of phases: single-phase or three-phase;
- Adjustment of the output voltage;
- Commutation of the switches: hard or soft;
- Presence or absence of isolation transformer;
- Number of power stages [1].

The topology proposed in this work has the characteristics of adjustment of the output voltage, hard commutation of the main switches, and isolation.

A. Single-Stage Topologies versus Mutiple-Stage Topologies

DC-AC converters can be classified in either single-stage or multiple-stage topologies. A single-stage DC-AC converter is responsible not only for the output voltage adjustment, but also for PWM drive of the switches. A typical example is the dual flyback inverter, shown in Fig. 1 [2].

A multiple-stage dc-ac converter is formed by several converters where each one has a specific function, e.g. output voltage adjustment and/or isolation and/or dc-ac conversion. They can be classified in three types: dc-ac-ac converters (Fig. 2), dc-dc-ac converters (Fig. 3), or dc-ac-dc-ac converters (Fig. 4).

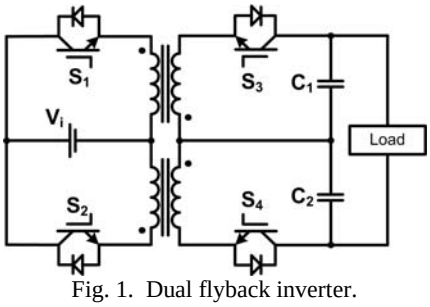

Fig. 1. Dual flyback inverter.

Single-stage dc-ac converters are typically used in low power applications, and are not the scope of this work, which is focused on dc-ac-dc-ac structures.

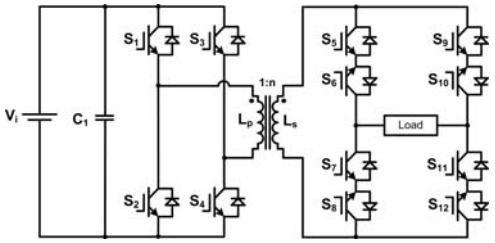

Fig. 2. Example of a dc-ac-ac topology [3].

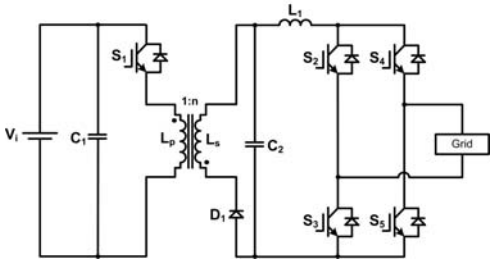

Fig. 3. Example of a dc-dc-ac topology.

II. PROPOSED TOPOLOGY

Fig. 4 shows the block diagram representing a dc-ac-dc-ac system. It is formed by three power stages, as each one of them can be implemented using a classical topology. One is supposed to define which structures must be employed.

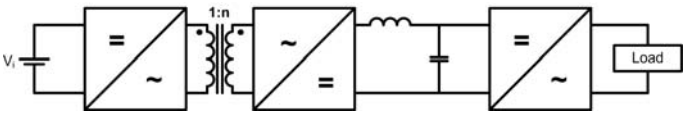

Fig. 4. Block diagram of a DC-AC-DC-AC system.

The complete schematic of proposed topology is shown in Fig. 5. A classical push-pull converter is used in the first stage, because the switches are not turned on simultaneously, and also due to the intrinsic isolation.

A full-bridge rectifier is chosen in the second stage, due to the absence of central tap and the reduced blocking voltage across the diodes. To further reduce the blocking voltage, two secondary windings are employed in the transformer of the push-pull converter.

The third stage is composed by a full-bridge inverter, once that a push-pull arrangement would require an additional low frequency transformer. A half-bridge topology is not adequate as well, due to the doubled input voltage.

Three LC filters are employed. The first one is placed between the primary voltage source and the first stage, in order to assure reduced high frequency ripple of the input current. The second one is placed between the second and

third stages, to provide the dc voltage link to the full-bridge inverter and also mitigate high frequency current flow through the previous stages. The last filter is placed in the load side.

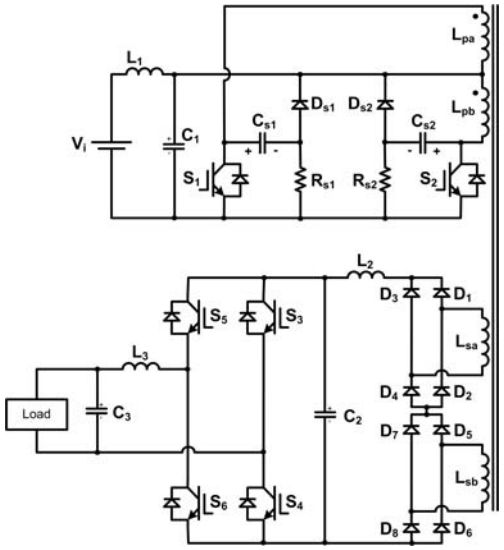

Fig. 5. Proposed topology.

A dissipative RCD snubber is employed in the switches of the push-pull converter to preserve the semiconductor devices due to eventual voltage overshoot caused by the leakage inductance of the high frequency transformer.

III. DESIGN PROCEDURE

The prototype specifications are shown in Table I.

TABLE I
Prototype specifications and design assumptions

Input voltage range	V_i=60-90 V
Rms output voltage	V_o=220 V_{rms} +/-5%
Output voltage THD	<5%
Apparent power	S_o=400 VA
Load power factor	PF=1
Output frequency	f_r=400 Hz
Modulation index	Ma=0.75
Maximum input current ripple	ΔI_i=6%
Maximum input voltage ripple	ΔV_i=3 V
Efficiency (push-pull converter)	η_1=0.9
Efficiency (full-bridge converter)	η_2=0.9
Switching frequency (push-pull converter)	f_1=40 kHz
Switching frequency (full-bridge converter)	f_2=40 kHz

A. Power Circuit Design

For the power circuit design, classical methodology as described in [10][11][12] was used.

The peak value of output voltage (V_{o_pk}) is given by (1).

$$V_{o\_pk} = \sqrt{2} \cdot V_o \cong 311\ V \quad (1)$$

The input voltage of third stage (V_r) is given by (2).

$$V_r = \frac{V_{o\_pk}}{M_a} \rightarrow V_r \cong 420\ V \quad (2)$$

Considering the maximum duty cycle in the push-pulll converter equal to 0.45, the minimum turns ratio (n) is given by (3).

$$n > \frac{V_r}{2 \cdot D_{\max} \cdot V_{i\_\min}} \rightarrow n > 7.78 \quad (3)$$

By convenience, the transformer turns ratio is chosen:

$$n = 8 \quad (4)$$

Thus the minimum duty cycle (D_{min}) in the push-pull converter is given by (5).

$$D_{\min} = \frac{V_r}{2 \cdot n \cdot V_{i\_\max}} \rightarrow D_{\min} \cong 0.29 \quad (5)$$

The peak current drained by the push-pull converter is given by (6).

$$I_{sh\_pk} = \frac{S_o \cdot PF \cdot n}{\eta_1 \cdot \eta_2 \cdot V_r} \rightarrow I_{sh\_pk} \cong 9.52\ A \quad (6)$$

The maximum and minimum average currents through the primary voltage source (I_{i_max} and I_{i_min}, respectively) are given by (7) and (8), respectively.

$$I_{i\_\max} = \frac{S_o \cdot PF}{\eta_1 \cdot \eta_2 \cdot V_{i\_\min}} \rightarrow I_{i\_\max} \cong 8.33\ A \quad (7)$$

$$I_{i\_\min} = \frac{S_o \cdot PF}{\eta_1 \cdot \eta_2 \cdot V_{i\_\max}} \rightarrow I_{i\_\min} \cong 5.56\ A \quad (8)$$

The rms current through filter capacitor C1 is given by (9).

$$I_{C1\_rms} = I_{sh\_pk} \cdot \sqrt{2 \cdot D_{\min} \cdot (1 - 2 \cdot D_{\min})} \rightarrow I_{C1\_rms} \cong 4.7A \quad (9)$$

The maximum equivalent series resistance of capacitor C1 (R_{C1}) is given by (10).

$$R_{C1} < \frac{\Delta V_i}{I_{sh\_pk}} \rightarrow R_{C1} < 315\ m\Omega \quad (10)$$

The filter inductance (L1) is given by (11).

$$L1 = \frac{\Delta V_i \cdot D_{\max}}{\Delta I_i \cdot I_{i\_\min} \cdot f_1} \rightarrow L1 = 100\ \mu H \quad (11)$$

The rms value current through capacitor C2 is obtained by simulation and given by (12).

$$I_{C2\_rms} \cong 2\ A \quad (12)$$

The peak output current (I_{o_pk}) is given by (13).

$$I_{o\_pk} = \sqrt{2} \cdot \frac{S_o \cdot PF}{V_o} \quad (13)$$

Considering the voltage ripple across C2 as 1% of V_r, the maximum equivalent series resistance of C2 (R_{C2}) is given by (14).

$$R_{C2} < \frac{0.01 \cdot V_r}{I_{o\_pk}} \rightarrow R_{C2} < 1.6\ \Omega \quad (14)$$

The cut-off frequency of the second filter (f_{f2}) must be established one decade below the low frequency current ripple and the voltage transients must be verified under input voltage steps. For the given example this frequency is defined as 110 Hz, and then inductance L2 is given by (15).

$$L2 = \frac{1}{\left(2 \cdot \pi \cdot f_{f2}\right)^2 \cdot C2} \rightarrow L2 = 21\ mH \quad (15)$$

Considering the current ripple through inductor L3 as 35% of I_{o_pk}, the respective inductance is given by (16).

$$L3 = \frac{\left(V_r - \sqrt{2}\cdot V_o\right)\cdot M_a}{0{,}35\cdot I_{o\_pk}} \rightarrow L3 = 2.27\ mH \qquad (16)$$

In order to get a cut-off frequency around 4kHz in the third filter, filter capacitance C3 can be obtained from (17).

$$C3 = \frac{1}{(2\cdot\pi\cdot f_{f3})^2\cdot L_3} \rightarrow C3 \cong 700\ nF \qquad (17)$$

Table II lists the components used in the prototype.

TABLE II
COMPONENTS LIST

C1	B43504-A2477-M000 (470uF/250Vdc)
C2	B43501-A5107-M000 (100uF/450Vdc)
C3	B32654-A6105-J000 (1uF/250Vac)
S1 e S2	IRFP460A
S3 to S6	IRGB20B60PD1

B. Push-Pull Control Loop Design

The transfer function of the dc-dc converter is shown in (18) and the respective Bode diagram is shown in Fig. 6.

$$G_{sh}(s) = k_d \cdot \frac{s + \frac{1}{\omega_{zsh}}}{\frac{1}{\omega_{osh}^2}\cdot s^2 + \frac{1}{\omega_{osh}\cdot Q_{sh}}\cdot s + 1} \qquad (18)$$

Where,

$$K_d = n\cdot V_i \qquad (19)$$

$$\omega_{zsh} = \frac{1}{C2\cdot R_{C2}} \qquad (20)$$

$$\omega_{osh} = \frac{1}{\sqrt{L2\cdot C2}}\cdot\sqrt{\frac{R_{osh}}{R_{osh}+R_{C2}}} \qquad (21)$$

$$R_{osh} = \frac{V_r\cdot\eta_2}{P_o} \qquad (22)$$

$$Q_{sh} = \frac{\sqrt{L2\cdot C2\cdot R_{osh}\cdot(R_{osh}+R_{C2})}}{C2\cdot R_{osh}\cdot R_{C2} + L2} \qquad (23)$$

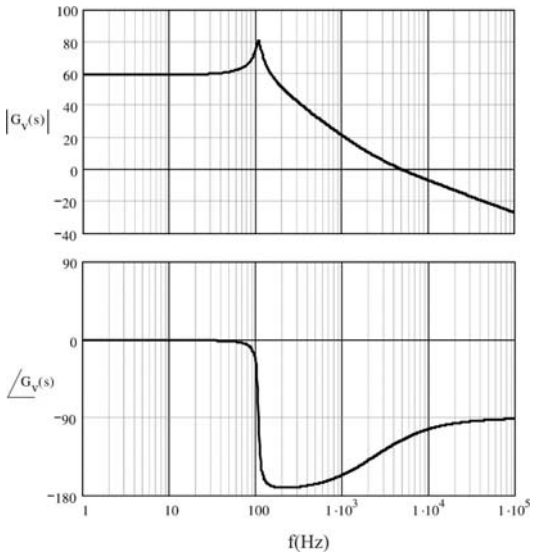

Fig. 6. Bode diagram of $G_{sh}(s)$.

The open loop transfer function $G_{sh}(s)$ is given by (24).

$$FTLA(s) = G_{sh}(s)\cdot F_m\cdot H(s) \qquad (24)$$

where H(s) is the feedback transfer function and F_m is the modulator gain:

$$H(s) = \frac{V_{ref}}{V_r} \qquad (25)$$

$$F_m = \frac{1}{V_{ref}} \qquad (26)$$

As the control goals are null steady state error and the mitigation of the low frequency ripple of the current through the inverter, a simple PID controller, shown in Fig.7, whose transfer function is given by (28), can be used.

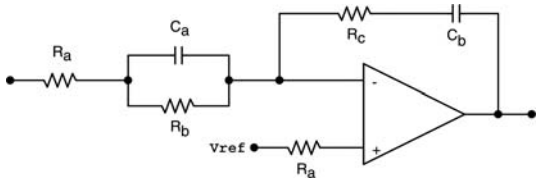

Fig. 7. Push-pull controller.

$$C_{sh}(s) = K_V\cdot\frac{(s+\omega_{osh})\cdot(s+\omega_{osh})}{s\cdot(s+\omega_{zsh})} \qquad (28)$$

The poles and zeros of the controller match those of the system, and an additional pole added at the origin establishes null error in the steady state.

Then gain K_v must establish a crossing frequency about 150 Hz, in order to attenuate the 800 Hz current ripple.

$$K_V = \frac{1}{FTLA(2\cdot\pi\cdot f_C)\cdot T(2\cdot\pi\cdot f_C)} \qquad (29)$$

Where,

$$T(s) = \frac{(s+\omega_{osh})\cdot(s+\omega_{osh})}{s\cdot(s+\omega_{zsh})} \qquad (30)$$

Then,

$$K_V \cong 5.6 \qquad (30)$$

The controller components can be obtained from expressions (31) to (34), and the resulting transfer function $FTLAC_{sh}(s)$ is shown in Fig. 8.

$$R_c = K_v\cdot R_a \rightarrow R_c = 5.6\ k\Omega \qquad (31)$$

$$C_b = \frac{1}{\omega_{osh}\cdot R_c} \rightarrow C_b = 270\ nF \qquad (32)$$

$$R_b = R_a\cdot\left(\frac{\omega_{zsh}}{\omega_{osh}} - 1\right) \rightarrow R_b = 22\ k\Omega \qquad (33)$$

$$C_a = \frac{1}{\omega_{osh}\cdot R_b} \rightarrow C_a = 68\ nF \qquad (34)$$

C. Inverter Control Loop Design

The transfer function of the dc-ac converter is given by (35).

$$G_{fb}(s) = V_r\cdot\frac{1}{L_3\cdot C_3\cdot s^2 + \frac{L_3}{R_o}\cdot s + 1} \qquad (35)$$

Where,

$$R_o = \frac{V_o^2}{S_o \cdot PF} \qquad (36)$$

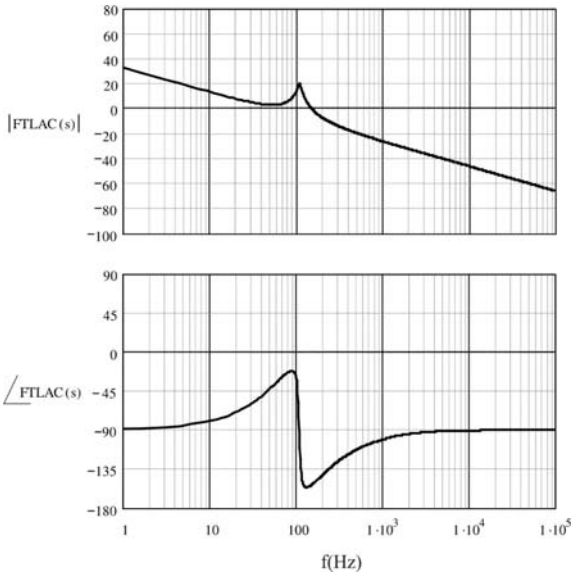

Fig. 8. Bode diagram of $FTLAC_{sh}(s)$.

The feedback gain and the modulator gain are given by (37) and (38), respectively.

$$H(s) = \frac{1}{100} \qquad (37)$$

$$F_m = \frac{1}{V_{ref}} \qquad (38)$$

The open loop transfer function $G_{fb}(s)$ ($FTLA_{fb}(s)$) is given by (39), and the respective Bode diagram is shown in Fig. 9.

$$FTLA_{fb}(s) = G_{fb}(s) \cdot F_m \cdot H(s) \qquad (39)$$

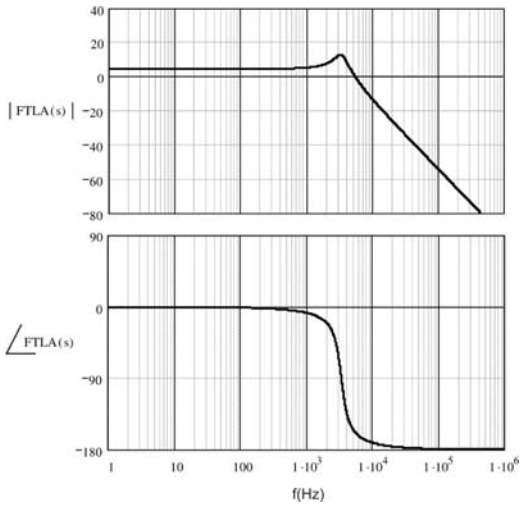

Fig. 9. Bode diagram of $FTLA_{fb}(s)$.

Then, the controller transfer function is given by (40), which is shown in Fig. 10.

$$C_{fb}(s) = K_V \cdot \frac{(s+\omega_{ofb}) \cdot (s+\omega_{ofb})}{s} \qquad (40)$$

Establishing the cross-over frequency as 8 kHz, the controller gain is given by (42). By choosing Ra=470kΩ, the controller components can be obtained from expressions (43) to (45).

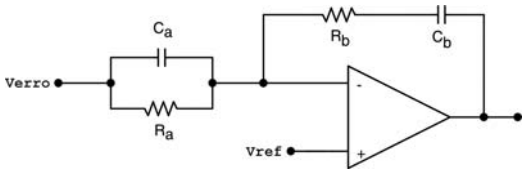

Fig. 10. Inverter controller.

$$K_V \cong 37 \times 10^3 \qquad (42)$$

$$C_a = \frac{1}{\omega_{ofb} \cdot R_a} \rightarrow C_a = 100\ pF \qquad (43)$$

$$C_b = \frac{1}{K_V \cdot R_a} \rightarrow C_b = 22\ nF \qquad (44)$$

$$R_b = \frac{1}{\omega_{ofb} \cdot C_b} \rightarrow R_b = 2.2\ k\Omega \qquad (45)$$

Then, the Bode diagram of the open loop system with the designed controller $FTLAC_{fb}(s)$ is shown in Fig. 11.

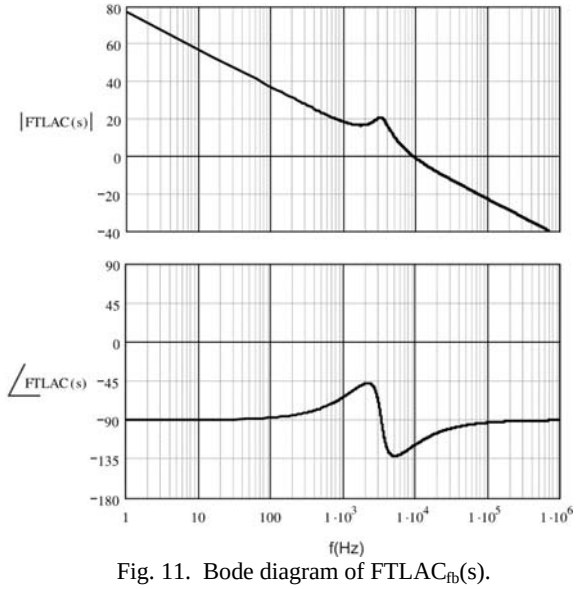

Fig. 11. Bode diagram of $FTLAC_{fb}(s)$.

IV. EXPERIMENTAL RESULTS

From an experimental prototype designed with the specifications given in Table I, some results are presented and discussed in this section. In Fig. 12 one can see a low input current ripple through inductor L1 and low voltage ripple across capacitor C1. Both them can be reduced even more by the accurate design of the input filter, if necessary.

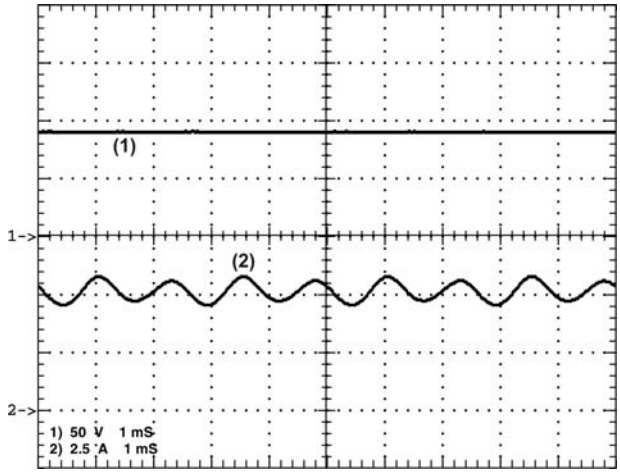

Fig. 12. Input current ripple and voltage ripple across the filter capacitor.

Fig. 13 shows that the voltage across the switches of the push-pull stage does not contain considerable voltage peaks and stresses. The current waveform presents some oscillation due to the reverse recovery of the output diodes, but it is considered acceptable.

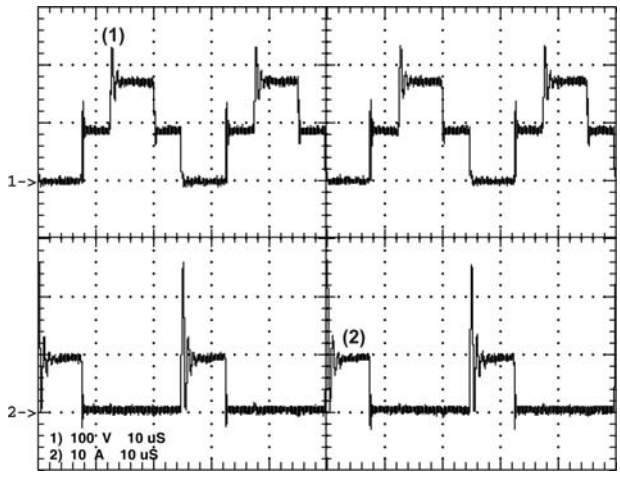

Fig. 13. Current through the primary winding and voltage across the switch in the push-pull converter.

The Fig. 14 shows the input current drained by the inverter.

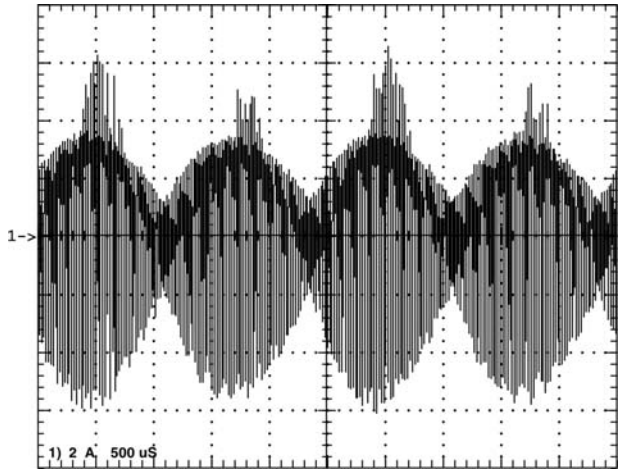

Fig. 14. Input current waveform of the inverter.

It can be seen that despite of the presence of high frequency and low frequency components, the ripple is not significant to the push-pull converter, and the low frequency ripple is attenuated in the current through L1, due to the voltage loop and the filter formed by L2 and C2.

Fig. 15 shows the inverter output voltage with low THD (below 2.5%), and also the current through output inductor L3.

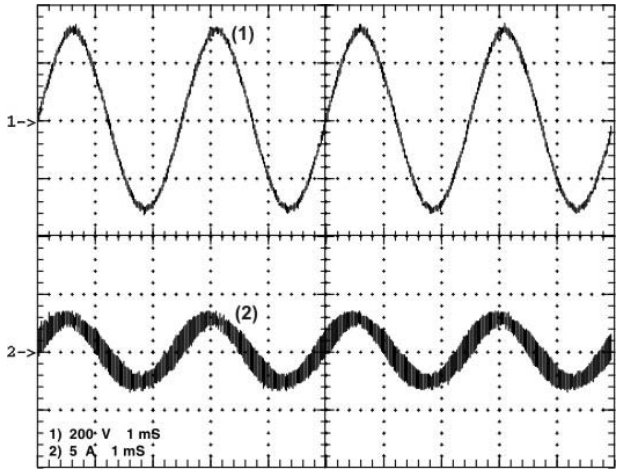

Fig. 15. Current through the filter inductor and output voltage.

In Fig. 16 it can be seen an optimum load step response from 10% to 100% of the rated load.

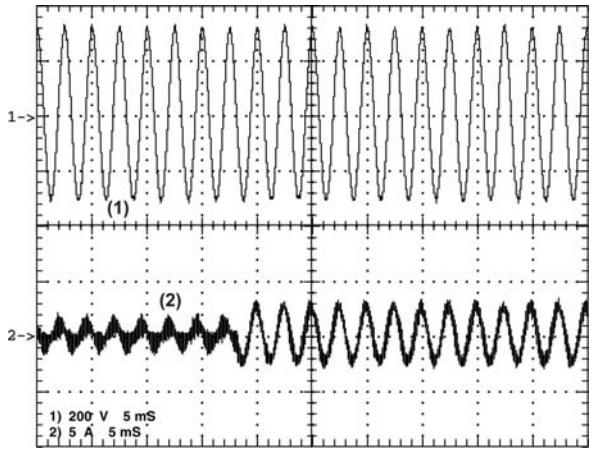

Fig. 16. Current through the filter inductor and output voltage for a load step (10% to 100% of the rated power).

Fig. 17 shows the output voltage for a nonlinear load.

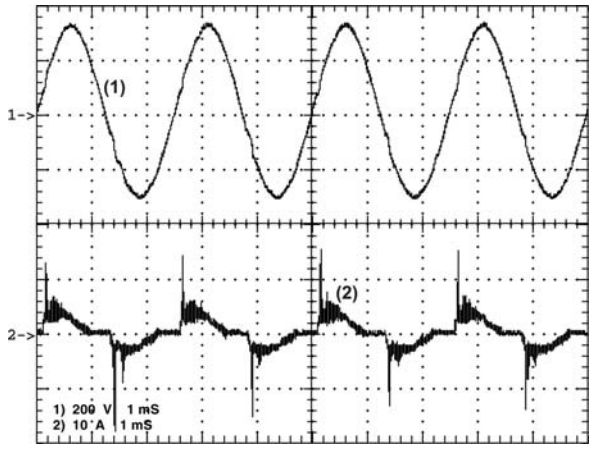

Fig. 17. Load current and output voltage for nonlinear load.

The harmonic spectrum is shown in Fig. 18 and the total harmonic distortion is about 3%.

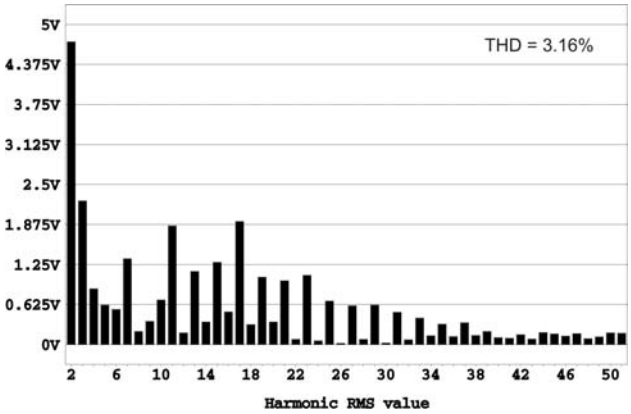

Fig. 18. Harmonic spectrum of the output voltage for nonlinear load.

In Fig. 19 one can see the obtained efficiency curve. Although the efficiency is greater than that specified in the design, it can be optimized by some experimental improvements, as the adjustment of the push-pull switching frequency and the use of MOSFET's with reduced on-resistance.

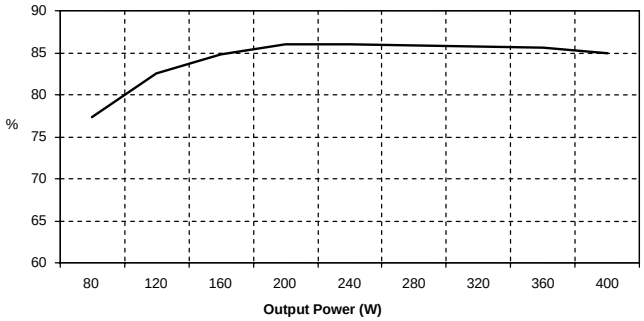

Fig. 19. Efficiency curve.

In Fig. 20 one can see the commercial prototype developed.

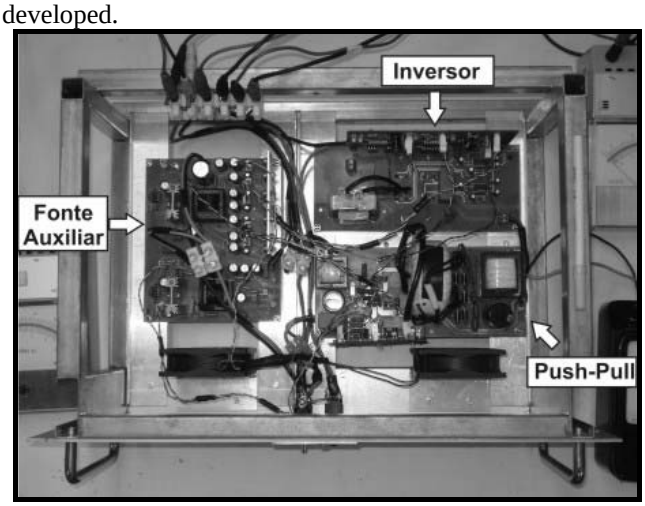

Fig. 20. Prototype picture.

V. CONCLUSION

This paper has presented a topology feasible for dc voltage sourced systems, where small input current ripple is necessary and high input voltage range exists. The low frequency component of the current injected by the inverter is attenuated by the LC output filter of the push-pull converter and by the design of the respective voltage loop controller. The work has been supported by experimental results showing the low input current ripple, low output voltage THD, and high efficiency.

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