THREE-STATE SWITCHING CELL APPLIED TO THE PWM BUCK CONVERTER OPERATING AT OVERLAPPING MODE

Juan P. R. Balestero*, Falcondes J. M. de Seixas**, Thiago N. Santelo**, Grover Torrico_Bascopé***

(*) CEFETSC – Federal Center of Technological Education of Santa Catarina
Av. Nereu Ramos, 3450-D – 89813-000 – Chapecó-SC, Brazil Phone: - Fax: +55-49-3331-4651
www.cefetsc.edu.br - juan@cefetsc.edu.br

(**) UNESP - São Paulo State University
Department of Electrical Engineering - www.dee.feis.unesp.br
P.O. Box 31 – 15385-000 - Ilha Solteira SP, Brazil Phone: +55-18-3743-1150 - Fax: +55-18-3743-1163
falcon@dee.feis.unesp.br

(***) Eltek Energy AB - Hammarbacken 4A, 191 24, Sollentuna
Stockholm, Sweden - www.eltekvalere.com
grover.torrico@eltekvalere.com

Abstract: **This paper presents a new approach on the three-state switching cell (TSSC) applied to the PWM buck converter operating at overlapping mode. In this converter only part of the load energy is processed by the active switches, reducing the peak current through these switches to half of the peak of the load current. This characteristic enables this topology to operate at higher power levels. The volume of reactive power elements (inductors and capacitors) is also decreased since the ripple frequency of the output voltage is twice the switching frequency. For lower operating frequency, switching losses are decreased. Another advantage of this converter is the smaller region to operate in discontinuous conduction mode when compared with the conventional buck converter or, in other words, the operation range in continuous conduction mode is enlarged. From the mathematical analysis and development by digital simulation, a 1kW prototype was implemented and tested in laboratory. The main experimental results are introduced and discussed in this paper, for duty cycle greater than 0.5 (the switches can operate simultaneously).**

Keywords: **Buck Converter, dc-to-dc converter, PWM, Three-state switching cell, TSSC.**

I. INTRODUCTION

Pulse-width modulated (PWM) converters are currently used in several DC-DC conversion applications [1] -[3] . Widespread applications of DC-DC converters include power supplies for a countless variety of electronic systems, telecommunication energy systems, solar energy applications, DC motor drivers and satellite energy systems. Also, DC-DC converters are often found as basic building blocks for other types of power converters [4] -[5] .

The conventional PWM converters (at hard commutation) present low power density, even though by using the power mosfets associated with commonly large heat sink, and because the capacitor and inductor filters are operating in lower switching frequency. Despite of the possibility of the mosfet to operate in higher switching frequencies, the operation with high power becomes impossible, since it increases the switching losses and also reduces the efficiency. In addition, the leakage inductances of the circuit and the capacitances of the semiconductor junctions affect the converter performance strongly. The effects of the leakage inductances are seem in the turning off process while the intrinsic capacitances affect the turning on of the semiconductors. The energy stored in the junctions is all dissipated in the semiconductors. Therefore, the facts written before limit the increase of the switching frequency in PWM converters with hard commutation.

The proposed buck converter operating at overlapping mode is able to process higher power than the conventional topology because it drives the switches with lower switching frequency and only part of the load energy is processed by the active switches. The volume of the reactive power elements (inductors and capacitors) is also decreased since the ripple frequency of the output voltage is twice the switching frequency. Another advantage of this converter is the smaller region to operate in discontinuous mode when compared with the classical buck converter. Generally, the DCM region is undesirable because it presents inherent nonlinearity and it becomes difficult to control the converter. In this paper, a systematic analysis, design and experimental results in CCM operation are provided.

II. OPERATION OF THE PROPOSED CIRCUIT

In [1] the three-state switching cell was proposed. It is composed by two switches (S1, S2), two diodes (D1, D2), and one transformer formed by two coupled inductors (T) or called autotransformer too. Fig. 1 shows the cell with its bilateral inversion of it.

Substituting the three-state switching cell from Fig. 1 into of the two-state switching cell of the classic buck topology Fig. 2 (a), the proposed buck converter is obtained, as shown in Fig. 2(b).

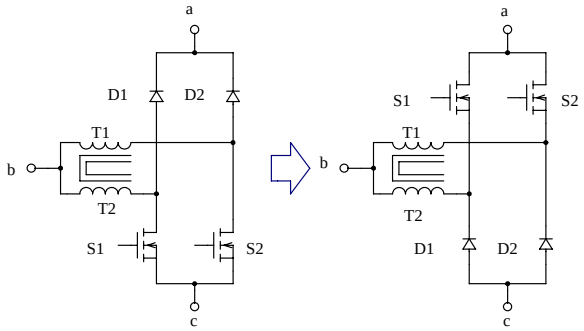
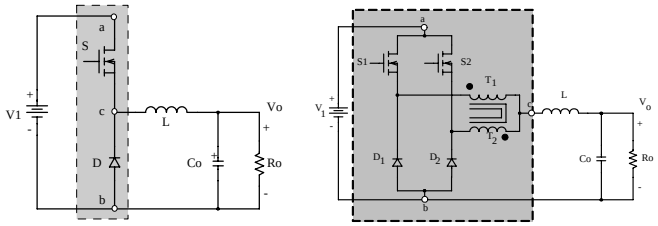


Fig. 1. Three-state switching cell and its bilateral inversion



(a) (b)

Fig. 2. (a) Classical Buck with two-state switching cell. (b) Buck topology with the Three-State Switching Cell.

Fig. 3 shows the proposed buck converter. The circuit is composed by a DC input voltage source (V1), the three-state switching cell, one output filter (Co), and the load (Ro). Being compared the Fig. 2(b) with Fig. 3, it can be noticed that the operation of the pairs of switches S1–D2 and S2–D1 are complementary. Therefore, in the three-state switching cell the bilateral inversion can be done without to change the behavior of the topological circuit and its operation mode.

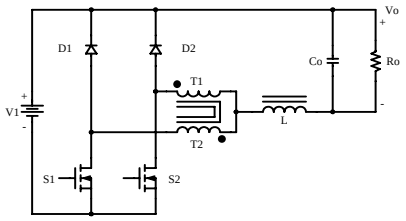


Fig. 3. Proposed buck converter.

This topology presents two operation modes. The first mode is for duty-cycle lower than 0.5 (0 <D <0.5), i.e., when the gating signals of the switches are not overlapping. The second mode is for duty cycle greater than 0.5 (0.5 < D < 1), i.e., when the gating signals of the switches are overlapping.

In [6] , the theoretical approach is detailed by qualitative and quantitative analyses, when the three-state switching cell is applied for the buck topology. The analysis covers the full range of the duty cycle (0 < D < 1) and some preliminary experimental results for duty-cycle lower than 0.5 are presented. The complete design and experimental results for full load and full duty cycle range (0 < D < 1) are presented in [7].

In this paper the three-state switching cell applied to the PWM buck converter, operating only at overlapping of the switch commands is investigated. It occurs when the duty-cycle is greater than 0.5.

With respect to the inductor current shape, three conduction modes are defined as: continuous conduction mode (CCM), discontinuous conduction mode (DCM) and critical conduction mode. Such modes are considered to determine the output characteristic of the converter.

A. Static Gain and Output Characteristic

For the proposed converter, the maximum value of the normalized load (γ) for critical conduction mode (boundary between the CCM and DCM), is only γ=0.0625. In this load condition, duty cycles are 0.25 and 0.75 for D lower than 0.5 and D greater than 0.5, respectively, as shown in Fig. 4. In the classical buck converter, the normalized load is twice (γ=0.25) when duty-cycle is 0.5. This is a great advantage of the proposed converter. In other words, it can be said that the calculated inductance of the proposed converter is reduced to one quarter of the inductance of the classical buck topology.

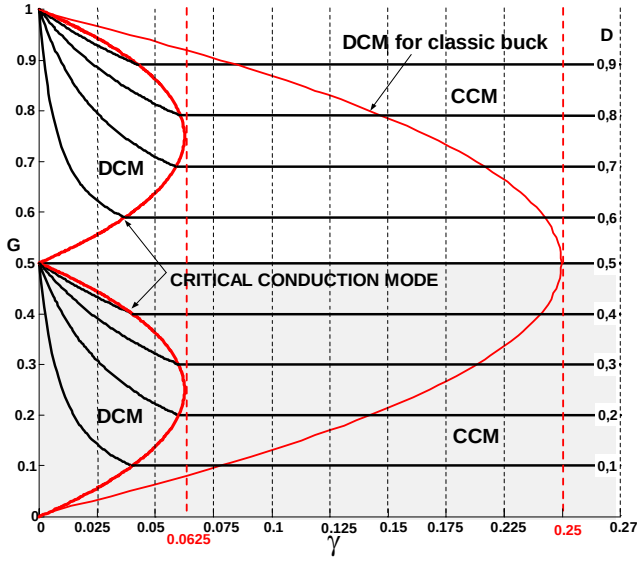


Fig. 4. Output characteristic (voltage gain x normalized load).

III. DESIGN PROCEDURE AND EXPERIMENTAL RESULTS FOR DUTY-CYCLE GREATER THAN 0.5

In this section, the design procedure and experimental results of the proposed buck converter are presented for duty-cycle greater than 0.5 and full load operation. The design is accomplished based on the topology represented in Fig. 3. The main parameters used for D>0.5 are shown below:

A. Specifications

Po = 1kW – output power;

V1 = 200V – input voltage;

V_0 = 150V – output voltage.

For the design the following parameters are adopted:

D = 0.75 – duty cycle;

fs = 30kHz – switching frequency;

ΔIL = 1.33A – ripple current (20% of the current through the inductor);

ΔV_0 = 1.5V – output ripple voltage (1% of V_0).

B. Main Expressions

The main voltage and current waveforms regarding active and passive elements for a given switching period T are shown in Fig. 5. The following expressions describe each operating mode:

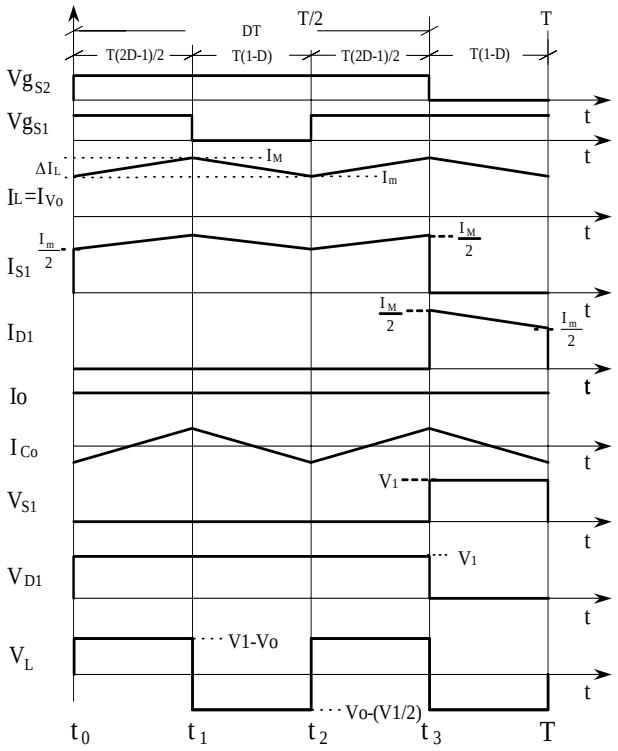


Fig. 5. Main waveforms for D > 0.5.

$$I_M = I_0 + \frac{V_1 \cdot (1-D) \cdot T \cdot (2 \cdot D - 1)}{4 \cdot L} \quad (1)$$

$$I_m = I_0 - \frac{V_1 \cdot (1-D) \cdot T \cdot (2 \cdot D - 1)}{4 \cdot L} \quad (2)$$

Where:

I_M – maximum current through the inductor L

I_m - minimum current through the inductor L

$$i_{L1}(t) = I_m + \frac{V_1 \cdot (1-D) \cdot t}{L} \quad if \quad 0 \le t \le t_1 \quad (3)$$

$$i_{L2}(t) = I_M - \frac{V_1 \cdot (2 \cdot D - 1) \cdot t}{2 \cdot L} \quad if \quad t_1 \le t \le t_2 \quad (4)$$

$$i_{L3}(t) = I_m + \frac{V_1 \cdot (1-D) \cdot t}{L} \quad if \quad t_2 \le t \le t_3 \quad (5)$$

$$i_{L4}(t) = I_M - \frac{V_1 \cdot (2 \cdot D - 1) \cdot t}{2 \cdot L} \quad if \quad t_3 \le t \le T \quad (6)$$

- Inductance L:

$$L = \frac{(2 \cdot D - 1) \cdot (1-D) \cdot V_0 \cdot T}{2 \cdot D \cdot \Delta IL} = 125\ \mu H \quad (7)$$

- Capacitance Co:

$$Co = \frac{\Delta IL}{4 \cdot \pi \cdot fs \cdot \Delta VCo} = 3.684uF \quad (8)$$

1) Inductor Design

From these parameters, inductor *L* was designed and the main characteristics are: ferrite core NEE-42/21/20 - IP12 (thornton), 15 turns, 7 × 23 AWG.

2) Transformer Design

$$V_{T1} = \frac{V_1}{2} = 100V \quad (9)$$

$$I_{rmsT1} = \sqrt{\frac{2}{T} \cdot \int_0^{\frac{T \cdot (2 \cdot D - 1)}{2}} \left(\frac{i_{L1}(t)}{2} \right)^2 dt + \frac{2}{T} \cdot \int_0^{\frac{(1-D) \cdot T}{2}} \left(\frac{i_{L2}(t)}{2} \right)^2 dt} \quad (10)$$

$$I_{rmsT1} = 3,37\ A$$

$$I_{pT1} = \frac{I_M}{2} = 4,47\ A \quad (11)$$

Where:

V_{T1} – voltage across the transformer windings;

I_{rmsT1} – rms current through the transformer windings;

I_{pT1} – peak current through the transformer windings.

From these parameters, the transformer was designed and the main characteristics are: transformer ratio 1:1, ferrite core NEE-42/21/20 - IP12 (thornton), 12 turns, 2 × 20 AWG.

3) Active switches S1 and S2

$$V_s = V_1 = 200V \quad (12)$$

$$I_{rmsS1} = \sqrt{\frac{2}{T}\cdot\int_0^{\frac{T\cdot(2\cdot D-1)}{2}}\left(\frac{i_{L1}(t)}{2}\right)^2 dt + \frac{1}{T}\cdot\int_0^{(1-D)\cdot T}\left(\frac{i_{L2}(t)}{2}\right)^2 dt} \quad (13)$$

$$I_{rmsS1} = 2{,}92\ A$$

Where:

V_S – voltage across the switch

I_{rmsS1} – rms current through the switch.

Since, the MOSFET IRF740 is used.

4) Diodes D1 and D2

$$V_D = V_1 = 200\text{V} \quad (14)$$

$$I_{mD1} = \frac{1}{T}\cdot\int_0^{(1-D)\cdot T}\left(\frac{i_{L4}(t)}{2}\right)dt = 0.83\ A \quad (15)$$

$$I_{pD1} = \frac{I_o}{2} + \frac{V_1\cdot(1-D)\cdot T\cdot(2\cdot D-1)}{8\cdot L} = 4.16\ A \quad (16)$$

Where:

V_{D1} – voltage across the diode;

I_{mD1} – average current through the diode;

I_{pD1} – peak current through the diode.

Since, the ultra-fast diode RHRP840 is used.

C. Simulation and Experimental Results

The laboratory prototype is shown in Fig. 6, which was designed for duty-cycle lower than 0.5 [7] .

The stresses across the devices in the buck topology with the three-state switching cell at duty-cycle greater than 0.5 are less than those across the same converter, operating with duty cycle lower than 0.5. Therefore, the prototype shown in Fig. 6 was employed in the experimental tests.

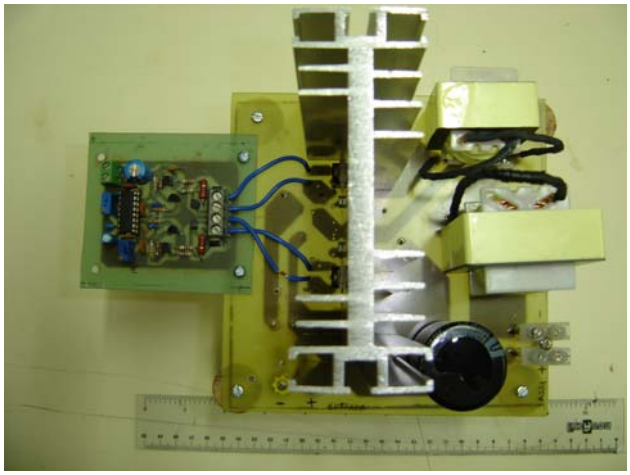


Fig. 6 - Photograph of the prototype.

Fig. 7 and Fig. 8 show the main simulation results. Fig. 9 and Fig. 10 present the experimental results. In Fig. 11, it can be seen that the input current is pulsed, with reduced ripple, while the converter operates at overlapping mode.

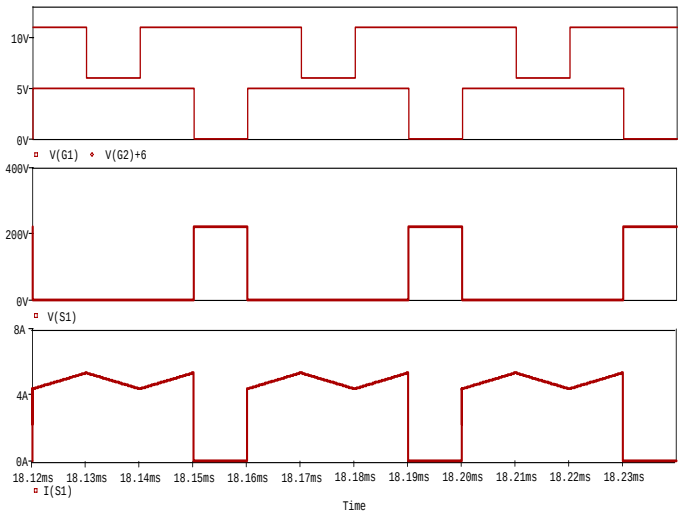


Fig. 7. Gate-to-source voltages through the switches S1 and S2 and voltage and current through S1.

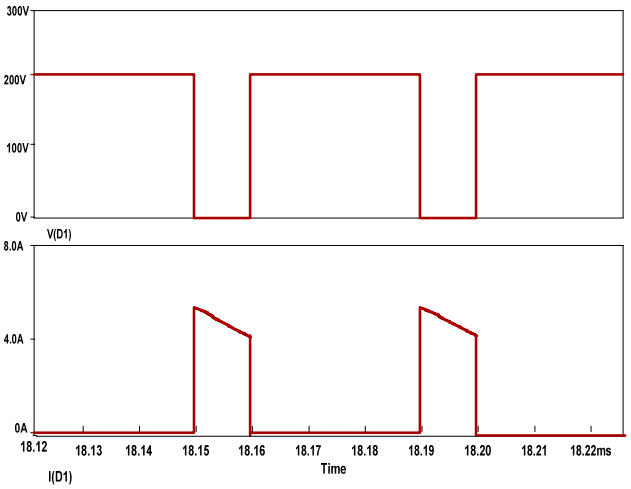


Fig. 8. Voltage and current through D1.

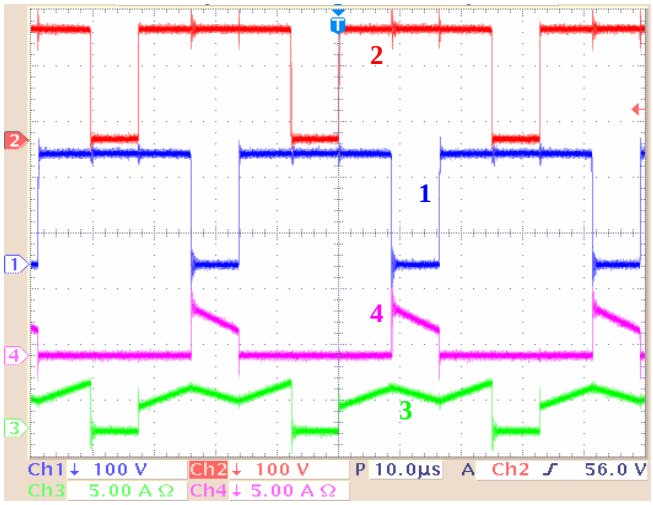


Fig. 9. Curves 1 and 2 show the voltages across D1 and D2, respectively; Curves 4 and 3 show the current through D1 and S2, respectively.

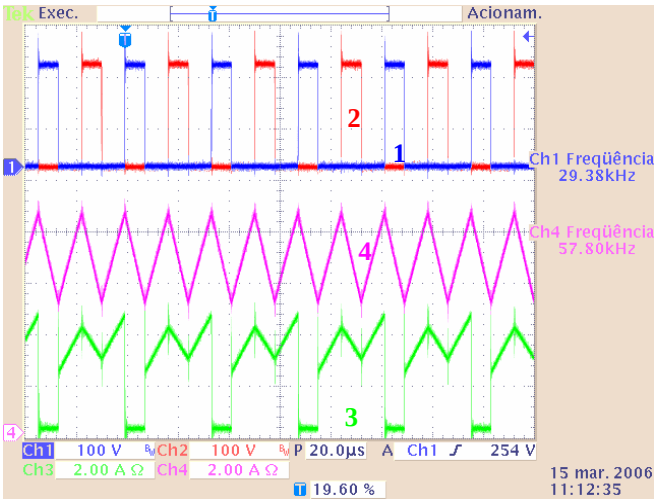


Fig. 10. Curves 1 and 2 show the voltages across S2 and S1, respectively. Curves 3 and 4 show the currents though S1 and L, respectively.

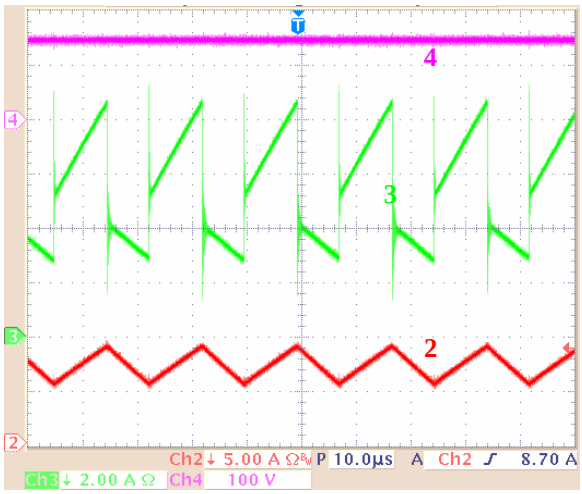


Fig. 11. Curve 4 shows the output voltages Vo. Curves 2 and 3 show the currents through L and the input current Ii, respectively

Fig. 12 presents the output characteristic as a function of the load current.

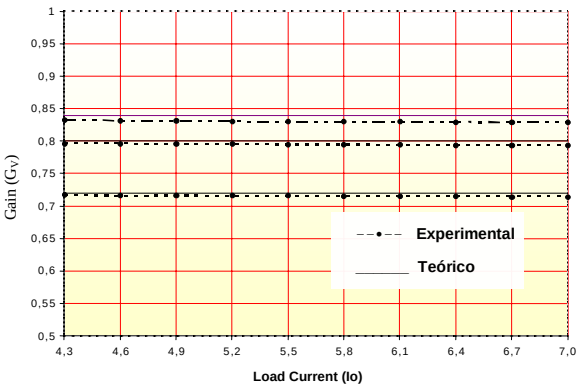


Fig. 12-: Static gain as a function of the load current.

Fig. 13 shows the converter efficiency as a function of the output power. High efficiency is obtained experimentally due to the minimized conduction losses, mainly those regarding the switches, which are turned on simultaneously when energy is transferred from the source to the load. Only 50% of this energy flows through the active switches (S1 and S2), which is due to the transformer, i.e. only 25% of the current flows through each switch. The remaining 50% of the energy flows through the diodes. The total conduction losses are divided among diodes and switches, which is a significant advantage over the classical buck topology.

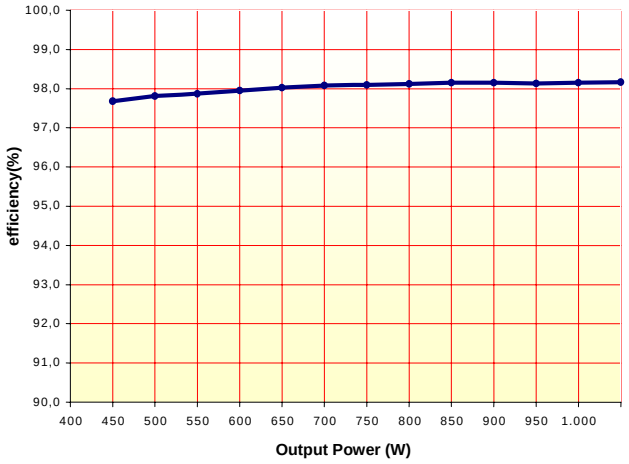


Fig. 13. Efficiency of the converter as a function of the output power.

We can verify experimentally that the minimum asymmetry of the pulses applied to the switches causes a great imbalance between the converter legs. Consequently, these differences affect the normal operation of the converter, as shown in Fig. 14.

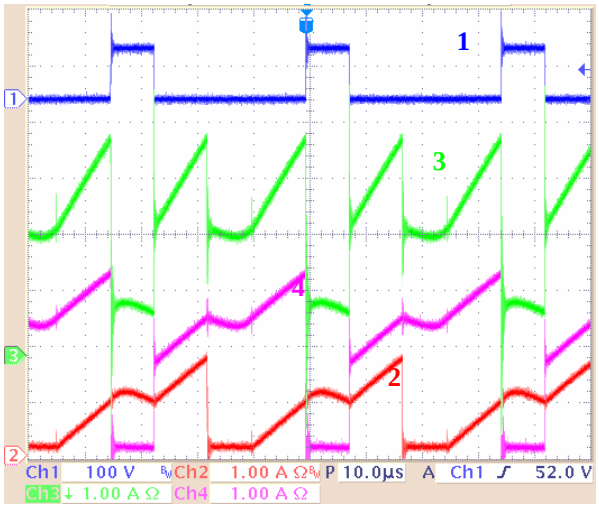


Fig. 14. Curve 1 is the voltage across S2. Curves 4 and 2 are the currents through S1 and S2, respectively. Curve 3 is the input current.

Therefore, the gating signals must be displaced by 180º, for duty cycle varying symmetrically from 0 up to 100%. The paper presented in [8] emphasizes that the peak current mode control can be used to mitigate this problem. This solution is also applied to the push-pull converter. The

same problem may occur if the transformer ratio is not unitary.

Fig. 15 shows the same waveforms as those represented in Fig. 14, although there is no imbalance.

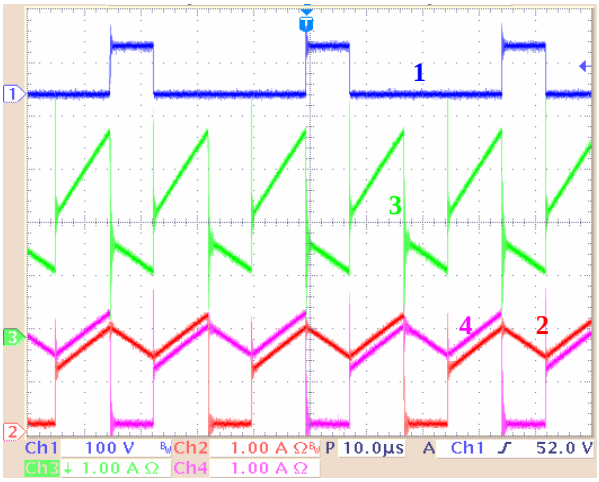


Fig. 15. Curve 1 is the voltage across S2. Curves 4 and 2 are the currents through S1 and S2, respectively. Curve 3 is the input current.

IV. CONCLUSION

The three-state switching cell applied to the buck converter operating at overlapping mode was presented in this paper. The study has shown the converter is suitable for commercial and industrial applications, when low voltage and high current DC-to-DC conversion are required. Since the switches can operate at lower switching frequencies, the topology can reach higher power levels than those obtained with the conventional buck converter. Also, this topology can be applied as a synchronous buck converter and it can increase the efficiency still more.

The input current is semi-pulsed and it presents a DC level this characteristic implicating a small input filter compared the buck converter. In addition, the volume of reactive elements (inductors and capacitors) is reduced because the ripple frequency is higher i.e. twice the switching frequency.

This converter processes only part of the load energy through the active switches. Furthermore this part is divided among the active switches when the converter is operating at Overlapping Mode. Another part of the energy from the input source is delivered to the load through passive components such as the diodes and the transformer winding. Due to the characteristics of the topology, the overall losses are distributed among all semiconductors, facilitating the heat sinking design.

Because all these features, this converter may have a high efficiency compared with the classical buck.

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