THREE-STATE SWITCHING CELL APPLIED TO THE SINGLE-STAGE BOOST PFC: DESIGN CRITERIA AND EXPERIMENTATION

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***Abstract* – This paper presents a bridgeless single phase pre-regulator based on three-state switching cell. In this topology, the energy storage inductor operates with the double of the switching frequency, allowing inductor weight and volume reduction. Also, the three-state switching cell permits parallel operation of the controlled switches eliminating the dynamic current sharing problems in conventional parallel connection. The controlled switches work with hard commutation that depreciates the global efficiency of the circuit. Its performance is demonstrated by means of theoretical analysis and experimental results obtained from 1kW output power prototype.**

***Keywords* – Bridgeless boost converter, power factor correction, single phase pre-regulator, three-state switching cell.**

I. INTRODUCTION

With the advent of telecommunications, it is increasing the search for more efficient power supplies with some characteristics in common: high power factor, low line current distortion, galvanic isolation between the utility and the load and regulated DC output voltage.

In low power applications, single-phase power supplies are commonly used and have been already extensively explored in researches. Nevertheless, it is very usual to find a diode rectifier followed by a capacitive filter in many topologies. Such arrangement generates high harmonic distortion in the line current, resulting in a low power factor (around 0.6).

To satisfy international standards like IEC-61.000-3-2, AC-DC conversion stages are required to operate with a power factor very next to unity. The technique normally used to correct the power factor consists of an input full-bridge diode rectifier, followed by a boost converter, as shown in the Fig. l(a). The conduction losses are very significant because the current always flows simultaneously through three power semiconductors, i.e., two rectifier diodes and another semiconductor which can either be a diode or one active switch, depending on the operation stage.

The circuit shown in Fig. 1(b), named as bridgeless in the literature, operates with lower conduction losses [1-5] because the current flows simultaneously only through two semiconductors, instead of three. It is also noticed that this circuit replaces the pair D1, D3 and D2, D4 for two simple switching cells (named two-state switching cell), composed by a passive switch (diode) and an active switch (MOSFET). In this circuit, it can be observed that between the terminals a and b there is a voltage source (capacitive link - Co) while between the terminal c there is a current source (inductive link - L1).

Fig. 1(c) shows the proposed single stage AC-to-DC converter using the three-state switching cell, defined as "cell B" in [1, 2, 6-11]. When this proposed converter is compared with Fig. 1(b), the following advantages are listed:

- The double switching frequency is applied in the reactive components, resulting lower weight and volume.
- The current through each semiconductor is the half of the projected rating.
- The losses are distributed among the semiconductors, leading to a better heat distribution and consequently more efficient use of the heat sink.
- Part of the input power is directly transferred to the load (output) through the diodes; mainly when duty cycle is lower than 0.5. As a consequence, conduction and switching losses in the active switches are reduced.

The three-state switching cell allows parallel connection of switches and therefore inexpensive devices can be used. Furthermore, this topology is suitable when high power is needed to be processed.

II. OPERATION OF THE PROPOSED CIRCUIT

The propose boost converter operates in continuous conduction mode (CCM) and it is controlled using average current mode control technique to achieve PFC. It has two operation modes regarding the value of the duty cycle (D). In the first mode, when the duty cycle is lower than 50%, there are four operation stages in a switching period of the main switches. The second mode, happening when the duty cycle is higher than 50%, has four operation stages in a switching period. When the converter operates in the first semi-cycle of the line voltage, one cell operates with gated switches, according to the PWM logic, while the other cell conducts through the body diodes of the switches. During the next semi-cycle occurs an inversion of the conduction for the cells.

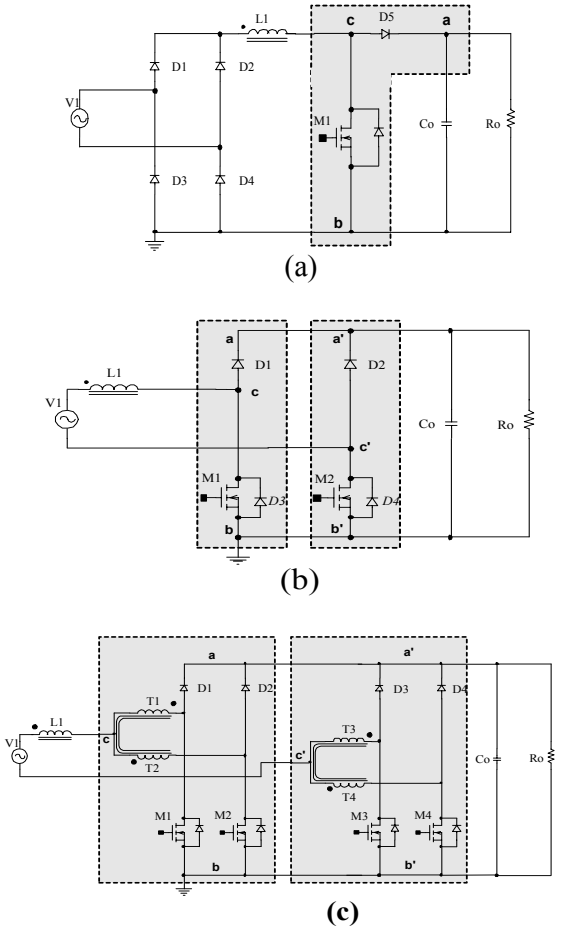


Fig. 1 – (a) Conventional two-stage boost PFC; (b) Single-stage converter named bridgeless, using two simple switching cells (two-state cell). (c) – Proposed bridgeless converter using two three-state switching cells.

The operation stages are defined by the comparison between the rectified voltage (V1) and the output voltage (Vo) as a function of the duty cycle (D). Thus, when the voltage V1 is lower than half of the voltage Vo, the converter operates with duty cycle higher than 0.5 (overlapping mode) and when the voltage V1 is greater than half of the voltage Vo, the converter operates with duty cycle lower than 0.5 (non-overlapping mode). These two operation modes are presented in Fig. 2(a). In Fig. 2(b), the graph of (β) as a function of the duty cycle (D) it shows the total current ripple. There are two points of maximum current ripple in the duty cycle range of $0 < D < 1$, namely when $D = 0.25$ and $D = 0.75$. When the duty cycle equals to 0.5, the ripple current is zero. At this point, the classic boost converter has maximum current ripple.

The ideal output characteristic of the converter is depicted in Fig. 3(a), where the voltage gain is shown as a function of the load, with the duty cycle as a parameter. DCM refers to the discontinuous conduction mode whereas CCM refers to continuous conduction mode. Fig. 3 (b) shows the static characteristic of the classic boost converter. The two load axes (γ) do not have the same scales. Nevertheless, it is possible to notice in Fig 3 (a) that the DCM region is smaller for boost converter using two three-state switching cell. The highest load limit (γ) for DCM, in the classic boost, is find in 0.25, while in the boost converter using three-state switching cells, the load limit (γ) happens in 0.0625.

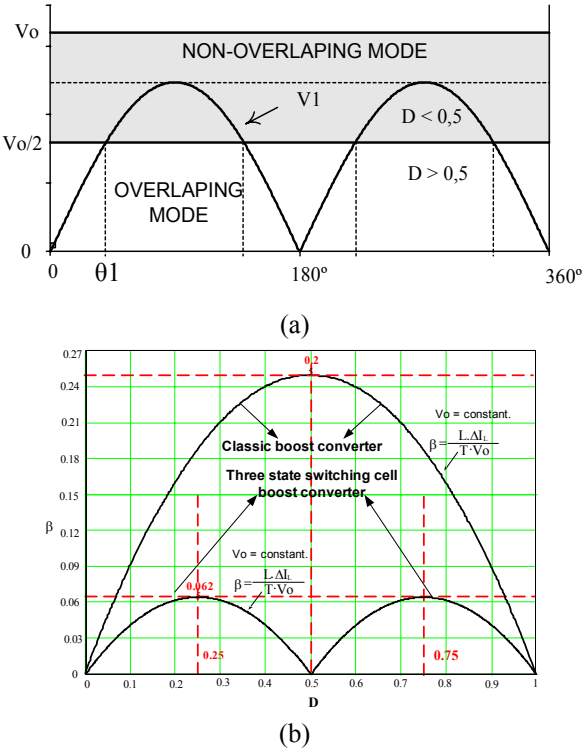


Fig. 2 – (a) Operation methods for one cycle of the line voltage. (b) Total current ripple for classic and proposed boost converters.

A. – Operation Stages for D > 0.5

1) First Stage ($t0 < t < t1$)

Initially, during the positive semi-cycle, the switch M1 is turned on and M2 keeps conducting. The diodes D1 and D2 are reverse biased. For the current through inductor L1 ($I1=I_{L1}$), one part flows through T1 and M1 ($I_{T1} = I_{M1}$) and another part flows through T2 and M2 ($I_{T2} = I_{M2}$). Since T1 and T2 have the same turns-ratio, the current through them are equal ($I_{T1} = I_{T2}$). The opposite polarity between the windings shown in Fig. 4(a) generates a null voltage across the windings (short-circuit). After that, the current returns to the source through body diodes of M3 and M4, which one through M3 and T3 ($I_{M3} = I_{T3}$) and another through M4 and T4 ($I_{M4} = I_{T4}$). Similarly with T1 and T2, the voltage across T3 and T4 is also zero. Moreover, the inductor L1 stores energy and its current grows linearly, without transferring energy to the load.

This stage is illustrated in Fig. 4(a), and the current circulation in the circuit is emphasized. This stage finishes when M2 is turned off.

2) Second Stage ($t1 < t < t2$)

The switch M2 is turned off and M1 keeps conducting. The voltage across the inductor is inverted. The diode D2 is forward biased while D1 is inversely biased. The current $I1 = I_{L1}$, which circulates through inductor L1 is divided in two parts: one flows from T1 and M1 ($I_{T1} = I_{M1}$) and the other from T2 and D2 ($I_{T2} = I_{D2}$), both toward the load. Moreover, this current decreases linearly, transferring the energy stored

in the previous stage and the energy of the source V1 to the load. Since T1 and T2 have the same turns-ratio, the current through them is equal ($I_{T1} = I_{T2}$). Likewise the first stage, the current returns to the source. This stage is shown in Fig. 4(b) and the current circulation is emphasized. This stage finishes when M2 is turned on.

3) Third Stage (t2 < t < t3)

This stage is similar to the first one with the difference that the switch M2 begins to conduct while M1 continues to conduct. The diodes D1 and D2 are reverse biased without transferring energy to the load. Fig. 4(c) illustrates this stage and the current circulation in the circuit is emphasized.

4) Fourth Stage (t3 < t < t4)

This stage is similar to the second one with the difference that the switch M1 is turned off and M2 keeps conducting. The diode D1 is forward biased and D2 is reverse biased. This way, energy is transferred from source V1 and from inductor (which was stored in the previous stage to the load). The current through the circuit is shown in Fig. 4(d).

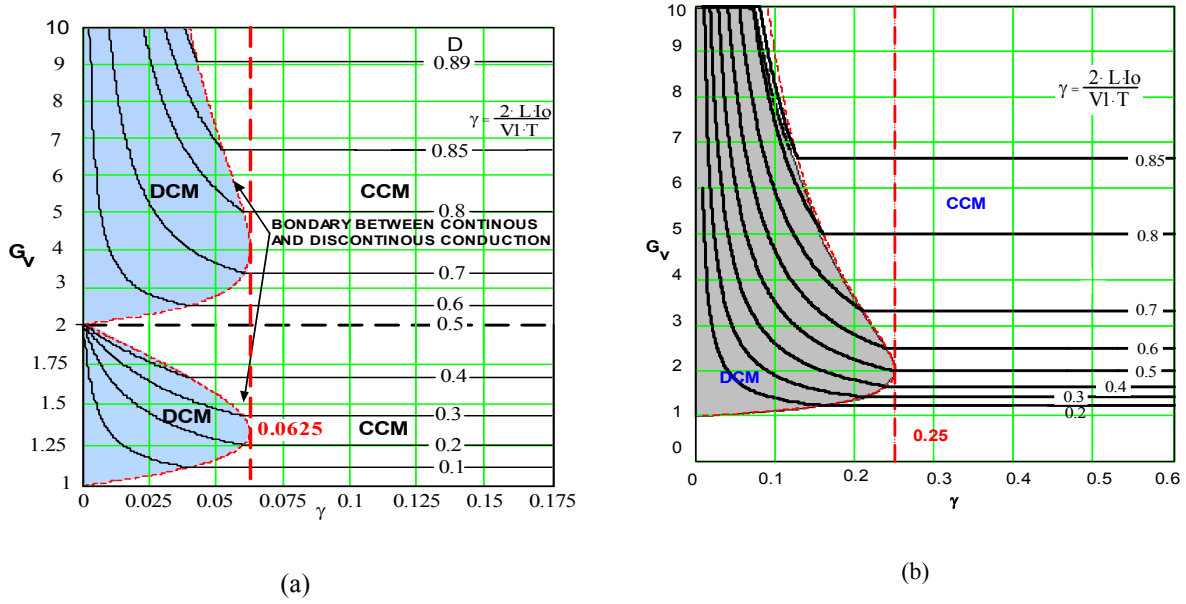


Fig. 3 – (a) Output characteristic for the three states boost converter. (b) Output characteristic for the classic boost converter.

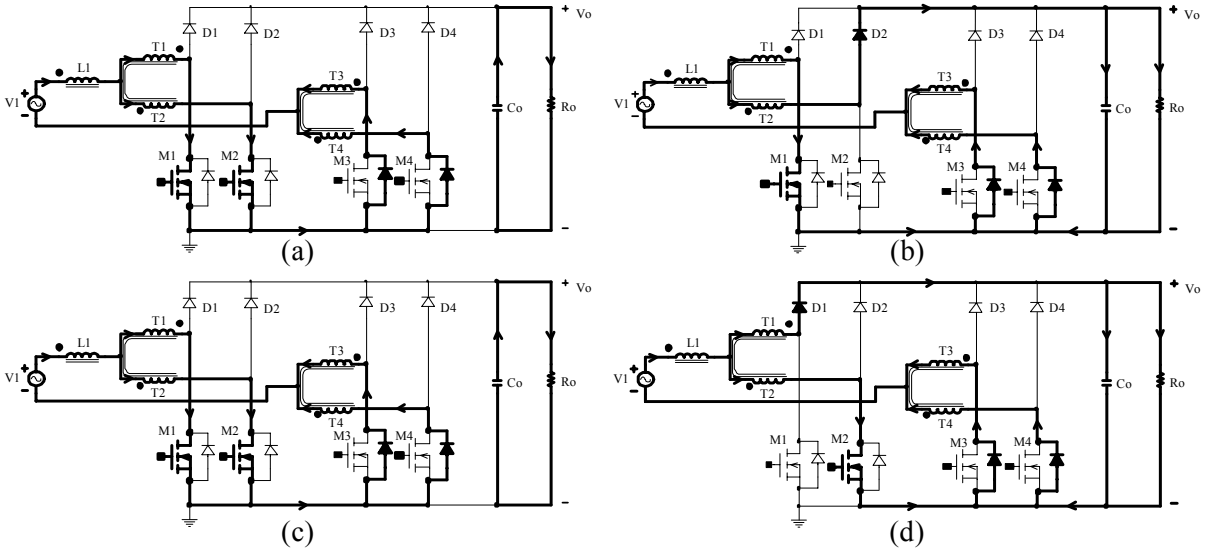


Fig. 4 – Operation stages for, D>0.5 and positive semi-cycle.

B. – Operation Stages for D < 0.5

1) First Stage (t0 < t < t1)

In the instant t = t0 (positive semi-cycle), switch M1 begins conducting and M2 is turned-off. The diode D1 is reverse biased and D2 begins conducting. The current through inductor L1 ($I1=I_{L1}$) is divided in two parts: one flows through T2 and D2 (IT2 = ID2) to the load and the through T1 and M1 (IT2 = IM1). Since T1 and T2 have the same turns-ratio, the current through the windings are equal ($IT1 = I_{T2}$). The current through the inductor L1 grows linearly and stores energy. The windings T1 and T2 have the same impedance; therefore, the voltages across

them are equal and the magnitudes are half of the output voltage Vo. The return of the current to the source happens through body diodes of M3 and M4. One part flows through M3 and T3 (IM3 = IT3) and another part flows through M4 and T4 ($I_{M4} = I_{T4}$). The voltage across the windings T3 and T4 is zero. This operation stage is illustrated in Fig. 5(a) and the current circulation in the circuit is emphasized. This stage finishes when M1 is tuned off.

2) Second Stage (t1 < t < t2)

In the instant t = t_1, the switch M1 is turned off and M2 stays turned off. The voltage across the inductor is inverted. The diode D1 is forward biased and D2 keeps conducting. The energy stored in L1, during the previous stage, is transferred to the load. The current circulation through T1 and T2 ($I_{T1} = I_{T2}$), in agreement with the polarity, generates a null magnetic flow through core. The current returns to the source like in the previous stage. This stage is illustrated in Fig. 5(b) and the current circulation is emphasized. This stage finishes when M2 is turned on.

3) Third Stage (t2 < t < t 3)

Due to symmetry of the circuit, this stage is similar to the first one with the difference that M2 is turned on while M1 keep turned off. The diode D1 keeps conducting and D2 is reverse biased. The return of the current to the source is also the same. The current loop through the circuit is shown in Fig. 5(c).

4) Fourth Stage (t3 < t < t4)

This stage is similar to the second one and the circuit is shown in Fig. 5(d). The current circulation is emphasized.

During the negative semi-cycle occurs the symmetry of all described stages for D>0.5 and D<0.5. M1 and M2 begin to conduct by their body diodes while M3 and M4 operate as active switches with PWM modulation.

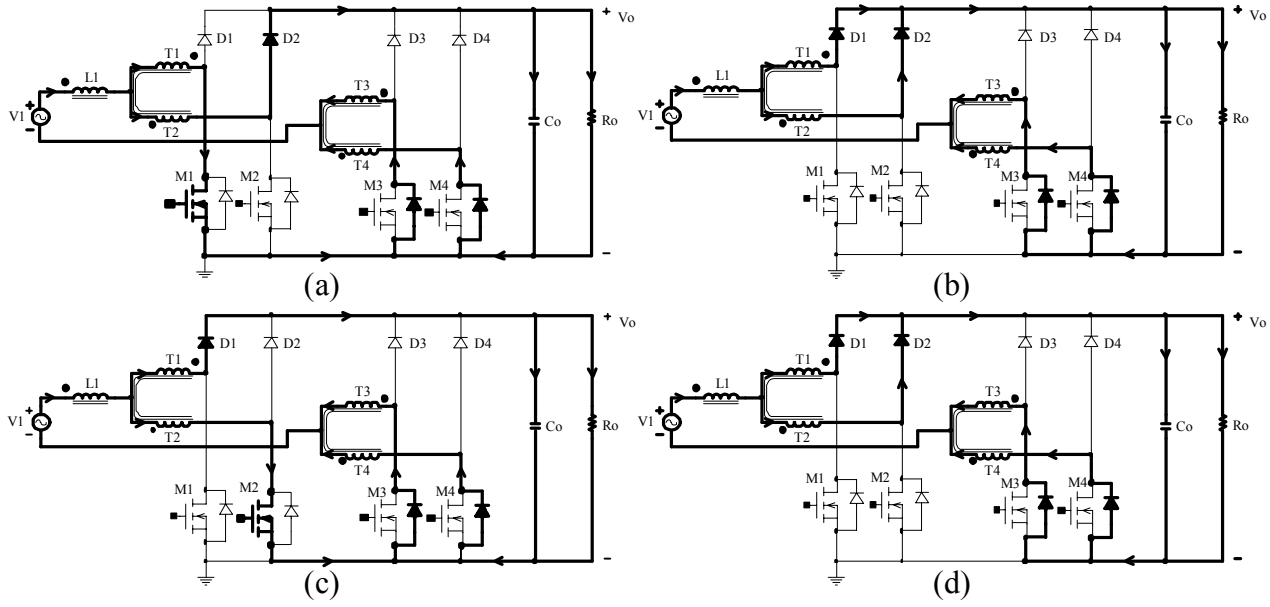


Fig. 5 - Operation stages for D < 0.5 and positive semi-cycle.

III. DESIGN PROCEDURE AND EXPERIMENTAL RESULTS

The design procedure of the pre-regulator with three-state switching cells is presented in this section. The control of the converter is based on an average current mode control. The modulation of the proposed converter is implemented as shown in Fig. 6.

A. Specifications

Input data:

Po = 1kW	output power;
V1 = 220V	rms input voltage;
Vo = 400V	DC output voltage.

For the design the following parameters are adopted:

Fs = 30kHz	switching frequency;
ΔIL = 1.325A	current ripple (20% of I1p);
ΔVo = 10V	output voltage ripple;
η = 97%	efficiency;

$$\alpha = \frac{Vo}{Vp} = 1.286$$ voltages ratio;

$$\theta l = \sin^{-1}\left(\frac{\alpha}{2}\right) = 0.6982\text{rad}$$ transition angle between the two operation modes.

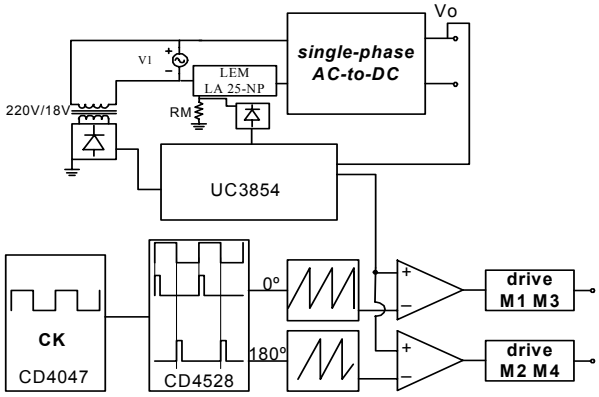


Fig. 6 – Full schematic diagram.

B. Inductor and output capacitor

Inductor L:

$$L_{boost} = \frac{V_0}{16 \cdot \Delta I_L \cdot F_s} = 6.29 \times 10^{-4} H \qquad L_{boost} = 630 \mu H$$

Capacitor C:

$$Co \geq \frac{Po}{4 \cdot \pi \cdot fr \cdot Vo \cdot \Delta Vo} = 1.658 \times 10^{-4} F \qquad Co = 780 \mu F$$

C. Voltage and current

1) Inductor (rms and peak currents)

$$I_{rmsL} = \frac{\sqrt{2} \cdot \alpha \cdot I_0}{\eta} = 4.686A \qquad I_{pL} = \frac{2 \cdot \alpha \cdot I_0}{\eta} = 6.627A$$

2) Transformer (DC voltage and rms and peak currents)

$$V_{T1} = \frac{Vo}{2} = 200V \qquad I_{rmsT1} = \frac{\sqrt{2} \cdot \alpha \cdot Io}{2 \cdot \eta} = 2.343A$$

$$I_{pT1} = \frac{\alpha \cdot Io}{\eta} = 3.314A$$

3) Switches (DC voltage, peak, average and rms currents)

$$V_{MI} = V_o = 400\,V \qquad I_{pM1} = \frac{\alpha \cdot Io}{\eta} = 3.314A$$

$$I_{avgM1} = \frac{\alpha \cdot Io}{\eta} \cdot \frac{sen(\alpha)}{(\pi \cdot \alpha)} = 0.787A$$

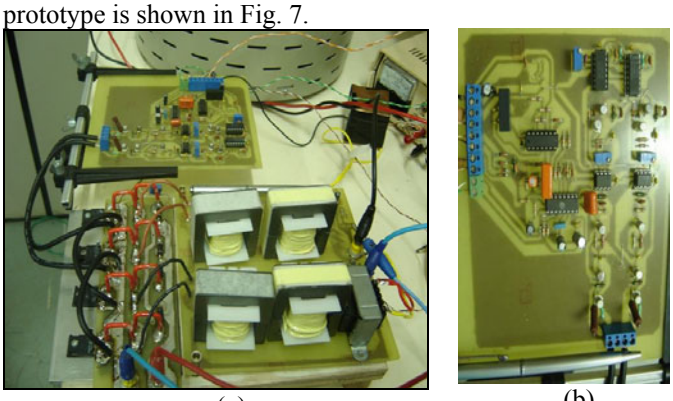
$$I_{rmsM1} = \frac{\alpha \cdot Io}{2 \cdot \eta} \cdot \sqrt{\frac{(2 \cdot \alpha - sen(\alpha))}{\alpha}} = 1.855A$$

4) Diodes (DC voltage, average and peak currents)

$$V_{DI} = Vo = 400\,V \qquad I_{avgD1} = \frac{\alpha \cdot Io}{4 \cdot \eta} = 0.828A$$

$$I_{pD1} = \frac{\alpha \cdot Io}{\eta} = 3.314A$$

With these calculated values, the main components of the converter are specified. The input current shape is obtained by applying average current mode control using the dedicated UC3854 integrated circuit [12]. The complete prototype is shown in Fig. 7.



(a) (b)

Fig. 7 – (a) Photo of the power and command circuits. (b) Detail of the command/control circuit.

In Fig. 8 are shown the input voltage and input current. The input current presents the fundamental component in phase with line voltage. As consequence, the power factor is high. Also, the same figure shows the transition points for duty cycle equal to D=0.5 where current ripple is almost zero.

Fig. 9 shows the harmonic analysis of the input current (line current), where the Total Harmonic Distortion of the input current is equal to THD=3.835%.

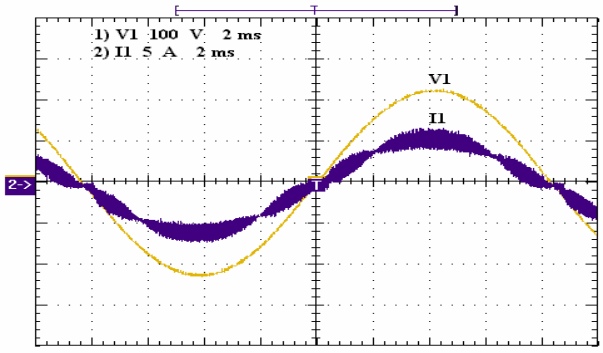


Fig. 8 – Voltage and current in the line.

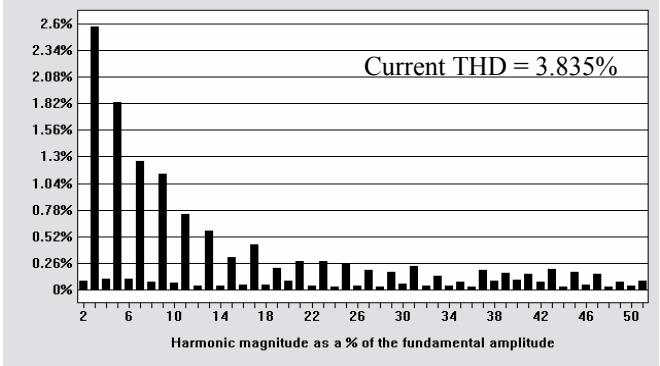
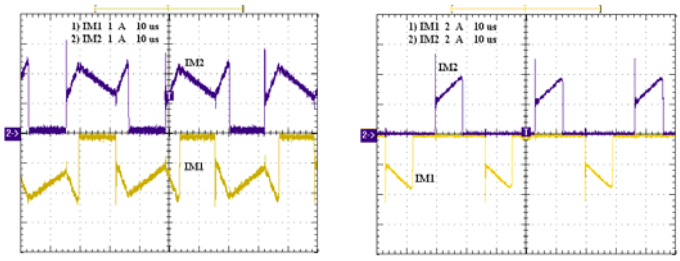


Fig. 9 – Harmonic spectrum of the line current

The pair of the switches M1-M3 is gated simultaneously with the corresponding pulse and the other pair of the switches M2-M4 also is gated simultaneously of similar way. The pulses are obtained after comparison of two 180º displaced tooth-saw external signals and the UC3854 control signal, as shows Fig. 6. The pulse width of each pair must be symmetrical to avoid auto transforms saturation.

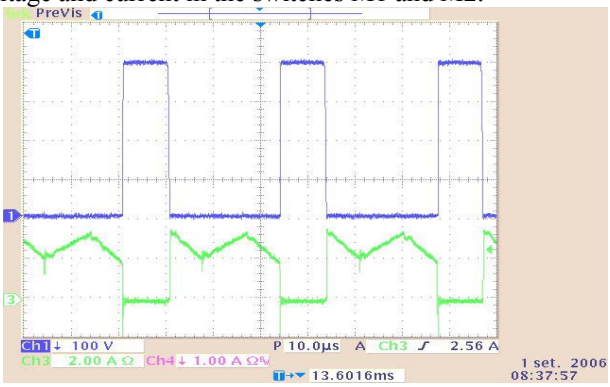
In Fig. 10(a) and Fig. 10(b) are shown current waveforms through switches M1 and M2 for a duty cycle higher than 0.5, and lower than 0.5. It is possible to observe a good symmetry of the currents.



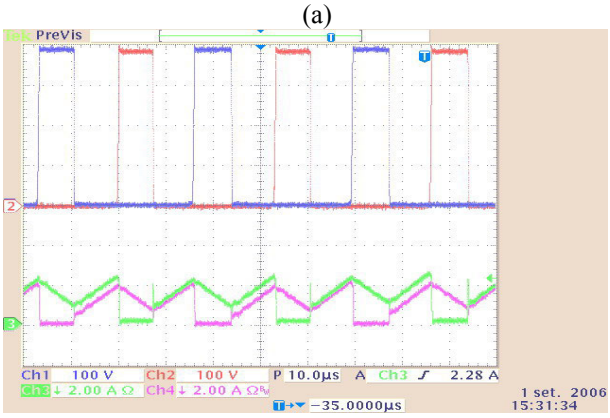
(a) (c)

Fig. 10 – Current through switches M1 and M2 for; (a) duty cycle D>0.5; (b) duty cycle D < 0.5.

In steady state operation condition, Fig. 11(a) shows voltage and current in the diode D1, and Fig. 11(b) shows voltage and current in the switches M1 and M2.



(a)



(b)

Fig. 11 – (a) Voltage and current in D1. (b) Voltage and current in M1 and M2.

Fig. 12 shows the converter efficiency as a function of the output power.

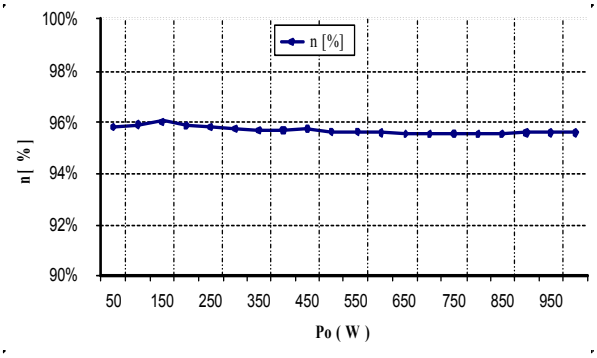


Fig. 12 - Efficiency as a function of the output power.

IV. CONCLUSION

In this work a bridgeless single phase pre-regulator with power factor correction using three-state switching cell was studied. In this converter, the MOSFET conduction losses are minimized because the current is divided between two components. When the duty cycle is lower than 0.5, part of the energy is directly transferred to the load without being processed by the active switches. In addition, the losses are better distributed on the heat sink and inexpensive devices can be used. Appling the average current mode control based on the dedicated UC3854 integrated circuit, high power factor (PF=0.98) and reduced total harmonic distortion (THD=4%) was achieved. In the converter were detected high diodes recovery currents, what increased commutation losses in the controlled switches and consequently degraded the efficiency. Therefore, in a future version the detailed commutation analyses will be realized.

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