FOUR-LEVEL HALF-BRIDGE INVERTER BASED ON THE Y-Δ FOUR-STATE SWITCHING CELL

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***Abstract* – This paper presents a half-bridge four-level inverter, based on a switching cell of four states. The principle of operation of this inverter is described and the main theoretical waveforms are presented, as well as the simulations and experimental results. The main expressions for the design of the inverter are also presented. This inverter presents the following advantages over the half-bridge classic inverter: the frequency at the output filter is triple the switching frequency; the amplitude of the voltage in the output filter (Vab) is third part that of the half-bridge classic converter; the load current is divided among the switches, therefore reducing the conduction losses. In light of its characteristics, we believe that inverter is appropriate for industrial applications.**

***Keywords* — half-bridge inverter, four-level inverter, four-state cell.**

I. INTRODUCTION

The advances in the power electronics have permitted the increasing usage of dc-ac converters, which transform the energy from a dc source into an ac source and, therefore, are referred as inverters. The dc input power source can be, among others, a battery bank, photovoltaic solar panels, fuel cells, as well as the output of a rectifier.

Among their many applications, inverters are used for speed control of ac machines, inductive heating and uninterrupted power supply systems, which are becoming more and more popular in the industry.

In PWM converters, it is common to increase the switching frequency, so that the harmonic components are shifted to higher frequencies, making filtering easier. However, increasing the switching frequency is limited due to the increase in the switching losses.

[1] presents a new Y-Δ commutation cell, which presents four commutation states. The use of this cell in DC-DC converters presents the following advantages: it does not require control circuits to balance the currents; the frequency of the input and output filters is three times the switching frequency; the conduction losses are reduced.

[2] presents the three-level half-bridge inverter based on the three-state switching cell, which presents the following advantages over the classic inverter: the frequency at the load is twice the switching frequency; the amplitude of the output voltage is half that of the classic converter; the load current is divided among the switches, therefore reducing the conduction losses.

Based in [1] and [2], this paper presents the four-level half-bridge inverter, which presents the following advantages: the frequency at the output filter is triple the switching frequency; the amplitude of the voltage in the output filter (Vab) is third part that of the half-bridge classic converter; the load current is divided among the switches, therefore reducing the conduction losses.

II. Y-Δ SWITCHING CELL

In [1], the Y-Δ four-state switching cell was proposed for application in DC-DC converters, this cell presents unidirectional current flow thus, in order to apply it to inverters, it is necessary to make it bidirectional, as shown in Fig. 1.

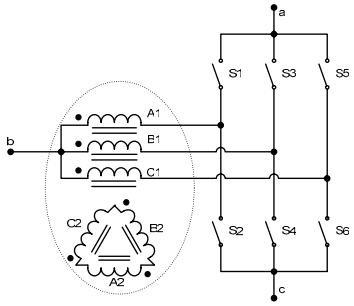

Fig. 1 - Bidirectional current Y-Δ four-state switching cell.

A. Operating states

The switching cell of classic inverters, is defined as a two-state commutation cell because of the complementary operation of the switches; that is, when one switch conducts the other is blocked and vice-versa[2].

The Y-Δ four-state switching cell proposed here has nine possible configurations for the switches, however, from an outside view of the cell, this present only four commutations states [1], as it can be seen in the summary description of the table I, as well as in the Fig. 2.

For the first state all switches of the upper group conduct; for the second state two switches of the upper group and one of the lower group conduct; for the third state one switches of the upper group and two of the lower group conduct; for the fourth state all switches of the lower group conduct and for the neutral state none switch conducts.

In continuous conduction mode (CCM), this cell operates in 1st and 2nd states, in 2nd and 3rd states or 3rd and 4th states, as a function of duty cycle [1]. In the discontinuous conduction mode (DCM), besides the states mentioned for CCM, there is also the neutral state.

TABLE I
Switching states of a Y-Δ four-state switching cell.
X → on - → off

	S1	S2	S3	S4	S5	S6
1st State	X	-	X	-	X	-
2nd State	X	-	X	-	-	X
2nd State	X	-	-	X	X	-
2nd State	-	X	X	-	X	-
3rd State	X	-	-	X	-	X
3rd State	-	X	X	-	-	X
3rd State	-	X	-	X	X	-
4th State	-	X	-	X	-	X
Neutral State	-	-	-	-	-	-

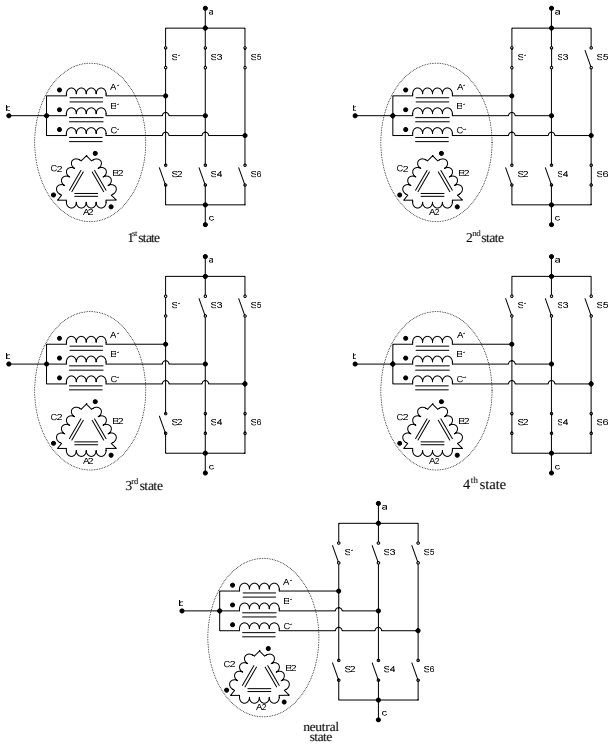

Fig. 2 - Switching states of a four-state switching cell.

B. Drive signals

The switches composing the Y-Δ four-state switching cell should obey the following drive rule: same-leg switches should be driven in a complementary fashion, whereas different-leg switches should have a 120º lag between their drive signals, that is, third part of cycle (1/3).

The duty cycle is determined by expression (1).

$$D = \frac{t_{onS1}}{T} \tag{1}$$

Where:

t_{onS1} – conducting interval of switch S1;

T – switching period of switch S1.

Converters based on this switching cell have three operating regions, given as a function of the duty cycle applied to the switches.[1]

Notice that each region of operation works with only two states of operation, thus, for region A, the 3rd and 4th states are presented, for region B, the 2nd and 3rd states are presented, and for region C, the 1st and 2nd states are presented.

III. HALF-BRIDGE CONVERTER

Fig. 3 presents the half-bridge converter based on the Y-Δ four-state switching cell.

For every operating regions the operation and the main waveforms of the converter will be presented in the following section.

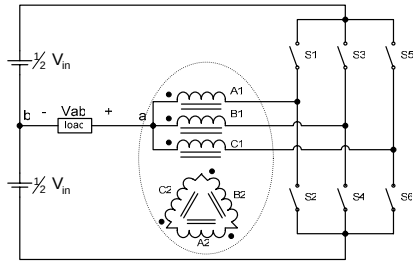

Fig. 3 – Proposed half-bridge converter.

A. Operating region A – 0 < D < 1/3

The operation of the converter in CCM for D<1/3 is described as follow. Fig. 4 and Fig. 5 depict the operating stages of the converter, while Fig. 6 illustrates its main waveforms.

1st Stage ($t_0 < t < t_1$)

At the instant t_0 switch S1 starts conducting, and S2 is switched off. Fig. 4a shows this operating stage, in which the switching cell is in the 3rd state. The simplified circuit of this stage can be observed in Fig. 5a.

Due to the magnetic effect of the transformer, the currents through the transformer windings are identical, thus, the load current is divided through the windings of the transformer[1].

Note that the voltage across winding A1 during this stage is 2/3 of the bus voltage. Therefore, the voltage at point A is given by (2) and the voltage imposed across the load during this stage is given by (4).

$$V_a = \tfrac{1}{3} V_{in} \tag{2}$$

$$V_b = \tfrac{1}{2} V_{in} \tag{3}$$

$$V_{ab} = \tfrac{1}{3} V_{in} - \tfrac{1}{2} V_{in} = -\tfrac{1}{6} V_{in} \tag{4}$$

2nd Stage ($t_1 < t < t_2$)

At the instant t_1 switch S1 is turned off, thus switch S2 starts conducting. Fig. 4b shows this operating stage and the simplified circuit is depicted in Fig. 5b. In this stage, it can be observed that the switching cell is in the 4th state.

The transformer windings are short-circuited through switches S2, S4 and S6, thus the voltage across the windings are zero. In this stage, the voltage at point A is given by (5), and the voltage across the load is given by (7).

$$V_a = 0 \tag{5}$$

$$V_b = \tfrac{1}{2} V_{in} \tag{6}$$

$$V_{ab} = 0 - \tfrac{1}{2} V_{in} = -\tfrac{1}{2} V_{in} \tag{7}$$

3rd Stage ($t_2 < t < t_3$)

At the instant t_2, which is equivalent to 1/3 of the switching period, switch S3 starts conducting, and switch S4 is turned off. Fig. 4c shows this operating stage, in which the switching cell is in the 3rd state.

The behavior of the circuit during this stage is similar to the first one, with a single difference regarding the switches

that are conducting and, as a consequence, the polarity of the voltage across the transformer.

4th Stage ($t_3 < t < t_4$)

At the instant t_3 switch S3 is turned off, thus switch S4 starts conducting. Fig. 4d depicts this stage, which is identical to the second stage, already described.

5th Stage ($t_4<t<t_5$)

At t_4, switch S5 starts conducting and switch S6 is turned off. Fig. 4e shows this operational stage. Like the third stage, the behavior of the circuit during this stage is similar to the first stage.

6th Stage ($t_5<t<t_6$)

At t_5, switch S5 is turned off, causing switch S6 to conduct. Fig. 4f shows this operational stage, which ends at t_6 when switch S1 starts to conduct, beginning a new switching period.

Average load voltage

The average voltage across the load, for a switching period, can be obtained from Fig. 6. Notice that, for this converter, is sufficient to analyze 1/3 of the operating period, keeping in mind that regarding the output voltage, the stages repeat themselves every 1/3 period, thus the average voltage across the load is given by (10).

$$V_{ab} = \frac{3}{T}\cdot\left(\int_{t0}^{t1} -\frac{V_{in}}{6}\cdot dt + \int_{t1}^{t2} -\frac{V_{in}}{2}\cdot dt\right) \quad (8)$$

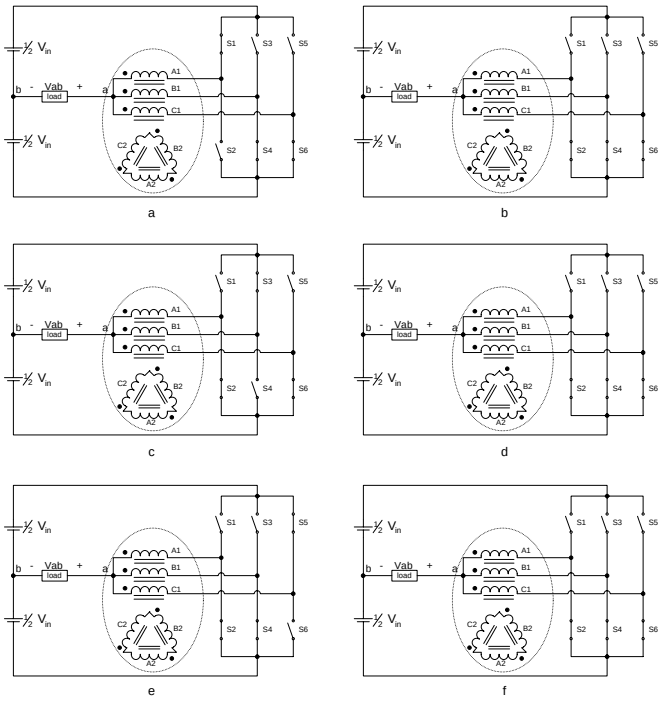

Fig. 4 - Operating stages (0<D<1/3).

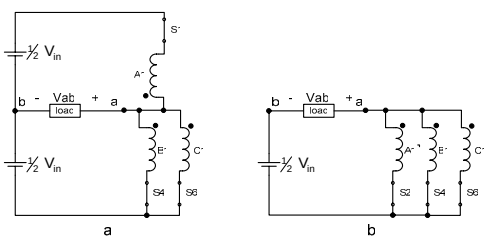

Fig. 5 – Simplified circuits (0<D<1/3).

$$V_{ab} = \frac{3}{T}\left(-\frac{V_{in}}{6}\cdot(D\cdot T - 0) - \frac{V_{in}}{2}\cdot(\tfrac{1}{3}\cdot T - D\cdot T)\right) \quad (9)$$

$$V_{ab} = \frac{V_{in}}{2}\cdot(2D-1) \quad (10)$$

B. Operating region B – 1/3 < D < 2/3

The operation of the converter in CCM for region B is described shortly through the table II, in which the states of the switches for each stage of operation are presented. Fig. 7 depict the simplified circuits of the converter for this operating region, while Fig. 8 illustrates its main waveforms.

TABLE II
Operating stages for region B.
X → on - → off

Stage	S1	S2	S3	S4	S5	S6	State
1st Stage	X	-	-	X	X	-	2nd State
2nd Stage	X	-	-	X	-	X	3rd State
3rd Stage	X	-	X	-	-	X	2nd State
4th Stage	-	X	X	-	-	X	3rd State
5th Stage	-	X	X	-	X	-	2nd State
6th Stage	-	X	-	X	X	-	3rd State

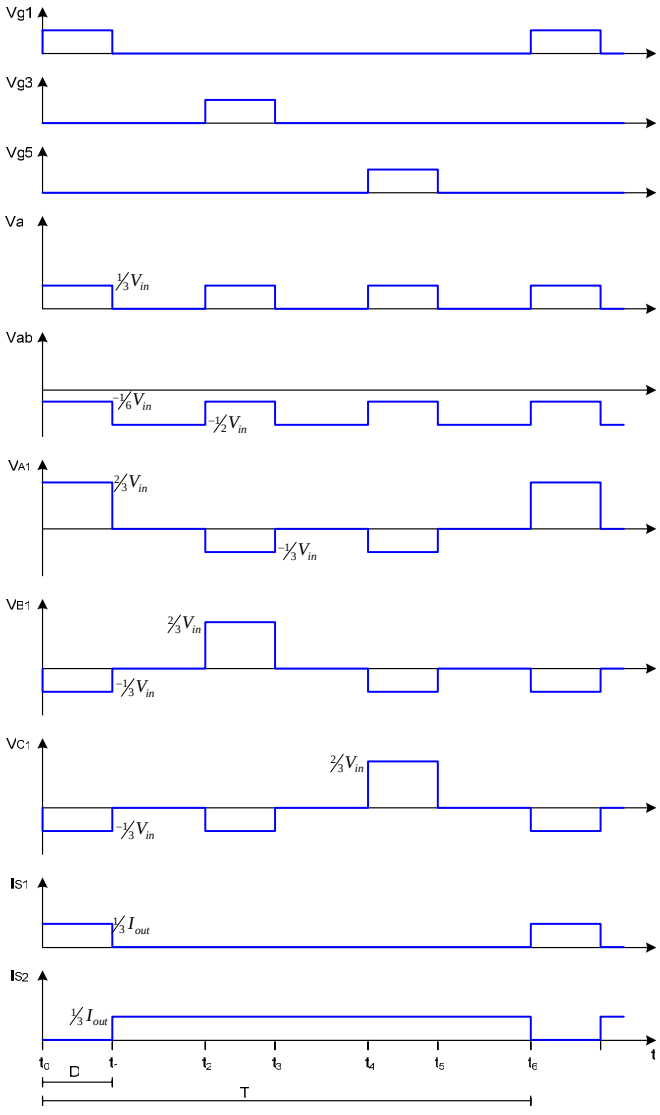

Fig. 6 – Basic waveforms (0<D<1/3).

C. Operating region C – 2/3 < D <1

The operation of the converter in CCM for region C is described shortly through the table III, in which the states of the switches for each stage of operation are presented. Fig. 9 depict the simplified circuits of the converter for this operating region, while Fig. 10 illustrates its main waveforms.

TABLE III
Operating stages for region C.
X → on - → off

Stage	S1	S2	S3	S4	S5	S6	State
1st Stage	X	-	X	-	X	-	1st State
2nd Stage	X	-	-	X	X	-	2nd State
3rd Stage	X	-	X	-	X	-	1st State
4th Stage	X	-	X	-	-	X	2nd State
5th Stage	X	-	X	-	X	-	1st State
6th Stage	-	X	X	-	X	-	2nd State

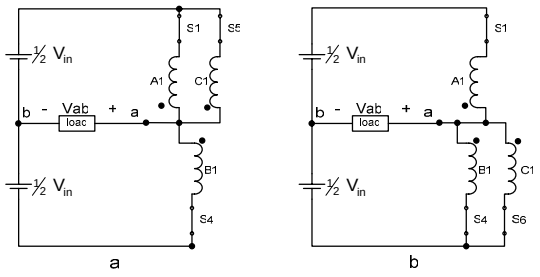

Fig. 7 – Simplified circuits (1/3<D<2/3).

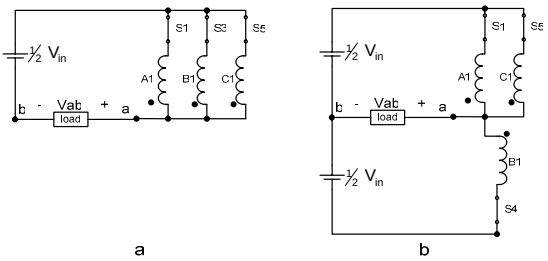

Fig. 9 – Simplified circuits (2/3<D<1).

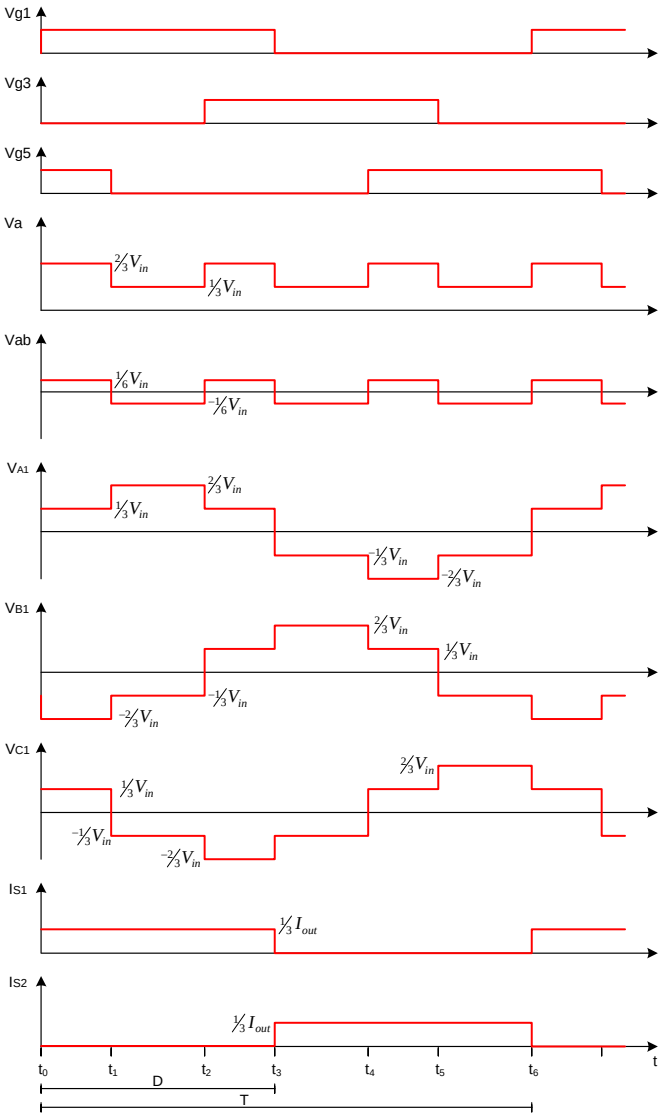

Fig. 8 – Basic waveforms (1/3<D<2/3).

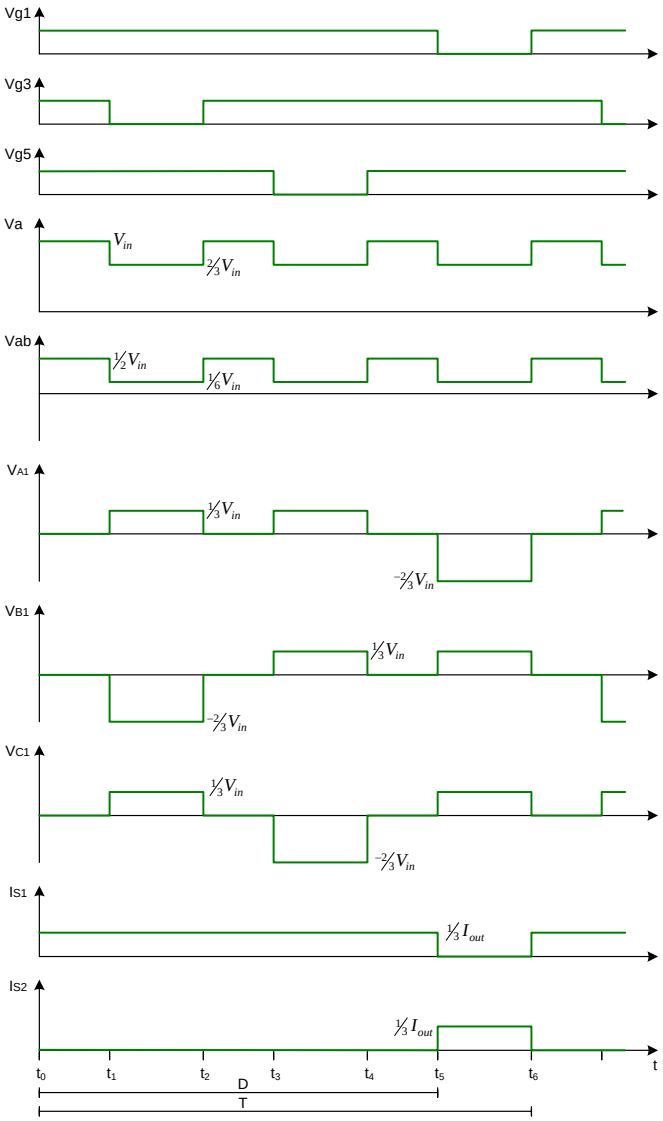

Fig. 10 – Basic waveforms (2/3<D<1).

IV. OPERATION AS AN INVERTER

For operating region A, negative output voltage values can be obtained, which are bounded by limits –Vin/2 and –Vin/6. For operating region B, negative and positive output voltage values are obtained within the limits of –Vin/6 and Vin/6. For operating region C, positive output voltage values are obtained within the limits of Vin/6 and Vin/2.

Although demonstrated only for the region A, it should be observed that (10) determine the average output voltage for every operating regions, there is no discontinuity when it is going from one region to another. Fig. 11 presents the average output voltage for the entire operation range of the converter.

Keeping in mind the limits of the output voltage, -Vin/2 and Vin/2, it can be concluded that by using the proper modulation strategy and filtering, a sinusoidal voltage waveform can be obtained at the output of the converter.

A. Sinusoidal PWM Modulation

The modulation used for the analysis, simulations and implementation of this structure is the classic sinusoidal PWM. In the implemented circuit, this modulation was made through a DSP.

The drive signal of switch S1 is obtained by comparing the sinusoidal voltage reference (Vsin) and the triangular voltage waveform (Vtri). The drive signal of switch S2 is complementary to that of switch S1.

The drive signal of switch S3 has the same duration as the drive signal of switch S1, however, it lags by 1/3 of a switching cycle. While the drive signal of switch S5 lags by 2/3 of a switching cycle.

V. STUDY OF THE TRANSFORMER

The high frequency transformer of this structure does not provide isolation between the input source and output voltage, its duties are to divide the current evenly and providing four voltage levels at the output.

Figures 6, 8 and 10 present the voltages across the transformer windings for operating regions A, B and C, respectively. The voltage across the windings and the time that the transformer is submitted to this voltage are a function of the operational duty cycle.

When operating as an inverter, the worst scenario from the standpoint of the voltage across the windings, occurs when the duty cycle is higher 1/3 and under 2/3.

When regarding the current through the windings, the current through each of the windings is equal to 1/3 of the load current for any duty cycle and for any type of load.

In this manner, with the knowledge of the voltage across and the current through the windings, the transformer can be designed.

VI. SIMULATION RESULTS

The simulation results of the half-bridge inverter using a Y-Δ four-state switching cell and sinusoidal PWM modulation are presented.

Fig. 12 shows the sinusoidal voltage reference (Vsin), the triangular voltage (Vtri) and the Vab voltage, which comply with operation principles described earlier. The software used for simulation is the *PSIM Demo Version 6.0*.

Two characteristics of this converter should be emphasized: the frequency at the load is three times the switching frequency and the output voltage has four levels. These features minimize the output voltage filtering efforts.

Fig. 13 presents the harmonic spectra of voltage Vab for the classic half-bridge inverter and for the proposed four-level half-bridge inverter, both with a switching frequency of 20kHz. It can be observed that the four-level half-bridge converter presents a significant reduction in the harmonic content.

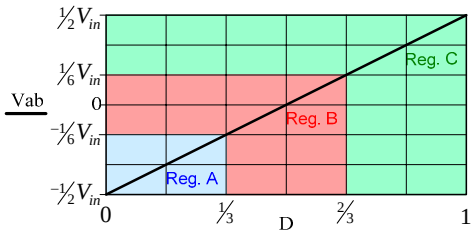

Fig. 11 - Average output voltage.

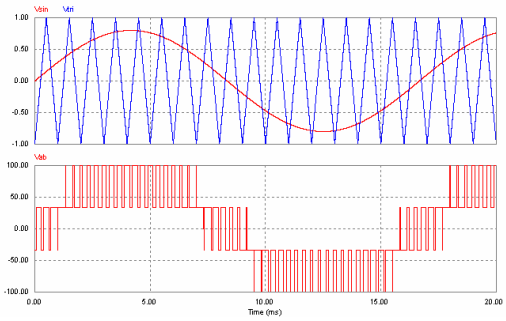

Fig. 12 - Simulation results.

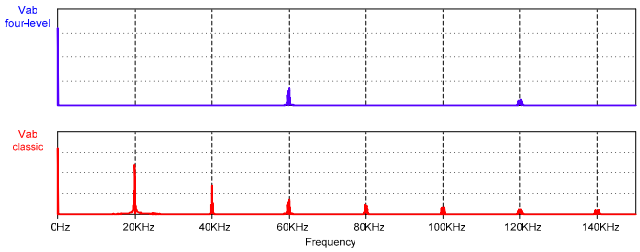

Fig. 13 - Harmonic spectra.

VII. EXPERIMENTAL RESULTS

In order to demonstrate the principle of operation and validate the analytical studies presented in this paper, an inverter with the characteristics depicted below was implemented.

P_{out} = 250 W, output power;
V_{out} = 65 V, output voltage;
V_{in} = 300 V, input voltage;
fs = 24 kHz, switching frequency;
f = 60 Hz, output frequency;
L_f = 410 μH, filter inductor;
C_f = 1 μF, filter capacitor.

Figure 14 shows the Vab voltage, output voltage and the current in the filter inductor, it can be noted that the Vab voltage has four levels.

In Fig. 15 and Fig. 16 the voltage across the switch S2, the voltage across the switch S5 and the current in the filter inductor when the converter operates with a duty-cycle of D=0.15 and D=0.85 are shown, respectively.

Figure 17 shows the photograph of the prototype implemented.

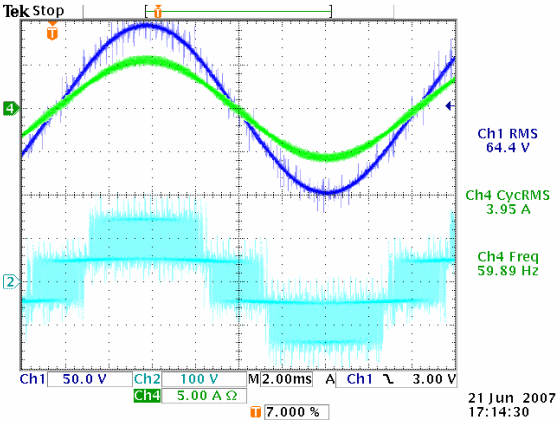

Fig. 14 – Output voltage (Ch1), 0Vab voltage (Ch2) and Lf current(Ch4).

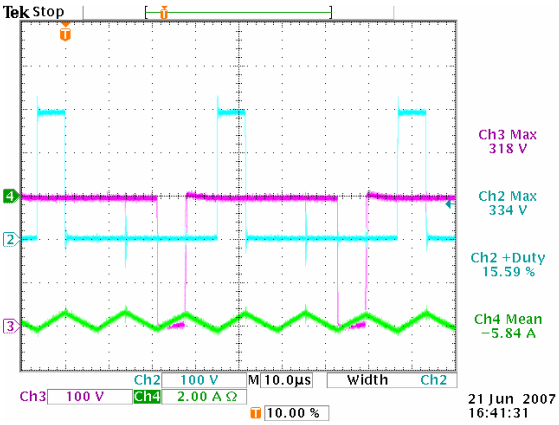

Fig. 15 – VS2 voltage (Ch2), VS5 voltage (Ch3) and Lf current(Ch4) ($D \cong 0.15$).

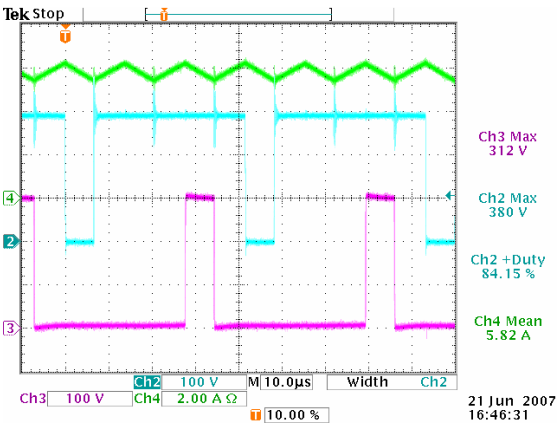

Fig. 16 – VS2 voltage (Ch2), VS5 voltage (Ch3) and Lf current(Ch4) ($D \cong 0.85$).

Fig. 17 - Photograph of the prototype.

VIII. CONCLUSIONS

In this paper, a new four-level half-bridge inverter, which uses a Y-Δ four-state switching cell, was proposed. For this converter, the operation principles, as well as simulation and experimental results were presented.

Among the advantages of the four-level half-bridge inverter, it should be emphasized: the output voltage presents four levels and its frequency is three times the switching frequency, making filtering an easier task; the current is divided among the switches, therefore, reducing the conduction losses.

The disadvantages are the need of a transformer as well as a higher number of switches.

In light of its characteristics, we believe that inverter is appropriate for industrial applications.

The concept of the proposed inverter can be extended to larger number of levels [1], and this will be analyzed in future publications.

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