PROPOSAL OF A SOFT COMMUTATION CELL APPLIED TO THE SINGLE-PHASE FULL-BRIDGE INVERTER

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***Abstract* — This paper presents an auxiliary cell that can be applied to the single-phase full-bridge inverter. The cell employs two auxiliary switches, two auxiliary diodes, a resonant capacitor, and a resonant inductor, and can be used in both inverter legs, so that switching losses can be minimized, implying increased efficiency and low EMI level. Three possible configurations are investigated, and theoretical analyses are carried out. Besides, the control strategy provides nearly sinusoidal output voltage, with reduced harmonic distortion. Experimental results are presented and discussed to validate the proposal.**

***Index Terms* — harmonic distortion, inverters, soft switching.**

I. INTRODUCTION

Voltage-source pulse width modulation (PWM) inverters have been widely used in industrial application such as uninterruptible power supplies, static frequency changes, and variable speed drives. This is due to their capability in allowing continuous and linear control of the frequency and fundamental component of the output voltage.

To accomplish the increasing requirement for power inverters with low output harmonic levels, improved dynamic performance, and high power density, high switching frequency is essential. However, operation in this condition results in the semiconductor devices being subjected to high switching stresses and high power losses. Additionally, due to the severe dv/dt and di/dt, the electromagnetic interference (EMI) increases with the switching frequency, while parasitic capacitances and stray inductances cause high current and voltage peaks during switching transients [1].

Power semiconductor devices commutate under two possible situations: hard and soft. With hard switching, the devices are supposed to change the states (on or off) when both current and voltage are not null. High switching stresses are due to the overlap between voltage and current, and high switching losses result [2]. Soft switching is supposed to reduce the mentioned overlap between voltage and current during the commutation, and can be classified in either active or passive methods.

Active methods can reduce the switching losses by using auxiliary switches. Unfortunately, an auxiliary switch increases the complexity of both the power circuit and the control circuit. Synchronization problems between control signals of two switches during transient also complicate the control strategy. Circuit cost is increased and reliability is affected by using active snubbers.

A passive lossless snubber can effectively restrict switching losses and EMI noise using no active components and no power dissipative components. No additional control is needed and no circulating energy is generated. Circuit structure is as simple as RCD snubbers while circuit efficiency is as high as active snubbers and resonant converters. Low cost, high performance, and high reliability are the distinct advantages of a passive lossless snubber. However, it is only possible to obtain zero current switching (ZCS) during turning on and zero voltage switching (ZVS) during turning off, respectively, by controlling the di/dt and dv/dt rates of the main switches, respectively. The choice between passive and active soft switching methods depends on a series of conditions [3], and this is not the scope of this work.

Particularly for PWM inverters, several soft switching techniques have been proposed, and nearly all topologies are able to achieve zero voltage switching [4] [5]. Among them, the soft-transition commutation cell is the most suitable, because soft switching conditions are achieved by means of an auxiliary shunt resonant network. This network provides the zero voltage transition (ZVT) or zero current transition (ZCT) condition for the main devices commutation. The choice between ZCT and ZVT depends on the semiconductor device technology that will be used [6]. In the case of majority carrier semiconductors, the best choice would be ZVS, where the capacitive turn-on losses can be eliminated. On the other hand, in the case of minority carrier semiconductors, the ZCS technique can avoid the turn-off losses caused by the current tail.

This paper proposes an auxiliary cell applied to the single-phase full-bridge inverter, so that switching losses are minimized, implying increased efficiency and reduced EMI levels. Three configurations are possible, which show the improvement of the basic cell. Key aspects of the inverter are investigated, such as the determination of the resonant tank parameters and overview of the employed control strategy. To validate the analysis, experimental results regarding three 2 kW prototypes are presented and discussed.

II. THE AUXILIARY COMMUTATION CELL

The basic cell proposed in this paper consists of two auxiliary switches, two auxiliary diodes, and a resonant tank, composed

by a capacitor and an inductor. For a single-phase full-bridge inverter, two auxiliary cells are supposed to be used. However, one must consider that the inverter has two legs. In usual applications, one leg operates at high frequency (e.g. on the order of kilohertz), and the other one operates at low frequency (e.g. 50 Hz or 60 Hz). Therefore only one cell is supposed to be employed, since the switching losses due to the low frequency leg are negligible. However, the analysis in the forthcoming sections considers two cells, for the case of a generic application where switching losses may be appreciable in both legs.

Three configurations involving the cell are possible, and discussed as follows. The following assumptions are considered in the analyses, valid for one switching cycle:

- The load current is constant and represented by I_o;
- The input current is constant and ripple-free;
- All semiconductor devices are ideal.

A. Auxiliary Cell with Antiparallel Diodes

In the first arrangement, the auxiliary diodes are placed in antiparallel with the switches. It must be mentioned that several types of semiconductor can be used as auxiliary switches, such as MOSFET's, IGBT's, and thyristors, as diodes may be or not intrinsic to them, depending on the application.

Since the paper aims to present the evolution of the proposed cell, the operating stages regarding the topology presented in Fig. 1 will not be discussed in detail in this paper.

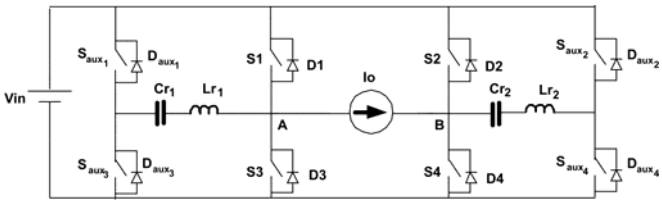


Fig. 1. Single-phase full-bridge inverter employing an auxiliary cell with antiparallel diodes.

B. Auxiliary Cell with Series Diodes

In the second arrangement, the auxiliary diodes are placed in series with the switches. Several types of semiconductor can be used as auxiliary switches e.g. MOSFET's, IGBT's, and thyristors. It must be mentioned that the presence of intrinsic diodes in auxiliary switches such as MOSFET's is not supposed to influence on the topology operation.

The main advantage of this topology compared with the previous one lies in the elimination of the parasitic resonance that occurs in the former fourth stage, what can be verified in the equivalent circuits and relevant waveforms.

Considering only one leg, the operation can be resumed to seven stages, as shown in Fig. 2, with the relevant waveforms represented in Fig. 3. The analysis is analogous for the remaining leg, although the switching frequency is not the same.

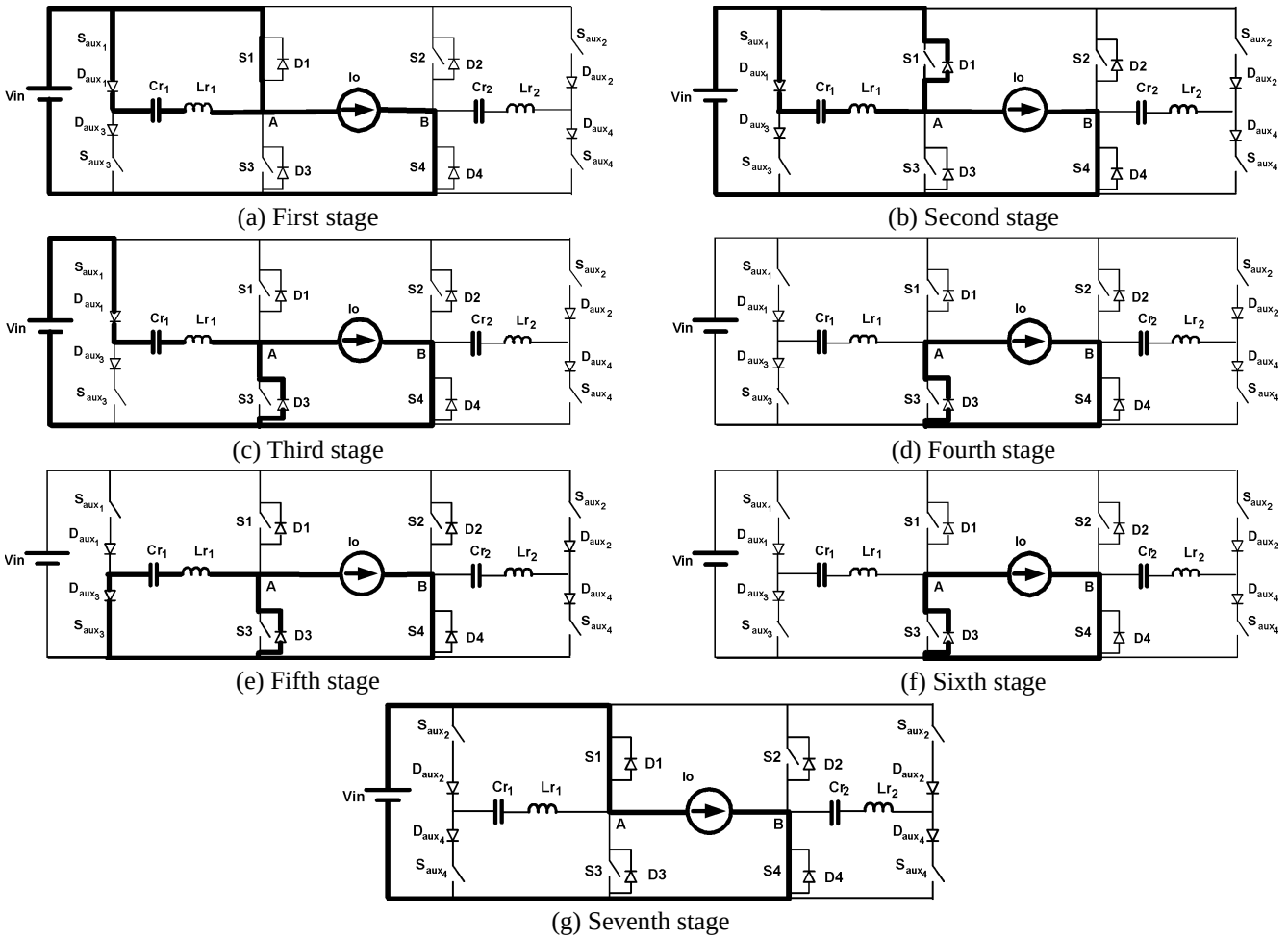


Fig. 2. Operating stages of the single-phase full-bridge inverter employing an auxiliary cell with series diodes.

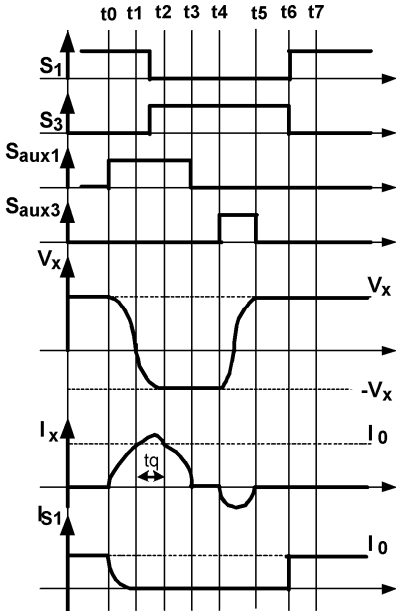


Fig. 3. Main theoretical waveforms.

First stage [t_0, t_1] (Fig. 2 (a)): Switch S_{aux1} is turned on, as the resonance between L_{r1} and C_{r1} begins. Load current I_o starts flowing though the resonant tank. The resonant current I_x increases, as the current through switch S_1 decreases proportionally.

Second stage [t_1, t_2] (Fig. 2 (b)): Diode D_1 is forward biased, and the current equal to the difference between I_x and I_o starts flowing through it. Such current represents the exceeding amount of energy from the resonance that causes switch S_1 to be turned off under zero current condition.

Third stage [t_2, t_3] (Fig. 2 (c)): Current I_x starts decreasing due to the charge of capacitor C_{r1}. Diode D_3 is forward biased, and part of the current of the resonant current flows through it, since the load current is constant.

Fourth stage [t_3, t_4] (Fig. 2 (d)): Switch S_{aux1} is turned off because capacitor C_{r1} is charged. The load current is freewheeling though diode D_3.

Fifth stage [t_4, t_5] (Fig. 2 (e)): Auxiliary switch S_{aux3} is turned on, as a new resonance begins so that capacitor C_{r1} is reverse charged. This stage finishes when the charging process is complete.

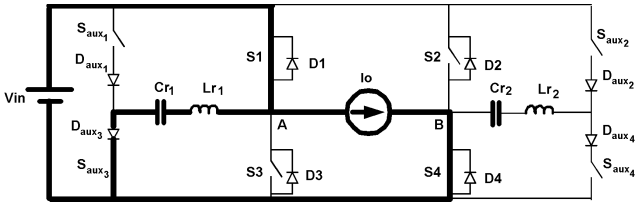
Sixth stage [t_5, t_6] (Fig. 2 (f)): When capacitor C_{r1} is fully charged, resonant current I_x becomes null, and diode D_{aux3} is forward biased.

Seventh stage [t_6, t_7] (Fig. 2 (g)): Switch S_1 is turned on under hard switching condition, as current I_o is assumed instantly, while diode D_3 is reverse biased.

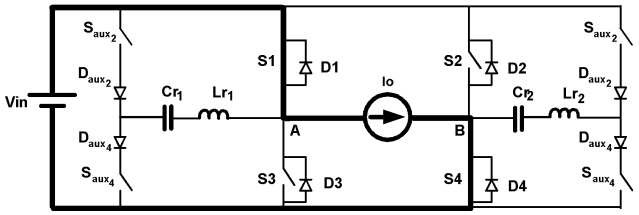
C. Auxiliary Cell with Series Diodes and Modified Gating Signals

In the second arrangement, the auxiliary diodes are also placed in series with the switches. However the gating signals is modified, so that the auxiliary switches are turned on twice within a switching cycle, and not only once as in the former configurations, what can be seen in the equivalent circuits and relevant waveforms. Besides, soft switching of the main switches is achieved during both turning on and off.

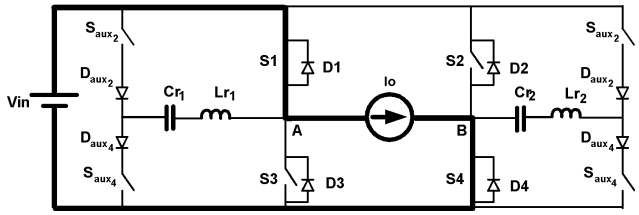
Considering only one leg, the operation can be resumed to twelve stages, as shown in Fig. 4, with the relevant waveforms represented in Fig. 5. The analysis is analogous for the remaining leg, although the switching frequency is not the same.



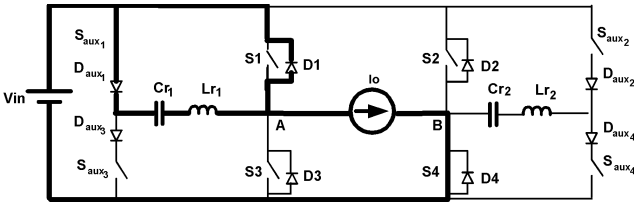
(a) First stage



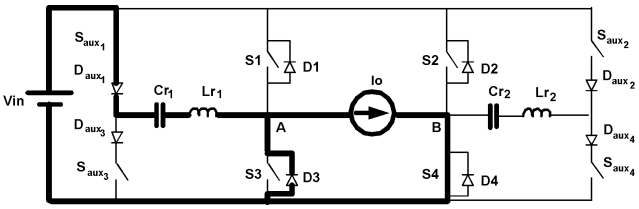
(b) Second stage



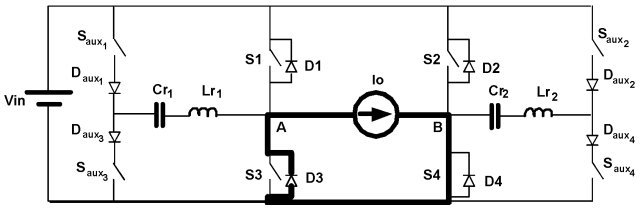
(c) Third stage



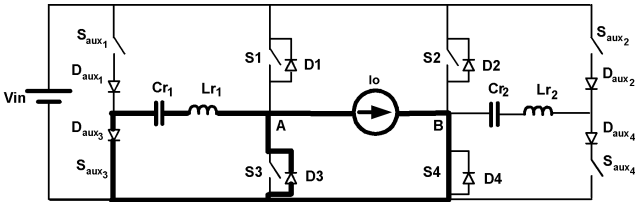
(d) Fourth stage



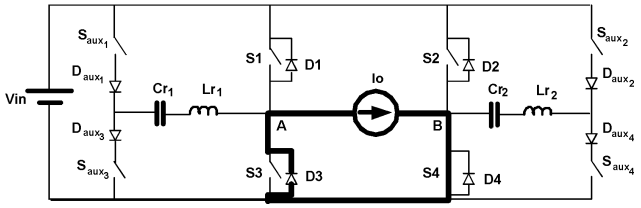
(e) Fifth stage



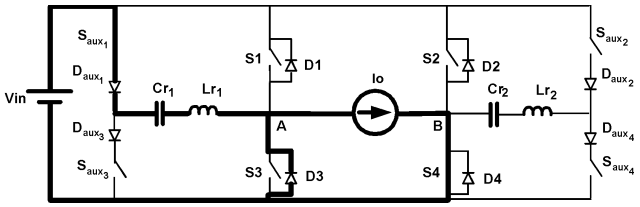
(f) Sixth stage



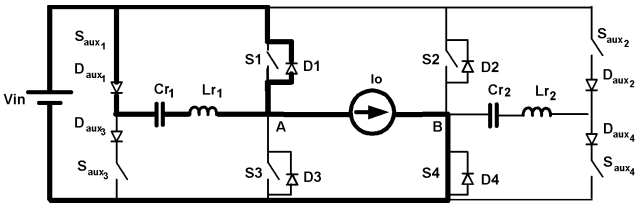
(g) Seventh stage



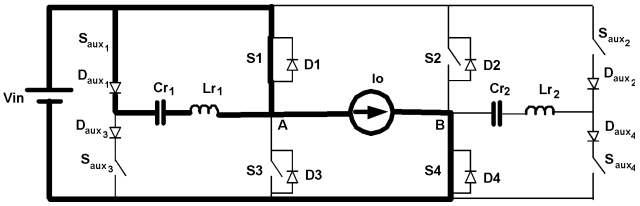
(h) Eighth stage



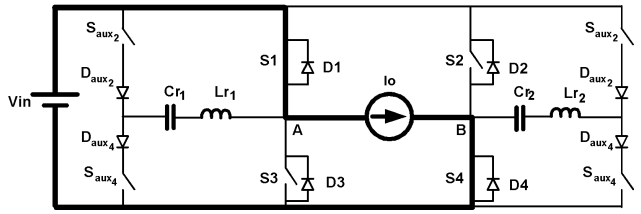
(i) Ninth stage



(j) Tenth stage



(k) Eleventh stage



(l) Twelfth stage

Fig. 4. Operating stages of the single-phase full-bridge inverter employing an auxiliary cell with antiparallel diodes and modified gating signals.

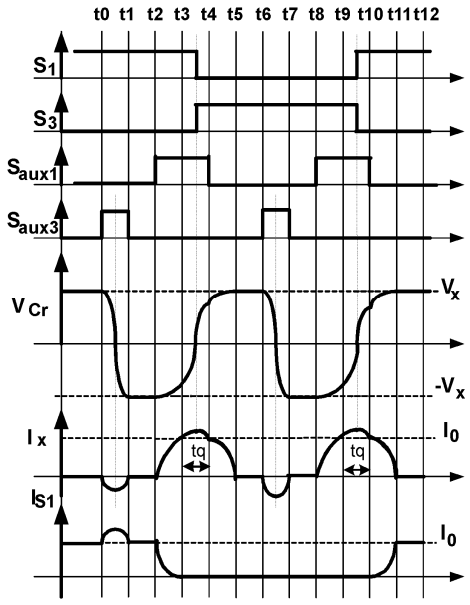


Fig. 5. Main theoretical waveforms.

First stage [t_0, t_1] (Fig. 4 (a)): Switch S_{aux3} is turned on, so that capacitor C_{r1} is reversely charged and resonant current I_x starts flowing through the resonant tank, which decreases and becomes null at instant t_1.

Second stage [t_1, t_2] (Fig. 4 (b)): Switch S_{aux3} is turned off. The load current flows through switch S_1, and the resonant capacitor remains negatively charged.

Third stage [t_2, t_3] (Fig. 4 (c)): Switch S_{aux1} is turned on so that main switch S_1 can be turned off with null current. The resonant current I_x increases, as the current through switch S_1 decreases proportionally. When I_x equals I_o, the current through S_1 becomes null.

Fourth stage [t_3, t_4] (Fig. 4 (d)): Diode D_1 is forward biased, since current I_x becomes greater than I_o. Since the current through main switch S_1 is null, it is turned off under zero current condition.

Fifth stage [t_4, t_5] (Fig. 4 (e)): The load current flows through the resonant tank, as capacitor C_{r1} is charged. Therefore current I_x starts decreasing. Diode D_3 is forward biased, so that current I_x becomes null and current I_o remains constant.

Sixth stage [t_5, t_6] (Fig. 4 (f)): Diode D_3 remains forward biased, as the load current is freewheeling though it.

Seventh stage [t_6, t_7] (Fig. 4 (g)): Switch S_{aux3} is turned on once again, so that switch S_1 can be turned on under soft switching condition. The resonance between L_{r1} and C_{r1} begins, as capacitor C_{r1} is reversely charged. The exceeding current flows though diode D_3, so that the load current remains constant. When C_{r1} is fully charged at t_7, current I_x becomes null.

Eighth stage [t_7, t_8] (Fig. 4 (h)): When the resonance finishes, the load current freewheels through diode D_3.

Ninth stage [t_8, t_9] (Fig. 4 (i)): Switch S_{aux1} is turned on, as the current though diode D_3 starts decreasing. It is blocked when the resonant current equals the load current.

Tenth stage [t_9, t_{10}] (Fig. 4 (j)): Diode D_1 is forward biased, since the resonant current becomes greater than I_o. The exceeding current is supposed to flow though it. Switch S_1 is turned on under zero voltage condition.

Eleventh stage [t_{10}, t_{11}] (Fig. 4 (k)): Switch S_1 is turned on, and current I_x starts decreasing. When capacitor C_{r1} is fully charged, the resonant current becomes null.

Twelfth stage [t_{11}, t_{12}] (Fig. 4 (l)): Load current I_o flows through switch S_1, as current I_x is null.

III. EXPERIMENTAL RESULTS

Experimental prototypes rated at 2kW were implemented regarding the aforementioned topologies. The parameters in

Table I are employed in the prototypes. The relevant results are presented and discussed as follows.

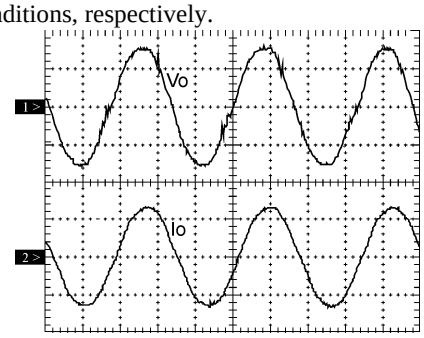
Table I. Parameters set used in the prototypes.

Parameter	Value
Output power	P_o=2000 W
DC input voltage	V_{in}=400 V
Rms output voltage	V_o=220 V
Inductive load	R=24 Ω L=1.8 mH
Output frequency	f_o=60 Hz
Switching frequency	f_s=30 kHz
Output current	I_0=15.4 A
Characteristic impedance	Z_0=15.3 Ω
Resonant inductor 1	L_{r1}=5.2 μH
Resonant capacitor 1	C_{r1}=7.4 nF
Resonant inductor 2	L_{r2}=2.6 mH
Resonant capacitor 2	C_{r2}=7.2 μF
Main switches S_1, S_2, S_3, S_4	IRFP460
Auxiliary switches S_{aux1}, S_{aux2}, S_{aux3}, S_{aux4}	IRFP460
Auxiliary diodes D_{aux1}, D_{aux2}, D_{aux3}, D_{aux4}	HFA08TB60

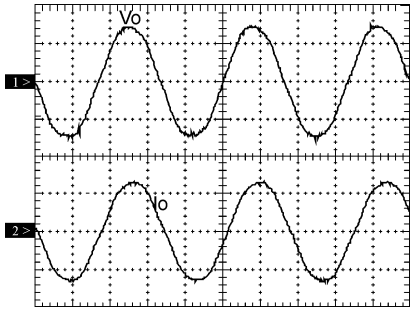
Fig. 6 shows the input voltage and input current waveforms for the aforementioned topologies under rated load condition. It can be seen that the control strategy provides nearly sinusoidal output voltage, as the harmonic distortion rates for Fig. 6 (a), (b), and (c) are 7.58%, 6.53%, and 6.17%, respectively.

Fig. 7 represents the resonant tank waveforms, which are in accordance with the theoretical study developed in Section II. It can be seen in Fig. 7 (b) and (c) that there is no parasitic resonance as in Fig. 7 (a), as predicted in the aforementioned analysis.

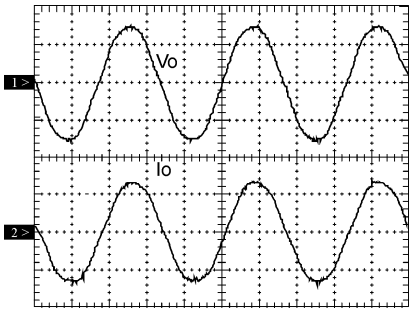
One can see in Fig. 8 the drain current and drain-to-source voltage on switch S_1 for rated load condition. In Fig. 8 (a) and (b), there are switching losses during turning on, but turning off occurs in zero current condition. On the other hand, for the auxiliary cell with series diodes and modified gating signals, switch S_1 is turned on and off under zero voltage and zero current conditions, respectively.



(a) Auxiliary cell with antiparallel diodes: V_o (200 V/div.); I_o (10 A/div.); time (5 ms/div.)

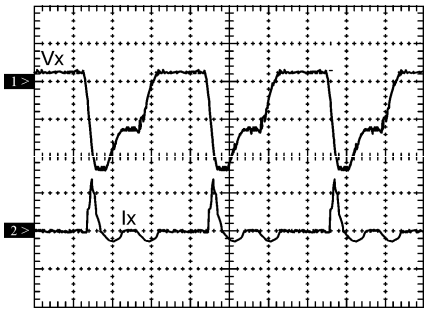


(b) Auxiliary cell with series diodes: V_o (200V/div.); I_o (10A/div.); time (5ms/div.)

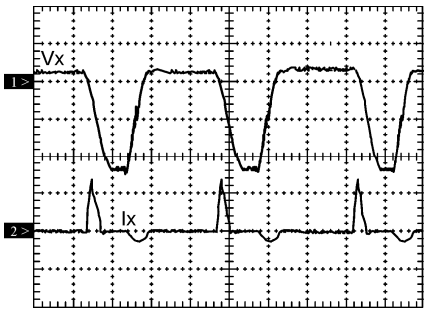


(c) Auxiliary cell with series diodes and modified gating signals: V_o (200V/div.); I_o (10A/div.); time (5ms/div.)

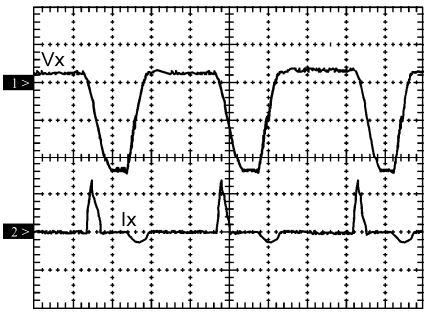
Fig. 6. Output voltage and output current.



(a) Auxiliary cell with antiparallel diodes: V_x (200 V/div.); I_x (1 A/div.); time (2 μs/div.)

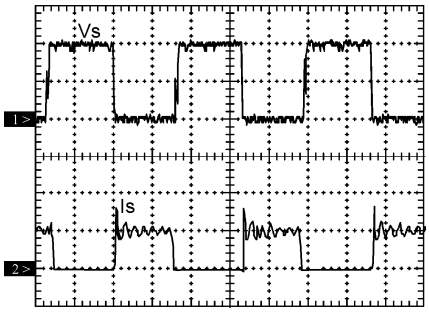


(b) Auxiliary cell with series diodes: V_x (200 V/div.); I_x (1 A/div.); time (2 μs/div.)

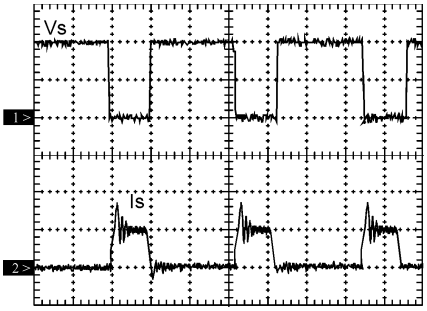


(c) Auxiliary cell with series diodes and modified gating signals: V_x (200 V/div.); I_x (1 A/div.); time (2 μs/div.)

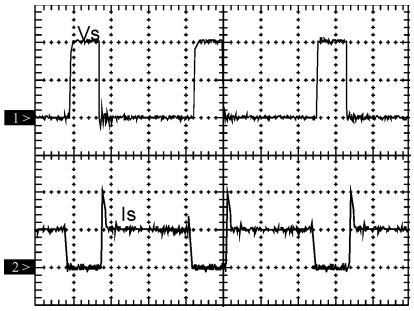
Fig. 7. Resonant tank waveforms.



(a) Auxiliary cell with antiparallel diodes: V_s (200 V/div.); I_s (5 A/div.); time (1 μs/div.)



(b) Auxiliary cell with series diodes: V_s (200 V/div.); I_s (5 A/div.); time (1 μs/div.)



(c) Auxiliary cell with series diodes and modified gating signals: V_s (200 V/div.); I_s (5 A/div.); time (1 μs/div.)

Fig. 8. Drain current and drain-to-source voltage on main switch S_1.

Fig. 9 depicts the efficiency curves for the full-bridge inverter with the high frequency leg operating at 30kHz. It can be seen that the introduction of the cell has increased efficiency if compared with the hard topology. The arrangement with series diodes and modified gating sequence presents the best performance e.g. efficiency has increased efficiency about 1.5%, due to soft switching during both turning on and off.

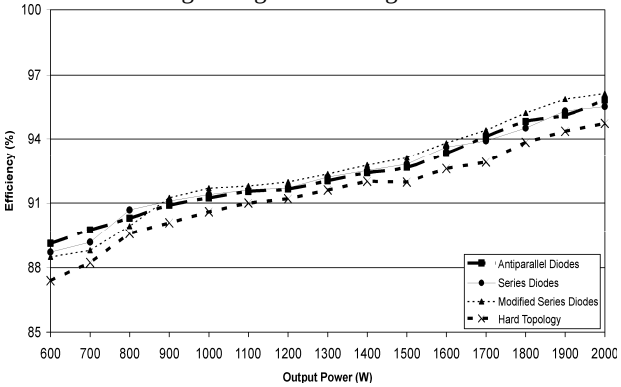


Fig. 9. Efficiency as a function of the output power.

IV. CONCLUSION

This work has presented an active auxiliary cell for the PWM full-bridge inverter, based on the resonance principle. Three configurations are possible in order to minimize switching losses and allow high frequency operation with increased efficiency. Although two cells are employed in the inverter legs, only one of them is really necessary if the output voltage frequency is low e.g. 50Hz or 60Hz for common applications. However both them are employed in the analysis to preserve symmetry.

The operating principle of the proposed auxiliary circuit was described and a simple design procedure of resonant tank was presented. The theoretical analysis was validated by experimental results obtained from three prototypes representing the studied topologies. The arrangement with series diodes and modified gating sequence has presented the best performance, with highest efficiency, which is due to the soft commutation during turning on and also turning off. In the remaining structures, soft switching could be obtained only during turning off.

V. REFERENCES

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