A Hybrid Control Strategy for Reduction of Switching Losses in Three-Phase Inverters with Current Control Loop

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Abstract: This paper deal with a hybrid control strategy for reducing the power losses in voltage source inverter (VSI) with current control loop. The current control technique is based on a sliding mode control (SMC) approach which permits the selection of the switching states of the power converter. Despite of the switching losses reduction due to the suitable selection of the inverter switching states, it can also be improved by clamping one pole of the inverter. The phase voltage clamped segments is synchronized with the current peak of the corresponding phase of VSI. In addition the proposed control strategy minimizes the interference among phases while allowing maximum output ac voltage to be obtained from the inverter. Distortion and losses study is also included. Simulation and experimental results are presented for corroborate the theoretical studies.

I. Introduction

Usually the design of the control system for power converters is usually performed into two steps: the selection of the control scheme and the suitable PWM pattern selection. The choice of the control strategy ensures the desired dynamical behavior of the closed loop system. The selection of the PWM pattern addresses voltage average outputs closed to the preselecting references with minimum switching losses. Both problems are solved separately by using linear controllers [1, 2] for accomplishing the desired dynamical performance and employing space vector PWM techniques for minimizing the switching losses [3]. It has been shown that the use of a sliding mode approach (SMC) can achieve these two requirements simultaneously [4]. The reduction of the switching losses can be also improved from the application of voltage clamped techniques on the selection of the inverter switching states [5,6]. However, the introduction of this voltage clamping scheme in one of the inverter pole results in non-linear system behavior. Therefore, to preserve the dynamics of the closed loop system and to accomplish the best power losses reduction it is necessary to define a different control scheme for choosing the optimum switching sequence.

Differently of the works proposed before, this paper introduces a hybrid control strategy for reducing the power losses in voltage source inverter (VSI) with current control loop. It is based on the integration of a sliding mode control (SMC) approach and a phase voltage clamped technique (SMC VC) which permits the suitable selection of the switching states of the power converter. The phase voltage clamped segments is synchronized with the current peak of the corresponding phase of VSI [6]. The proposed control strategy minimizes the interference among phases while allowing maximum output ac voltage to be obtained from the inverter. Distortion and losses study is also presented. Simulation and experimental results corroborate the theoretical studies.

II. System Description and Modelling

The basic scheme of a VSI controlled by proposed hybrid strategy SMC VC, discussed in this paper, is shown in Fig. 1. It comprises a standard three-phase VSI feeding a RLE load for representing a generic symmetrical three-phase load (i.e. a three-phase machine for instance.). The VSI is a standard converter composed power switches q_1 to q_6, and a capacitors bank as a DC-link. The conduction states of the switches can be represented by an homonymous binary pair variable $q_i \in \{0, 1\}$, $i = 1, .., 6$; where $q_i = 1$ indicates a closed switch while $q_i = 0$ an opened one. The pairs q_1q_4, q_2q_5 and q_3q_6 are complementary, therefore $q_4 = 1$ q_1, $q_5 = 1$ q_2 and $q_6 = 1$ q_3. The symmetrical three-phase load is composed by three-phase back- emf e_{s1}, e_{s2} and e_{s3} connected to phase impedances represented by series association of resistances and inductances (r_s and l_s). The VSI pole voltages can be obtained as

$$v^s_{k0} = (2q_k \quad 1)\frac{E}{2} \tag{1}$$

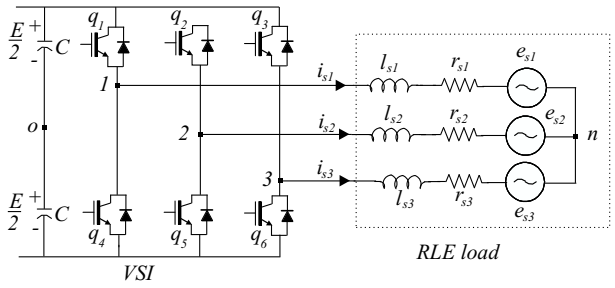

Fig. 1. Basic scheme of a VSI controlled by proposed hybrid strategy $SMC \quad VC$

where $k = 1, 2, 3$. The use of $K.L.V.$ on the equivalent circuit of Fig. 1(a) results in the following dynamic system model

$$\frac{di^s_{s123}}{dt} = \frac{r_s}{l_s} i^s_{s123} + \frac{1}{3l_s} v^s_{s123} \tag{2}$$

where superscript s refers to the stationary reference frame, $i^s_{s123} = [i^s_{s1} \; i^s_{s2} \; i^s_{s3}]$, and machine phase voltages v^s_{s123} are given by

$$\begin{aligned} v^s_{s1} &= 2(v^s_{10} \quad e^s_{s1}) \quad (v^s_{20} \quad e^s_{s2}) \quad (v^s_{30} \quad e^s_{s3}) \\ v^s_{s2} &= (v^s_{10} \quad e^s_{s1}) + 2(v^s_{20} \quad e^s_{s2}) \quad (v^s_{30} \quad e^s_{s3}) \\ v^s_{s3} &= (v^s_{10} \quad e^s_{s1}) \quad (v^s_{20} \quad e^s_{s2}) + 2(v^s_{30} \quad e^s_{s3}) \end{aligned} \tag{3}$$

These three-phase current-voltage dynamic model can be transformed into equivalent orthogonal dq components, through the 123 odq conservative transformation given by

$$\mathbf{x}^s_{odq} = \mathbf{A}\mathbf{x}_{123} \tag{4}$$

where $\mathbf{x}^s_{odq} = x^s_o \quad x^s_d \quad x^s_q$, $\mathbf{x}_{123} = x_1 \quad x_2 \quad x_3$ and

$$A = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \tag{5}$$

This results in equivalent dq machine model given by

$$\frac{di^s_{sdq}}{dt} = \frac{r_s}{l_s} i^s_{sdq} + \frac{1}{l_s}(v^s_{sdq} \quad e^s_{sdq}) \tag{6}$$

where $v^s_{sd} = u_{sd}\frac{E_{dq}}{2}$ and $v^s_{sq} = u_{sq}\frac{E_{dq}}{2}$, in which E_{dq} is a equivalent voltage of dc-link voltage E on the dq orthogonal reference frame. The state of power switches determines eight voltage vectors $\mathbf{v}_{sn} = v_{sdn} + jv_{sqn}$, $n = 0, 1, 2..., 7$, in which there are two zero space voltage vectors and six nonzero space voltage vectors, as presented in Fig. 2.

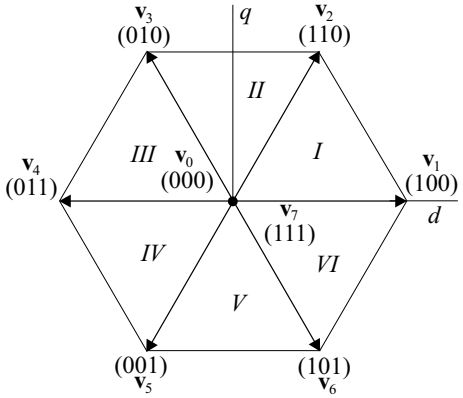

Fig. 2. VSI state space voltage vectors.

III. Proposed Control System

Fig. 3 presents the block diagram of the proposed control system. Blocks SM performs the sliding mode control strategies. It is implemented from the load phase currents errors σ^s_{sd} and σ^s_{sd} and, generate at their outputs tracking variables u_{sd} and u_{sq} as presented next. Blocks d/dt calculates the time derivative of current errors σ^s_{sd} and σ^s_{sd}. Block DPF calculates the load power factor based on the load phase current measurements and load phase voltages obtained from switching pattern of inverter switches. From the load power factor, block CR determines the phase angle intervals Φ_{ko}, in which the switches of each pole voltage inverter will be clamped as the proposed technique. Both current errors and their time derivatives together to phase angle intervals Φ_{ko} are employed for selecting the inverter space voltage vector to be used. This is performed by block KB which implements a knowledge based rule which will be described next.

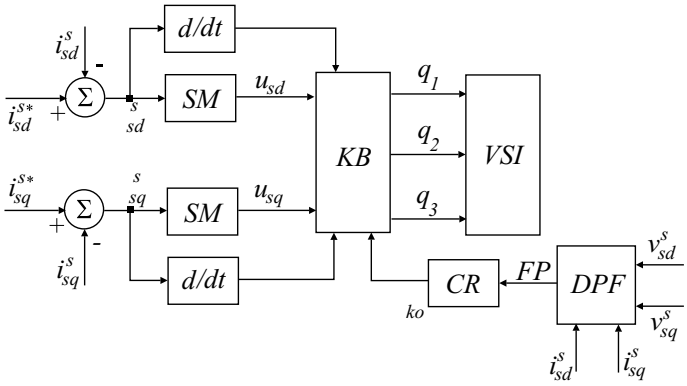

Fig. 3. Block diagram of the proposed $SMC \quad VC$ control system.

TABLE 1. The switching function table of power converter switches states without clamping technique.

σ^s_{sd}	+	+	+	+	+	+	+	+								
$\dot{\sigma}^s_{sd}$	+	+	+	+					+	+	+	+				
σ^s_{sq}	+	+			+	+			+	+			+	+		
$\dot{\sigma}^s_{sq}$	+		+		+		+		+		+		+		+	
$\mathbf{v}_{sk}$	$\mathbf{v}_{s2}$	$\mathbf{v}_{s1}$	$\mathbf{v}_{s1}$	$\mathbf{v}_{s6}$	$\mathbf{v}_{s2}$	$\mathbf{v}_{s07}$	$\mathbf{v}_{s07}$	$\mathbf{v}_{s6}$	$\mathbf{v}_{s3}$	$\mathbf{v}_{s07}$	$\mathbf{v}_{s07}$	$\mathbf{v}_{s5}$	$\mathbf{v}_{s3}$	$\mathbf{v}_{s4}$	$\mathbf{v}_{s4}$	$\mathbf{v}_{s5}$

A. SRM Current Control Strategy

The control goal is to track the reference currents which should be selected from desired dynamic of closed loop system. The basis for the solution can be accomplished by introducing a sliding mode motion into the system. Now consider the current errors of dq axis that can be expressed as

$$\sigma^s_{sdq} = i^{s*}_{sdq} \quad i^s_{sdq} \tag{7}$$

where i^{s*}_{sdq} are the desired reference currents. From equations (6), one can obtain the derivatives of the current errors as

$$\frac{d\sigma^s_{sdq}}{dt} = \quad \frac{r_s}{l_s}\sigma^s_{sdq} + \frac{di^{s*}_{sdq}}{dt} + \frac{r_s}{l_s}i^{s*}_{sdq} \quad \frac{1}{l_s}(v^s_{sdq} \quad e^s_{sdq}) \tag{8}$$

From the equations (8), it can be verified that the dq machine phase currents have time constant $_s = l_s/r_s$ and are influenced by reference currents, derivatives of reference currents, machine $back \quad emf$ and inverter voltage vectors. Qualitatively, the current error derivatives could be driven by nonzero voltage vectors which makes the machine phase currents track their respective references. On the other hand, if the zero voltage vectors are employed the equations (8) become

$$\frac{d\sigma^s_{sdq}}{dt} = \quad \frac{r_s}{l_s}\sigma^s_{sdq} + \frac{di^{s*}_{sdq}}{dt} + \frac{r_s}{l_s}i^{s*}_{sdq} + \frac{1}{l_s}e^s_{sdq} \tag{9}$$

Hence, the current errors derivatives will be driven the reference current and machine $back \quad emf$. Thus, for making the machine phase currents tracking the desired references it is necessary determine suitable nonzero voltage vectors. However, the use of zero voltage vectors reduces the inverter switching frequency. Therefore, the control problem is to find a suitable switching sequence for the power converter so that the given dynamical specifications of closed-loop system are satisfied.

By selecting the manifold

$$\sigma^s_{sdq} = i^{s*}_{sdq} \quad i^s_{sdq} = 0 \tag{10}$$

for providing the desired motion of the overall system. The sliding conditions can be determined from the stability requirements as follows. Selecting the Lyapunov-like function given by

$$V(\sigma^s_{sdq}) = \frac{1}{2}(\sigma^s_{sdq})^2 > 0 \tag{11}$$

Admitting that the control command v^s_{sdq} which satisfies the stability conditions can be determined as

$$v^s_{sdq} = \frac{E_{dq}}{2} sign(\sigma^s_{sdq}) \tag{12}$$

Therefore, the sliding mode existence is obtained as the following conditions are fulfilled

$$\sigma^s_{sd}\dot{\sigma}^s_{sd} < 0 \quad and \quad \sigma^s_{sq}\dot{\sigma}^s_{sq} < 0 \tag{13}$$

these conditions guarantee the attraction of the system to the desired sliding surface.

To implement the proposed technique it is necessary to select the voltage vector to be applied from all possible values determined by switching states of $q_1 \quad q_6$ as presented next. For accomplishing this selection we use the time derivative of dq machine phase currents, together with the output of commands u^s_{sdq}. For instance, consider that the case when $u^s_{sd} > 0$. If its derivative is positive one can consider the use of a suitable nonzero voltage vector. Otherwise, if the signal corresponded derivative is negative it can be employed a zero voltage vector. Table 1 presents the proposed switching function of power converter switches states of the proposed control strategy. In this table, the possible signals of σ^s_{sd}, σ^s_{sq}, $\dot{\sigma}^s_{sd}$and $\dot{\sigma}^s_{sq}$are used for determining the suitable voltage vector. In the columns in which zero voltage vectors are employed there are two possibilities $\mathbf{v}_{s0}$ or $\mathbf{v}_{s7}$, the choice between them is made inspecting which nonzero voltage vectors was applied before. For instance, if the previous voltage vector was $\mathbf{v}_{s1}$, $\mathbf{v}_{s3}$ or $\mathbf{v}_{s5}$ the zero voltage vector employed will be $\mathbf{v}_{s0}$, otherwise $\mathbf{v}_{s7}$ is used.

B. Voltage Clamped Technique

The reduction of the converter power losses can be obtained by selecting a suitable switching pattern as proposed before. This reduction can be also improved if each leg of the inverter can be clamped alternatively on positive or negative rail of dc-link for 120° intervals of the

TABLE 2. The switching function table of power converter switches states with clamping technique on phase 1.

σ^s_{sd}	+	+	+	+	+	+	+	+								
$\dot{\sigma}^s_{sd}$	+	+	+	+					+	+	+	+				
σ^s_{sq}	+	+			+	+			+	+			+	+		
$\dot{\sigma}^s_{sq}$	+		+		+		+		+		+		+		+	
$\mathbf{v}_{sk}$	$\mathbf{v}_{s2}$	$\mathbf{v}_{s1}$	$\mathbf{v}_{s1}$	$\mathbf{v}_{s6}$	$\mathbf{v}_{s2}$	$\mathbf{v}_{s7}$	$\mathbf{v}_{s7}$	$\mathbf{v}_{s6}$	$\mathbf{v}_{s2}$	$\mathbf{v}_{s7}$	$\mathbf{v}_{s7}$	$\mathbf{v}_{s6}$	$\mathbf{v}_{s2}$	$\mathbf{v}_{s7}$	$\mathbf{v}_{s7}$	$\mathbf{v}_{s6}$

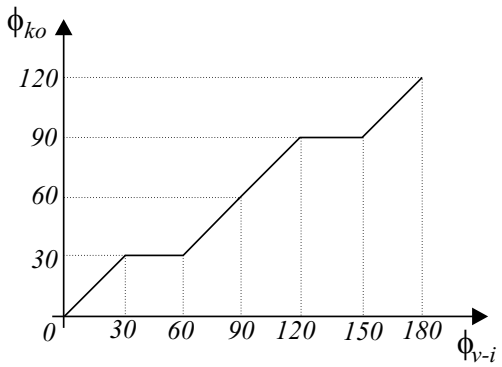

Fig. 4. Modified load power angle Φ_{ko} as a function of load power factor.

fundamental period. This time interval is distributed in two subintervals of 60° of no switching region to positive and negative peak of inverter phase currents respectively. This loss minimization results from the following two factors [6]: (a) low switching frequency ration, and (b) absence of switching in the vicinity of peaks of the inverter output phase currents. The clamped segments of each output phase of the inverter varies with the machine power factor $\Phi_{v\ i}$. Generically, the angle when the clamped segment starts can be given by 60° Φ_{ko}. After that, the corresponded inverter phase remains clamped for 60° electrical degrees. Thus, the clamped strategy must determine the modified power factor angle Φ_{ko} as a function of load power factor angle $\Phi_{v\ i}$, as shown in Fig. 4. In the proposed control strategy represented by block diagram 3, the modified switching sequence of the inverter power switches can be determined by blocks DPF, CR and KB. For instance, consider the case in which the output phase 1 of the inverter is clamped on the positive rail of the dc-link. The resultant switching function of the power converter switches can be given in table 2. This table is obtained by considering that the power switch q_1 remains closed during the 60° interval. Thus, from the possible voltage vectors determined by the switching states of power converter switches, only four possible vectors can be employed. They are three nonzero voltage vectors $\mathbf{v}_{s1}$, $\mathbf{v}_{s2}$ and $\mathbf{v}_{s6}$ and a zero voltage vector $\mathbf{v}_{s7}$. This addresses to a reduction of the effectiveness of the control strategy during this time interval.

IV. Simulation and Experimental Results

The performance of the proposed SMC VC was evaluated by simulation and experimental results. To realize the simulation tests, it was implemented a simulation program written in C^{++} language which implements a full drive system. It is composed by power inverter, RLE load, current measurement and proposed SMC VC control scheme. The experimental results was obtained from a laboratory setup composed by a microcomputer equipped with a specific data acquisition card, a control board and a induction motor drive as RLE load. The command signal of power converter are generated by a microcomputer with a sampling time of 50 s. The data acquisition card employs Hall effect sensors and 12 bits A/D converters.

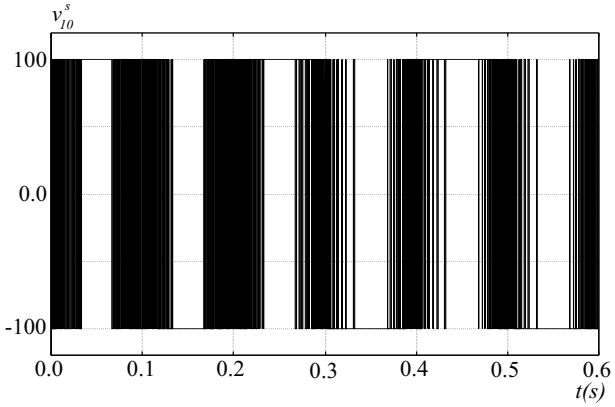

Fig. 5. Simulation result of inverter pole voltage v^s_{10}.

Figures 5-6 present the simulation results realized for evaluating the effectiveness of the proposed control strategy. Fig. 5 shows the inverter pole voltage v^s_{10} generated for imposing the reference current presented in the Fig. 6. In this figure is show the inverter output phase current i^s_{s1} superimposed by its respective reference current i^{s*}_{s1}. In this test the reference current is initially settled in $i^{s*}_{s1} = 1.0A$. At time $t = 0.25s$, a positive current step of $0.4A$ is applied on the reference current. The power factor angle of the load is $\Phi_{v\ i} = 0°$ and the proposed clamping technique is employed. This can be verified on both

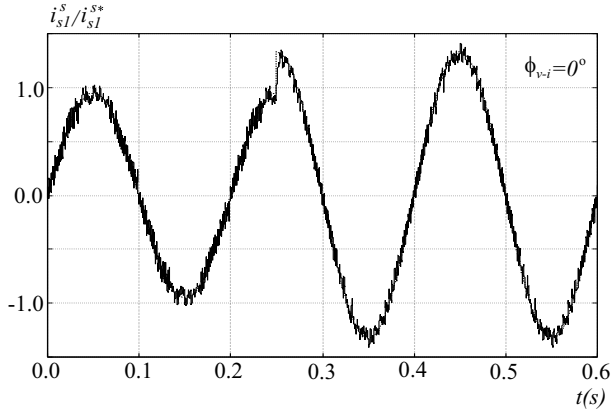

Fig. 6. Simulation result of machine phase current i^s_{s1} superimposed by its reference current i^{s*}_{s1} for $SMC \quad VC$ with $\Phi_{v-i} = 0°$.

figures of simulation results. It is important to observe that the machine phase current follows its reference current with a fast transient response. The harmonic pollution imposed by the proposed method was also evaluated. It was made three tests that are: (i) the proposed current control strategy without voltage clamping technique (SMC), (ii) $SMC \quad VC_1$ with load power angle $\Phi_{v \ \ i} = 0°$ and, (iii) $SMC \quad VC_2$ with load power angle $\Phi_{v \ \ i} = 45°$. The results obtained n these tests are presented in table 3. Analyzing this table one can observe that there is a little increase on the THD when the clamping technique is used, however the losses of the power converter is minimized as mentioned before.

TABLE 3. Comparison of the THD of the proposed method as a function of the use of clamping technique and load power factor.

$Method$	SMC	$SMC \quad VC_1$	$SMC \quad VC_2$
THD	3.45%	4.65%	5.36%

Figures 7-9 present the experimental results realized. In Fig. 7 is shown the experimental results of the the inverter output phase current i^s_{s1} superimposed by its respective reference current i^{s*}_{s1} for the case in which the proposed current control strategy is employed without the clamping technique. The test conditions is the same of the simulation test presented before. As in the simulation essay, the machine phase current follows its respective reference with a fast transient response. In the result presented in Fig. 8, the clamping technique is introduced for load power angle $\Phi_{v \ \ i} = 0°$. In comparison with the corresponded simulation test, one can observe that both tests have almost the same performance. Finally, in Fig. 9 the test is now effectuated with load power angle $\Phi_{v \ \ i} = 45°$. In this case it cab be verified that there is a discrete distortion on the controlled current. However, the machine phase phase current also follows in average its respective reference current.

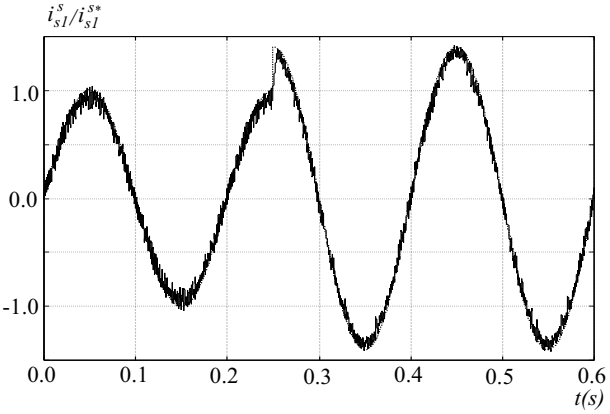

Fig. 7. Experimental result of machine phase current i^s_{s1} superimposed by its reference current i^{s*}_{s1} for SMC without clamping technique.

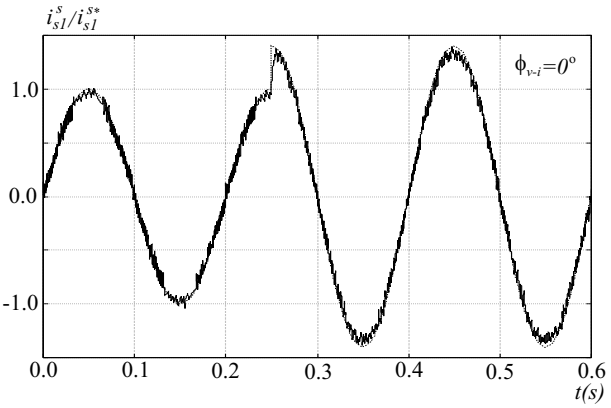

Fig. 8. Experimental result of machine phase current i^s_{s1} superimposed by its reference current i^{s*}_{s1} for $SMC \quad VC$ with $\Phi_{v-i} = 0°$.

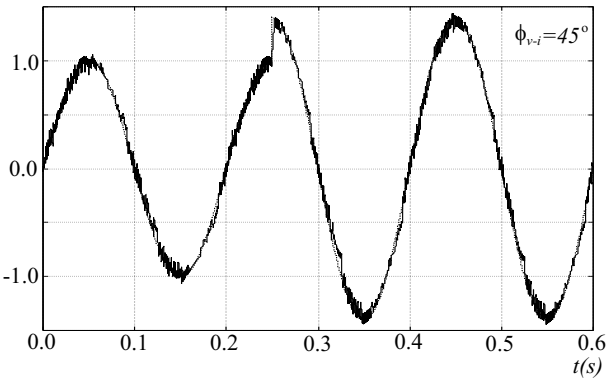

Fig. 9. Experimental result of machine phase current i^s_{s1} superimposed by its reference current i^{s*}_{s1} for $SMC \quad VC$ with $\Phi_{v-i} = 45°$.

V. Conclusions

This paper has presented a hybrid control strategy for reducing the power losses in voltage source inverter with current control loop. It is based on the integration of a sliding mode control and a clamping technique of the inverter pole voltage. This integration permits a suitable selection of the power converter switches states which minimizes power converter losses. Both techniques was presented and analyzed. The implementation of the proposed control scheme presents a simple implementation. The simulation and experimental results demonstrate that the proposed $SMC \quad VC$ has presented a good performance.

References

[1] D. M. Brod and D. W Novotny. Current control of vsi-pwm inverters. *IEEE Trans. Ind. Applicat.*, 21(4):562–570, 1985.

[2] M. P. Kazmierkowski and L. Malesani. Current control techniques for three-phase voltage source pwm converters: A survey. *IEEE Trans. Ind. Electron.*, 45(5):691–703, 1998.

[3] H. W. V. Broeck, H. Skudelny, and G. V. Stanke. Analysis and realization of pulsewidth modulator based on voltage space vectors. *IEEE Trans. Ind. Applicat.*, 24(1):142–150, 1988.

[4] N. S. Behlilovic, A. Sabanovic, K. Jezernic, and O. M. Kaynac. Current control in three-phase switching converters and ac electrical machines. In *Conf. Rec. PESC*, pages 581–586, 1994.

[5] L. Malesani, P. Tenti, E. Gaio, and R. Piovan. Improved current control technique of vsi pwm inverters with constant modulation frequency and extended voltage range. *IEEE Trans. Ind. Applicat.*, 27(2):365–369, 1991.

[6] M. C. Cavalcanti, E. R. C. da Silva, A. M. N. Lima, C. B. Jacobina, and R. N. C. Alves. Reducing losses in three-phase pwm pulsed dc-link voltage-type inverter systems. *IEEE Trans. Ind. Applicat.*, 38(4):1114–1122, 2002.