AN ISOLATED AC-DC SINGLE-STAGE FULL-BRIDGE CONVERTER POWER FACTOR CORRECTED WITH INTERLEAVED BOOST INPUT TYPE

Paulo C. S. Ficagna & José Renes Pinheiro
Power Electronics and Control Research Group - GEPOC
Federal University of Santa Maria – UFSM
ZIP Code: 97015-900 – Santa Maria, RS – Brazil
paulоficagna@gmail.com, renes@ctlab.ufsm.br

Abstract – In this paper, a new steady-state analysis for an Isolated AC-DC Single-Stage Full-Bridge Converter Power Factor Corrected with Interleaved Boost Input Type operating in continuous conduction mode is presented. Flux-reset of High-Frequency Transformer (HFT) and mitigation of circulating reactive energy conditions, design considerations, and the validation of theoretical analysis by numerical simulation are provided.

***Keywords* – Single-Stage, PFC, AC-DC, Interleaved, Boost, Full-Bridge, Isolated Converter, High-Frequency Transformer.**

I. INTRODUCTION

To meet the requirements defined in norms, as IEC61000-3-2, which restrict harmonics emissions, the use of power factor corrected (PFC) converters is largely adopted. A well know solution is the use of AC-DC Two-Stage Converters (TSCs). As the power is processed twice, this solution has as main drawback a penalty in the efficiency.

To overcome this, AC-DC Single-Stage Converters (SSCs) topologies has been proposed in many papers [1-4]. Compared with TSC solution, SSC has, potentially, better efficiency and reliability, due to reduction of semiconductor devices and the fact that the power is processed in only one stage.

In Discontinuous Conduction Mode (DCM) SSC [4] the input current naturally follows the line voltage. With a wide bandwidth voltage control loop, these SSC have good dynamical behavior with a neglected low frequency output voltage ripple. However, due to large conduction losses, their use is restricted to low power applications. The topology presented in [2] is an integration of an Interleaved Boost PFC with a Transformer-Isolated Full-Bridge Converter, both in DCM. Its main advantages are: EMI problems filters reduced and wide bandwidth output voltage control loop. However, it operates in DCM and conduction losses still degrade its efficiency.

A new topology, similar to presented in [2], was proposed in [1]. This topology operates in CCM and, with reduced dissipating elements, has, comparatively, lower conduction losses. However, the solution presented by the authors has a narrow conduction angle, large output voltage ripple and four control loops, where two of these loops have to be adjusted experimentally. In this article, based on a new and more detailed steady-state analysis, the conditions that achieve magnetic flux-reset of the HFT and mitigation of circulating reactive energy are provided. Also, power transference during all line period is feasible due to a proposed input current control strategy.

In section II, the analysis of the converter is presented. The design guidelines are showed in section III. In section IV, the results of numerical simulation are provided. The conclusions are in section V.

II. OPERATING PRINCIPLE AND CONVERTER ANALYSIS

The topology proposed in [1] is showed in Figure 1. Some conditions are defined for the following analysis in this section:

- Input voltage: $v_{in}(t) = V_{in}\sin(2\pi f_{line}t)$;
- Constant output current $I_o = V_o / R_o$ (small *ripple* approximation);
- Turns ratio of HFT T_1: $n = \frac{N_p}{N_{s1}} = \frac{N_p}{N_{s2}}$;
- $C_1 = C_2 = C_{Bus}$ and $L_1 = L_2 = L$;
- Switching frequency much larger than line frequency: $f_s >> f_{line}$;
- C_1 and C_2 have constants (small *ripple* approximation) and equals DC voltages (V_c) where $V_{in} < V_{C1} = V_{C2} = V_c$.

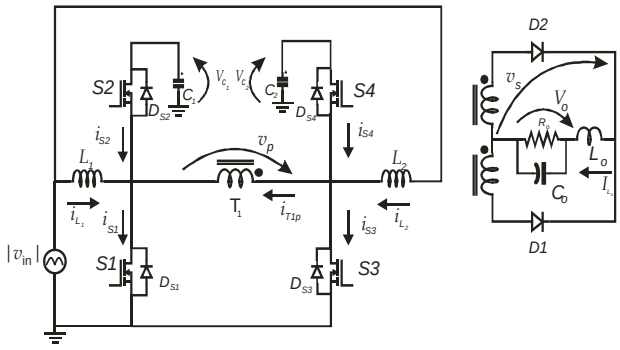

Figure 1 – Topology proposed in [1].

A. Operating Principle within One Switching Period

With $v_{in}(t) \cong V_{in}$ and considering the currents of the inductors L_1 and L_2 with maximum and minimum positive values, $I_{L1(2)M}$ and $I_{L1(2)m}$ respectively, and $I_{L1(2)M} < I_o/n < I_{L1(2)m}$, the main waveforms and the gating

signals of the switches *S1-S4* are showed in Figure 2 and Figure 3, respectively.

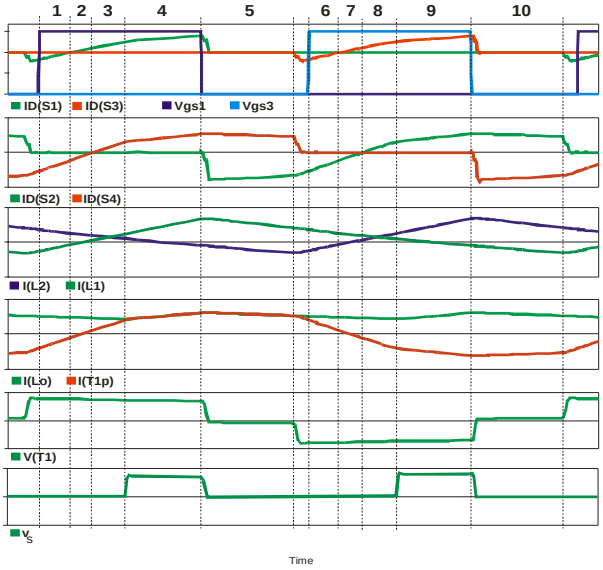

Figure 2 – Main waveforms of the converter within a switching period at steady-state condition.

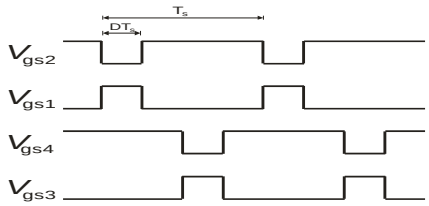

Figure 3- Gating signals of the switches *S1-S4* [1].

First stage ($i_{L1} < I_o/n = -i_{T1}$): With D_{S1} and D_{S4} on conducting state, see Figure 4, L_1 is linearly charged by V_{in} and the voltage V_c is applied in T_1 while L_2 is linearly discharged. In this condition, the diodes D1 and D2 conducts the current I_{Lo}. Thus, the leakage inductance (L_d), at the primary side, assumes all the voltage applied on T_1. C_2 absolve the energy initially stored in L_d and part of the energy previously stored in L_2. No power is transferred from input to load (R_o) which is provided by the output filter (C_o and L_o). When i_{L1} becomes equal to i_{T1}, the next stage begins.

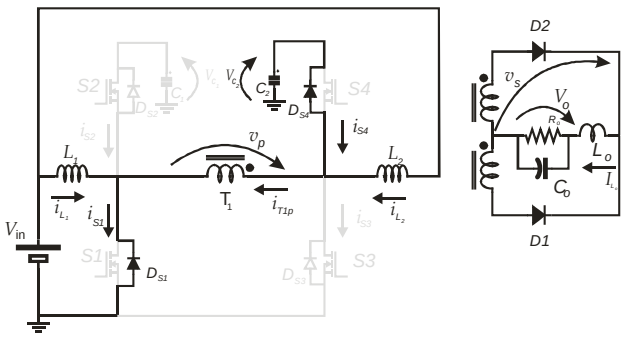

Figure 4 - First stage ($i_{L1} < I_o/n = -i_{T1}$).

Second stage ($i_{L1} \geq i_{T1}$): This stage is similar to the previous one. It only differs by the commutation of *S1* on ZVS condition assuming the current i_{T1} plus i_{L1}, see Figure 5. When $i_{T1} > i_{L2}$, this stage ends.

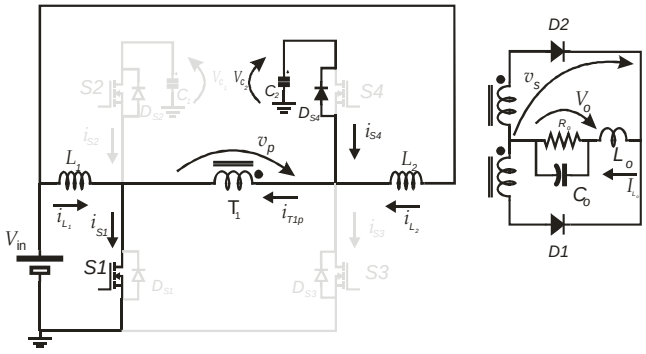

Figure 5 - Second stage ($i_{L1} \geq i_{T1}$).

Third Stage ($i_{T1} \geq i_{L2}$): In this stage, the commutation of the switch *S4* occurs on ZVS condition, see Figure 6. When $i_{T1} = I_o/n$, the next stage begins.

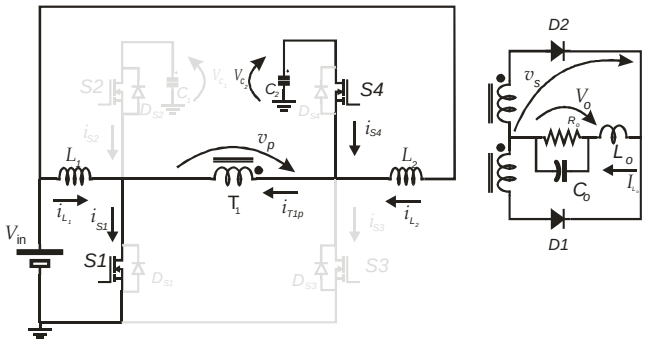

Figure 6 - Third Stage ($i_{T1} \geq i_{L2}$).

Fourth stage ($i_{T1} = I_o/n$): With *S1* and *S4* on conducting state, the power is transferred from input to output, see Figure 7. The charging and discharging condition of L_1 and L_2, respectively, are the same to the previous stages. When *S1* stops to conduct and *S2* is able to conduct, the next stage starts.

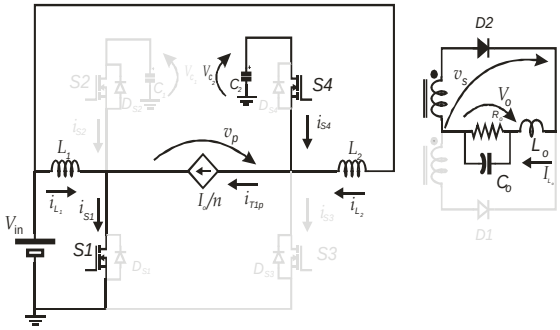

Figure 7 - Fourth stage ($i_{T1} = I_o/n$).

Fifth stage ($i_{T1} = {}^{I_o}\!/_{n}$ e $v_p = 0$): With *S4* and D_{S2} on conducting state, see Figure 8, a zero differential voltage is applied on the terminals of T_1. The energy delivered to the load is provided only by the output filter.

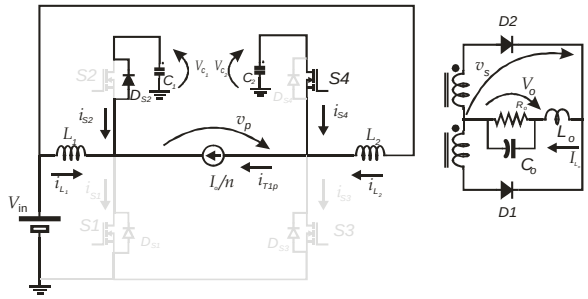

Figure 8 - Fifth stage ($i_{T1} = {}^{I_o}\!/_{n}$ e $v_p = 0$).

The remaining stages are similar to the previously presented and were omitted. Particularly, for $d_{Boost} > 0.5$, in the fifth (and tenth stages), the switches and their respective body diodes on conducting state are *S1(3)* and *D3(1)*, instead of *S2(4)* and *D4(2)*.

B. Steady-State Gain

Neglecting the effect of non idealities and sharing the theoretical analysis of the converter in two parts, they are: input stage, similar to a conventional interleaved Boost converter, and output stage, similar to a Buck converter, the derivation of steady-state gain is obtained considering the variable control of the Interleaved Boost Stage (IBS) showed in Figure 9 and defined in (1).

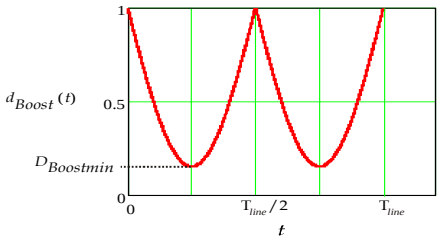

Figure 9- Control variable for the Interleaved Boost stage.

$$d_{Boost}(t) = 1 - \frac{V_{in}}{V_c} \cdot \sin(2 \cdot \pi \cdot f_{line} \cdot t) \quad (1)$$

$$D_{Boost\,\min} = 1 - \frac{V_{in}}{V_c} \quad (2)$$

1) Steady-State Gain for $D_{Boostmin} \leq d_{Boost} < 0.5$

Based on Figure 10:

$$D_{Buck} = \frac{2 \cdot t_c}{T_s} \rightarrow D_{Buck} = 2 \cdot D_{Boost} \quad (3)$$

$$\overline{v}_o = \frac{1}{T_s}\int_0^{T_s} v_o(t)dt \Rightarrow \overline{v}_o = 2 \cdot \frac{V_c}{n} \cdot D_{Boost} \quad (4)$$

$$V_c(D_{Boost\,\min}) = \frac{V_{in}}{1 - D_{Boost\,\min}} \quad (5)$$

Substituting (5) in (4), the steady-state gain, for $D_{Boostmin} \leq d_{Boost} < 0.5$, is defined by

$$\frac{\overline{v}_o}{V_{in}} = \frac{2 \cdot d_{Boost}(t)}{n \cdot \left(1 - D_{Boost\,\min}\right)} \quad (6)$$

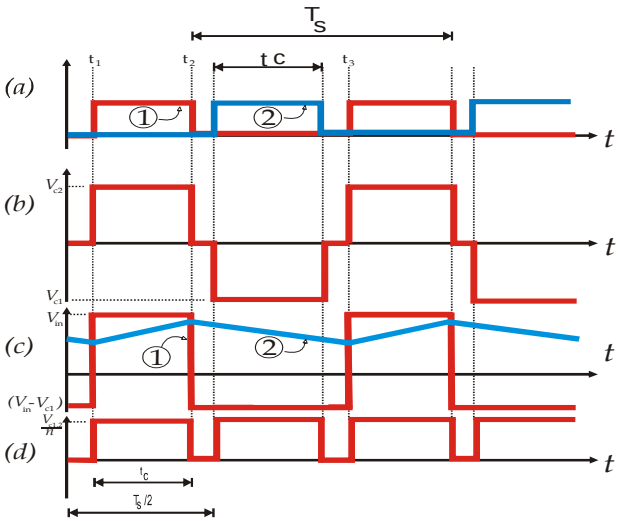

Figure 10 – Waveforms of gating signals of *S1*, (a)1, and *S2*, (a)2; voltage on the terminals of T_1 (v_p), (b); voltage, (c)1, and current, (c)2, on L_1 and the voltage applied on output filter (v_s), (d).

2) Steady-State Gain for $0.5 \leq d_{Boost} < 1$

Based on Figure 12, the steady-state gain can be obtained as following:

$$\overline{v}_o = \frac{1}{T_s}\int_0^{T_s} v_o(t)dt = \frac{V_c}{n} \cdot D_{Buck} \quad (7)$$

$$D_{Buck} = \frac{2 \cdot t_c'}{T_s} = \frac{2 \cdot (T_s - t_c)}{T_s} = 2 \cdot (1 - D_{Boost}) \quad (8)$$

Thus, substituting (5) and (8) in (7) and for $0.5 \leq d_{Boost} < 1$, results in

$$\frac{\overline{v}_o}{V_{in}} = \frac{2 \cdot \left(1 - d_{Boost}(t)\right)}{n \cdot \left(1 - D_{Boost\,\min}\right)} \quad (9)$$

Therefore, based on (3) and (8), the behavior of $d_{Buck}(t)$ can be showed in Figure 11.

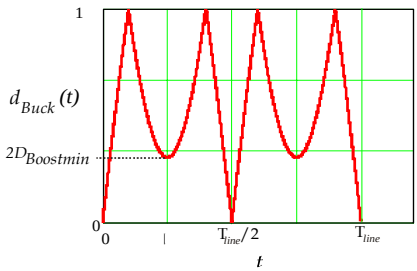

Figure 11 – Behavior of $d_{Buck}(t)$.

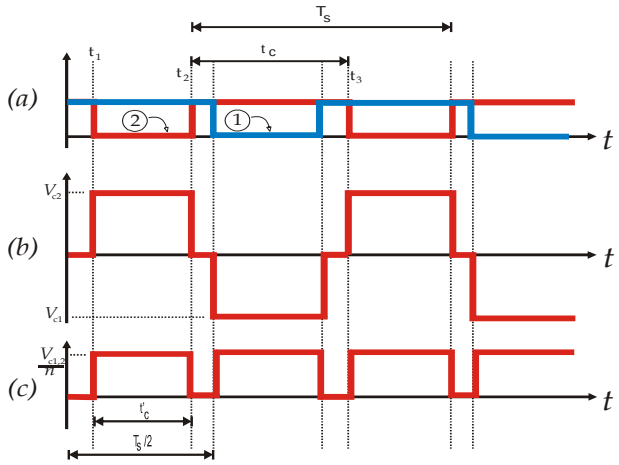

Figure 12 – Waveforms for $0.5 \leq d_{Boost} < 1$. Gating signals of *S1*, (a)1, and *S2*, (a)2; voltage on the terminals of T_1 (v_p), (b), and the voltage applied on output filter (v_s), (d).

3) Steady-State Gain for $D_{Boostmin} \leq d_{Boost} < 1$

Analyzing the equations (6) and (9), it is clear that there are two different steady-state gains. Thus, for one line period, the overall steady-state gain can be calculated as following:

$$\text{With } V_o(D_{Boost\,min}) = \frac{1}{T_{line}} \int_0^{T_{line}} \bar{v}_o(t, D_{Boost\,min}) \cdot dt \,, \quad \text{the}$$

equation (10) is obtained.

$$\frac{n \cdot V_o(D_{Boost\,min})}{2 \cdot V_{in}} = \frac{f\left(D_{Boost\,min}\right)}{1 - D_{Boost\,min}} \tag{10}$$

Where $f(D_{Boostmin})$ is defined by (11), for $D_{Boostmin} \leq 0.5$, and by (12), for $0.5 \leq D_{Boostmin} \leq 1$.

$$f(D_{Boost\,min}) = \frac{2 \cdot \left(1 - D_{Boost\,min}\right)}{\pi} - \frac{4}{\pi}\left\{\left(1 - D_{Boost\,min}\right) \cdot \sqrt{1 - \left(\frac{0.5}{1 - D_{Boost\,min}}\right)^2} - \frac{1}{2} \cdot \left[\frac{\pi}{2} - \sin^{-1}\left(\frac{0.5}{1 - D_{Boost\,min}}\right)\right]\right\} \tag{11}$$

$$f(D_{Boost\,min}) = \frac{2}{\pi} \cdot \left(1 - D_{Boost\,min}\right) \tag{12}$$

Analyzing the graphic of equation (10), showed in Figure 13, it is clear that the regulation of the output voltage for $0.5 \leq D_{Boostmin} \leq 1$ is not possible, since this voltage only depends of the peak input voltage (V_{in}) and the transformer turns ratio (n).

As the control of the input current waveshape depends on the instantaneous value of $d_{Boost}(t)$ and the output voltage can be regulated by $D_{Boostmin}$, it is feasible to transfer power from input to output continuously, i.e., during all line period, and, at the same time, to regulate the output voltage for $0 \leq D_{Boostmin} < 0.5$. By equation (10), it is easily verified that this allowed range of variation for $D_{Boostmin}$ ideally makes universal input voltage applications feasible ($V_{in\,max} / V_{in\,min} = 10/\pi \cong 265/85$).

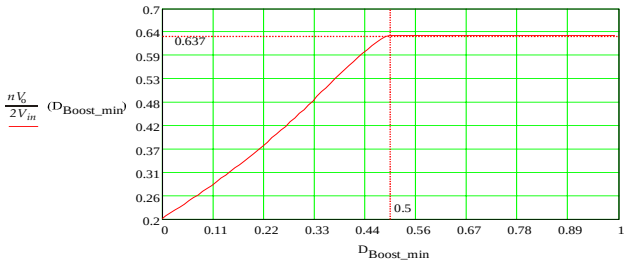

Figure 13 – Graphic of $nV_o / (2V_{in})$.

C. Flux-Reset of T_1 and Minimum Circulating Reactive Energy Conditions

The converter showed in Figure 1 is represented by functional blocks in Figure 14. The Boost cell A is formed by C_1, S_1, S_2 and L_1 and The Boost cell B is formed by C_2, S_3, S_4 and L_2. The high frequency transformer T_1 and its secondary circuit are represented by the "Load" functional block.

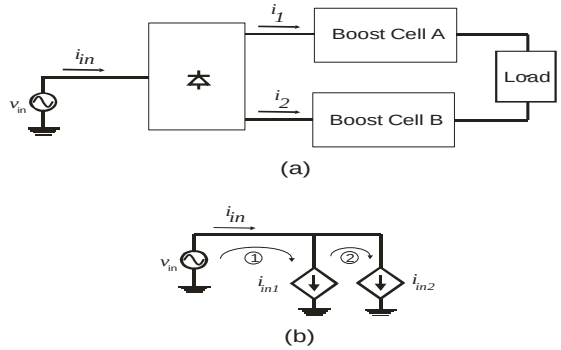

Figure 14 – (a) Representation of converter of Figure 1 by functional blocks. (b) Input port equivalent circuit.

1) Minimum Circulating Reactive Energy Conditions

In Figure 14(b), assuming that i_{in} is in phase and has the same waveshape of v_{in}, no reactive energy can circulate in loop 1. Thus, to guarantee that no reactive energy circulates in loop 2, i.e., between Boost Cell A and Boost Cell B, it is necessary that i_{in1} and i_{in2} be forced to follow, in phase, the waveshape of v_{in}. Consequently, this condition also reduces conduction losses due circulating reactive energy.

One of the possible solutions is proposed in this paper, as showed in Figure 15. It uses two current control loops that make the input current of each Boost Cell (i_{L1} and i_{L2}) to follow, in phase, the waveshape of $|v_{in}|$.

2) Conditions for Flux-Reset of T_1 into Switching Period

To guarantee the magnetic flux-reset of *T1* into switching period, the product volt-second for the first semi-period has to be equals, in module, to the second one. So, based on Figure 10(b), the flux-reset of *T1* is guaranteed since the equation (13) is satisfied.

$$V_{c1} \cdot D_{B\_ef} = V_{c2} \cdot D_{A\_ef} \tag{13}$$

Where, D_{A_ef} and D_{B_ef} are the effective duty ratio of Boost Cell A and Boost Cell B, respectively.

The averaged instantaneous power ($\bar{p}$), i.e., the averaged power within a switching period, delivered by the Boost

Cells A and B, are respectively defined by equations (14) and (15).

$$\overline{p}_1 = V_{c1} \cdot D_{B\_ef} \cdot I_{T_{1p}} \quad (14)$$

$$\overline{p}_2 = V_{c2} \cdot D_{A\_ef} \cdot I_{T_{1p}} \quad (15)$$

Making $\overline{p}_1 = \overline{p}_2$ results on (13). This means that the flux-reset of T_1 can be achieved forcing a balanced load-sharing between Boost Cell A and B. Assuming that the two input current control-loops and Boost Cell's efficiency are identical, the flux-reset of T_1 is achieved within a switching period adopting the same solution showed in Figure 15. However, a DC blocking capacitor should be used to prevent the core saturation of T_1 if, for instance, some difference between the current sensor's gain occur.

III. DESIGN GUIDELINES

The influence of L_d will be considered in this section. It can be represented by a reduction of the effective duty-cycle, ΔD, as showed in (16).

$$\Delta D\left(D_{Boost\,\min\_ef}\right) = \frac{2 \cdot V_o \cdot L_d \cdot f_s \cdot \left(1 - D_{Boost\,\min\_ef}\right)}{n \cdot R_o \cdot V_{in} + 2 \cdot \overline{V}_o \cdot L_d \cdot f_s} \quad (16)$$

So, the minimum duty-cycle for Boost stage is now defined by (17).

$$D_{Boost\,\min} = D_{Boost\,\min\_ef} + \Delta D \quad (17)$$

For variable input applications ($V_{in\min} \le V_{in} \le V_{in\max}$), the reduction of allowed variation for V_{in}, due to influence of L_d, is defined by (18).

$$V_{in\min} = \frac{V_{in\max}}{3.169 - 4.338 \cdot \Delta D_{\max}} \quad (18)$$

A. Transformer Turns Ratio (n)

Using equations (16) and (17), considering $D_{Boost\min}$=0.5, ΔD=$\Delta D_{\max}$ and determining $V_{in\min}$ using (18), for a desired $V_{in\max}$, the parameter n is calculated using (19).

$$n = \frac{V_o \cdot f_s \cdot L_d}{\Delta D_{\max} \cdot V_{in\,\min} \cdot R_o} \quad (19)$$

B. Output filter

1) Output Inductance L_o

Considering the worst case, V_{in} = $V_{in\max}$, L_o can be estimated by:

$$L_o \ge \frac{V_{in\max}}{4 \cdot n \cdot \left(1 - \Delta D(0)\right) \cdot \pi \cdot f_{line} \cdot \Delta i_{Lo}} \cdot k \quad (20)$$

Where:

$$k = \left| \begin{matrix} \frac{a}{2} \cdot \left(\sin(8 \cdot \pi \cdot f_{line} \cdot t_1) - \sin(8 \cdot \pi \cdot f_{line} \cdot t_2)\right) + \\ b \cdot \left(\sin(4 \cdot \pi \cdot f_{line} \cdot t_2) - \sin(4 \cdot \pi \cdot f_{line} \cdot t_1)\right) \end{matrix} \right| \quad (21)$$

$$a = \frac{2}{\pi} \cdot \sin(4 \cdot \theta) - \frac{16}{15\pi} \cdot \gamma \cdot \left(\begin{matrix} 0.5 + 4 \cdot \cos\theta \cdot \sin(4 \cdot \theta) \\ -\sin\theta \cdot \cos(4 \cdot \theta) \end{matrix} \right) \quad (22)$$

$$b = \frac{4}{\pi} \cdot \sin(2 \cdot \theta) - \frac{16}{3\pi} \cdot \gamma \cdot \left(\begin{matrix} 2 \cdot \cos\theta \cdot \sin(2 \cdot \theta) \\ -\sin\theta \cdot \cos(2 \cdot \theta) - 0.5 \end{matrix} \right) \quad (23)$$

$$\gamma = 1 - \frac{2 \cdot V_o \cdot L_d \cdot f_s}{n \cdot R_o \cdot V_{in\max} + 2 \cdot \overline{V}_o \cdot L_d \cdot f_s} \quad (24)$$

$$\theta = \frac{\pi}{2} - \sin^{-1}\left(\frac{0.5}{\gamma}\right) \quad (25)$$

$$t_1 = \frac{1}{4 \cdot \pi \cdot f_{line}} \cdot \left[\pi + \cos\left(-\frac{b}{a} - \frac{\sqrt{4 \cdot b^2 + 2 \cdot a^2}}{2 \cdot a} \right) \right] \quad (26)$$

$$t_2 = \frac{1}{4 \cdot \pi \cdot f_{line}} \cdot \left[\pi - \cos\left(-\frac{b}{a} - \frac{\sqrt{4 \cdot b^2 + 2 \cdot a^2}}{2 \cdot a} \right) \right] \quad (27)$$

2) Output Capacitance C_o

Neglecting the influence of the equivalent series resistance, the capacitance of C_o can be founded using

$$C_o \ge \frac{V_{in\max}}{16 \cdot n \cdot \left(1 - \Delta D(0)\right) \cdot \pi^2 \cdot {f_{line}}^2 \cdot L_o \cdot \Delta v_o} \cdot \delta \quad (28)$$

Where:

$$\delta = \left| b \cdot \left(\cos\left(4 \cdot \pi \cdot f_{line} \cdot t_3\right) - 1\right) - \frac{a}{4} \cdot \left(1 - \cos\left(8 \cdot \pi \cdot f_{line} \cdot t_3\right)\right) \right| \quad (29)$$

$$t_3 = \frac{1}{4 \cdot f_{line}} \quad (30)$$

C. Input Inductance (L) and Bus Capacitance (C_{Bus})

The calculus of L is similar to a conventional interleaved Boost converter and can be founded in the bibliography, as in [5].

$$L \ge \frac{25 \cdot R_o \cdot \eta \cdot V_{C_{Bus}\max} \cdot V_{in\max}}{4 \cdot f_s \cdot \Delta i_{in\%} \cdot {V_o}^2} \quad (31)$$

For the capacitance of C_{Bus}, the minimum hold-up time ($t_{hold\text{-}up}$) criterion was adopted. Thus,

$$C_{Bus} \ge \frac{{V_o}^2 \cdot t_{hold-up}}{R_o \cdot \left[{V_{C_{Bus}\max}}^2 - \left(0.9 \cdot V_{C_{Bus}\max}\right)^2 \right]}. \quad (32)$$

The maximum average voltage applied on C_{Bus} ($\overline{V}_{C_{Bus}\max}$) can be estimated using (33).

$$V_{C_{Bus}\max} = \frac{V_{in\max}}{1 - \frac{2 \cdot V_o \cdot L_d \cdot f_s}{n \cdot R_o \cdot V_{in\max} + 2 \cdot V_o \cdot L_d \cdot f_s}} \quad (33)$$

IV. NUMERICAL SIMULATION

The circuit simulated is showed in Figure 15. The values of the components calculated using the design guidelines previously provided for η=1, Ro=2.3Ω, ΔD_{max}=0.1, V_o=48V, $V_{in\max}$=375V, $\Delta i_{Lo\%} \le 20\%$, $\Delta v_{o\%} \le 5\%$, $\Delta i_{in\%} \le 20\%$, $t_{hold\text{-}up}$= 16.667ms and f_s=50kHz are showed in Table 1. The results of numerical simulation are displayed in Figure 16 and compared with theoretic results in Table 2, confirming the results predicted by previous theoretical analysis.

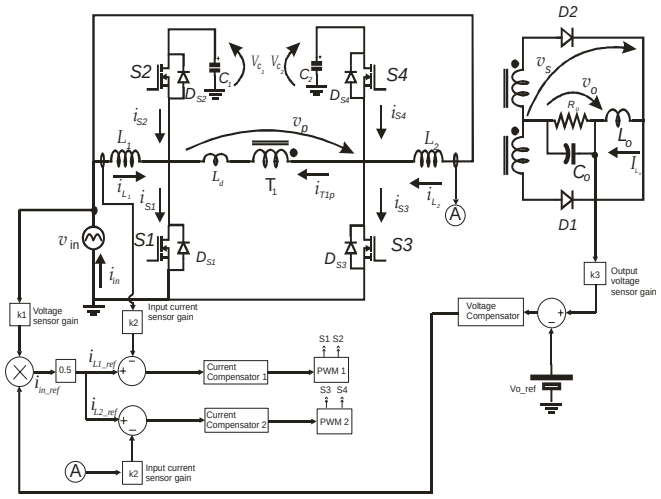

Figure 15 – Circuit simulated.

Table 1
Values of the components calculated using the design guidelines.

Device designation	Value
L_1, L_2	$939\mu H$
C_1, C_2	$545\mu F$
L_o	$33mH$
C_o	$1.4mF$
T_1	n=2.1; L_m=2.45mH and L_d=27μH

Table 2
Simulated and Calculated results.

Parameter	Calculated	Simulated
Δi_{Lo}	4.2 (A)	4.3 (A)
Δv_o	2.4 (V)	3.0 (V)
Δi_{in}	1.07 (A)	0.98 (A)
$V_{C_{Bus}\max}$	398.7 (V)	382 (V)

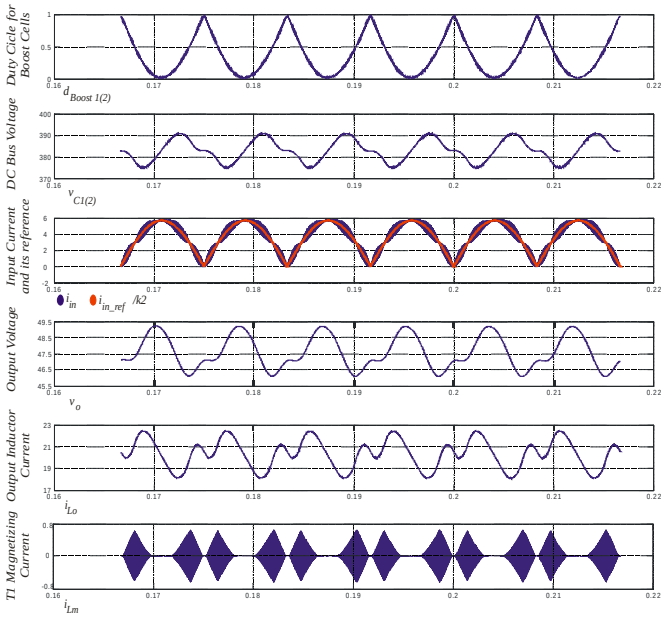

Figure 16 – Key waveforms results of the numerical simulation. From de top: $d_{Boost\ 1(2)}$; $v_{c1(2)}$; $i_{in}(t)$ and $i_{in\_ref}(t)$; $v_o(t)$; $i_{Lo}(t)$ and $i_{Lm}(t)$.

V. CONCLUSION

In this paper, a new steady-state analysis and a design guideline for an AC-DC Single-Stage Full-Bridge Converter Power Factor Corrected with Interleaved Boost Input Type was presented. It was clarified, that is feasible to control the input current, during all line period, and to regulate the output voltage such that the power is transferred during all line period which reduces the output filter size, when compared with solution presented in [1]. Moreover, conditions that guarantee the flux-reset of HFT T_1 and minimum conduction losses, due to circulating reactive energy, were provided.

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