HIGH-POWER-FACTOR HYBRID THREE-PHASE RECTIFIER WITH PROGRAMMABLE INPUT CURRENT THD

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***Abstract* — A digital hysteresis modulation using a FPGA (Field Programmable Gate Array) device and VHDL (Hardware Description Language), applied at a hybrid three-phase rectifier with almost unitary input power factor, composed by parallel SEPIC controlled single-phase rectifiers connected to each leg of a standard 6-pulses uncontrolled diode rectifier, is proposed and analyzed in this paper. The digital control allows a programmable THD (Total Harmonic Distortion) at the input currents, and it makes possible that the power rating of the switching-mode converters, connected in parallel, can be a small fraction of the total average output power, in order to obtain a compact converter, reduced input current THD and almost unitary input power factor. Finally, the proposed digital control, using a FPGA device and VHDL, offers an important flexibility for the associated control technique, in order to obtain a programmable PFC (Power Factor Correction) hybrid three-phase rectifier, in agreement with the international standards (IEC, and IEEE), which impose limits for the THD of the AC (Alternate Current) line input currents.**

***Keywords* - Digital Control, FPGA Device, VHDL Language, Hybrid Rectifier, Active Power-Factor Correction, Hysteresis Modulation.**

I. INTRODUCTION

In the last decade, due to the significant increase of the non-linear loads, including the single-phase and three-phase rectifiers, high values of harmonic distortions in the currents through the AC distribution feeders have been observed, causing significant harmonic distortions in the voltages over the point of common coupling (PCC). In this context, were established international standards such as the IEC 61000-3-2, IEC 61000-3-4, and IEEE 519, in order to impose limits on harmonic current emissions from these equipments [1-2]. Furthermore, considering the necessity to impose restrictions on the harmonic input current content, several researches have been developed passive active strategies/structures, in order to provide high input power factor, and compatible electromagnetic levels for the three-phase rectifier applications. Considering the researches developed in order to combine the advantages of passive and active rectifiers, the "*Hybrid Rectifiers*" were proposed, applied to medium and high power levels. Hybrid rectifiers are generated through special connections of one passive rectifier with PWM active rectifiers. The passive rectifier operates in low frequency, and transfers the most part of the total active power to the load. On the other hand, the PWM active rectifier transfers only a small fraction of the total active output power, and operates in high frequency. The most important advantage of these structures is that they combine the robustness and efficiency of the passive and active rectifiers, respectively, with the imposition of an input current with reduced THD, through the appropriate control of the PWM active rectifiers [3-5]. Therefore, hybrid rectifiers, in a general analysis, behave as controlled current sources, using a very simple strategy. Thus, considering the proposed structure shown in Fig. 1 [5], imposing a special reference current to the SEPIC converters so that the driven currents by them, when added with the driven currents by the standard 6-pulses diode rectifier, will result in a programmable input current waveform, with low harmonic distortion as desired and designed, in order to comply with the standards. So, manipulating the waveform of the reference current of each SEPIC converter, it is possible to obtain an input current with a shape of 12, 18, 24-pulses or more, and also to obtain an approximately sinusoidal input current, resulting in an almost unitary input power factor. Nevertheless, considering the proposed rectifier, shown in Fig. 1, operating with an input current of "q.6±1" pulses [6], depending on the index "q" and processed output power values, the harmonic content may not obey the limits imposed by international standards, for example the IEC61000-3-4. Furthermore, it was proposed by the authors [5] an analogical control technique that results in complex analogical circuitry, hindering the imposition of a sinusoidal input current and consequently not allowing the appropriate control of the THD at the input currents. Thus, in order to obey fully the limits imposed by international standards IEC/IEEE, it is proposed a modified digital control technique in this paper, using hysteresis modulation, offering flexibility to the implemented circuitry, that imposes the input current of the controlled converters (for example, $i_{a2}(\omega.t)$), resulting in a almost unitary power factor and small fraction of the total active power processed by controlled rectifier, allowing programmable line input currents THD. It should be noticed that, in order to implement the proposed digital control, it is necessary to make sampling and the digital processing of several signals of the hybrid three-phase rectifier. In this context, the proposed digital control uses a FPGA device and VHDL language, due to its characteristics such as flexibility and concurrent processing, allowing to perform all the procedures of control in several simultaneous operations. Additionally, the use of hardware description language results in reduction of the time to design and to redesign and for implementation the control technique. Furthermore, the required logic must be optimized even using FPGA devices, in order to limit the

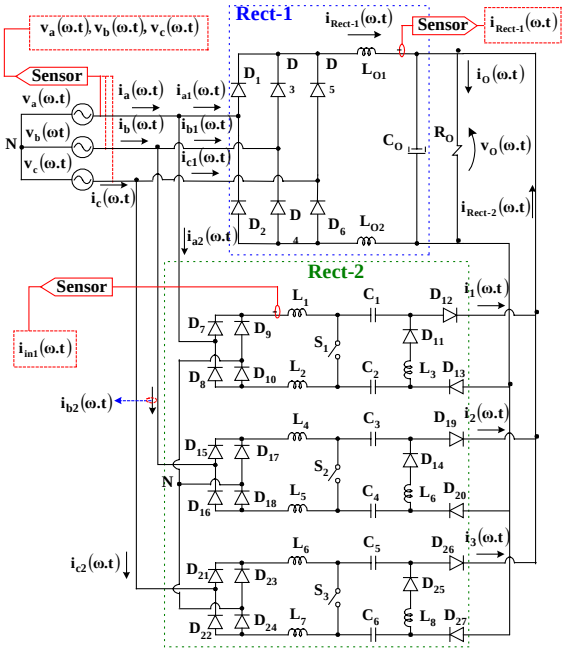


Fig. 1. Hybrid Three-Phase Rectifier with High Input Power Factor.

occupation of silicon area of FPGA devices, and to improve the performance of control [7].

II. THEORETICAL ANALYSIS

In order to simplify the analysis, it will be considered a three-phase sinusoidal balanced input voltage system. Thus, it will be discussed in this paper just the control of the input current $i_a(\omega.t)$, which belongs to phase "a", as shown in Fig. 1. The main goal of the analysis presented in this section is to establish a relation between the THD (Total Harmonic Distortion) imposed to line input currents, with practically sinusoidal waveforms, as shown in Fig. 2, and the total input and output powers processed by the active and passive rectifiers. According to Fig. 2, the input current of the active rectifier, $i_{a2}(\omega.t)$, follows a reference current generated by $i_{sin}(\omega.t)$-$i_{a1}(\omega.t)$. The current $i_{sin}(\omega.t)$, given by equation (1), is an imposed auxiliary sinusoidal current. It should be noticed that, the shape of $i_a(\omega.t)$ depends on a constant relation between peak values of the currents $i_{a1}(\omega.t)$ and $i_{sin}(\omega.t)$, represented through the parameter "K" according to equation (2).

$$I_{sin}(\omega.t) = K.I_{Rect\text{-}1}.sin(\omega.t) \quad (1)$$

$$K = \frac{I_m}{I_{Rect\text{-}1}} \quad (2)$$

Where:

I_m - Peak value of auxiliary sinusoidal current $i_{sin}(\omega.t)$.
$I_{Rect\text{-}1}$ - Peak value of current $i_{a1}(\omega.t)$ (equal to average value of output current of the Rect-1).

The discontinuity of $i_{a2}(\omega.t)$, as shown in Fig. 2, occurs due to the unidirectionality of the proposed hybrid three-phase rectifier. Therefore, the time interval $\omega.\Delta t$ is given by equation (3).

$$\omega.\Delta t(K) = \begin{cases} asin\left(\frac{1}{K}\right) - \frac{\pi}{6}, & 1 \le K \le 2 \\ 0, & K > 2 \end{cases} \quad (3)$$

It is interesting to observe that, increasing the value of the parameter "K", it will result in a reduction of the THD value of the line input current $i_a(\omega.t)$, until it reaches THD=0, when K=2. However, it increases the processed power by the active rectifier (Rect-2) and reduces the overall efficiency of the hybrid rectifier. Thus, following, it will be discussed the analysis performed by [8] to find a value of "K", through the curves shown in Figs. 3 and 4, that provides the minimum power processed by the active rectifier, and the maximum THD value allowed by the international standards.

It should be noticed that, in order to obtain the rms value of related input current, the value of parameter "K" must be specified. Thus, selecting a desirable THD value for the line input current, according to Fig. 3, a correspondent value of "K" is obtained. In addition, an important parameter used to design the proposed hybrid rectifier is the relation between the average value of the output current for each rectifier, uncontrolled and controlled, and the overall average value of

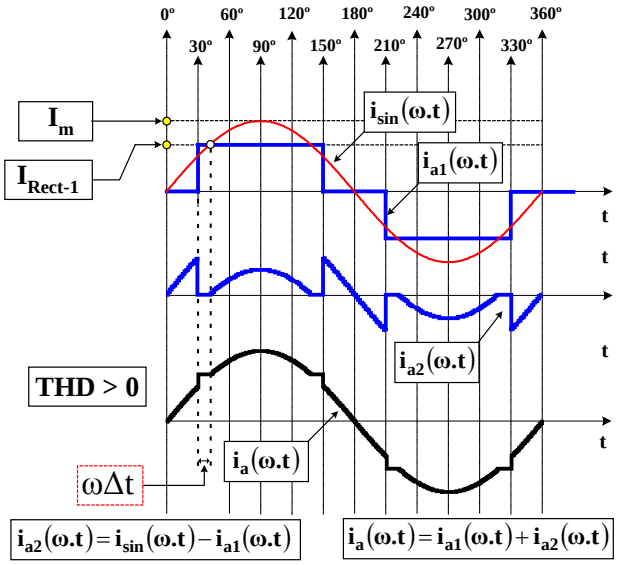


Fig. 2. Theoretical current waveforms, regarding phase "a", of the hybrid three-phase rectifier, operating with almost unitary input power factor.

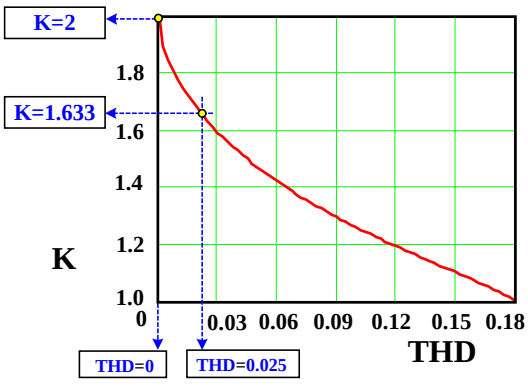


Fig. 3. Parameter "K" as a function of line input current THD for the hybrid three-phase rectifier.

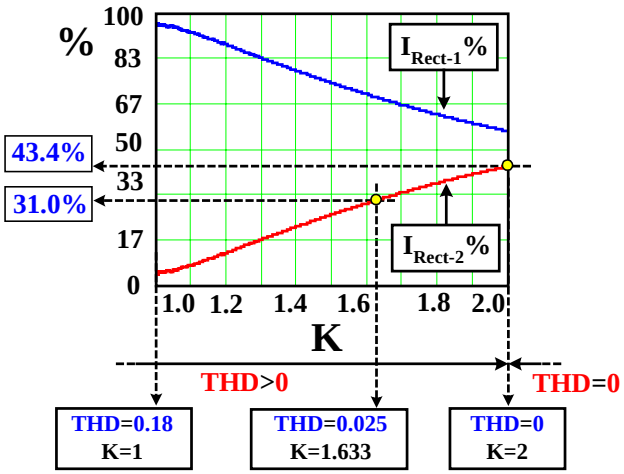


Fig. 4. Fractions of the average output currents I_{Rect-1} [%] and I_{Rect-2} [%], in relation to the overall load output current, as a function of parameter "K".

the load output current. In this context, Fig. 4 shows the fraction of the overall average load output current processed by passive rectifier (I_{Rect-1} [%]), and active rectifier (I_{Rect-2} [%]), as a function of parameter "K". Fig. 3 and 4 show that for a line input current THD smaller than 3%, the value of the parameter "K" increases quickly, increasing also the power processed rate by the active rectifier. Therefore, a nominal operation point with THD larger than 3% must be considered in the design, in order to reduce the relation I_{Rect-2} [%] for the switching-mode converters. The definitive choice of the point of operation will impose simulation verifications, in order to analyze if the values of the line input current harmonic components are in agreement with the limits imposed by the standards (such as IEC 61000-3-2, or, IEC 61000-3-4, or, IEEE 519).

III. PROPOSED DIGITAL CONTROL

The proposed digital control uses a Xilinx FPGA device (Spartan 2e) and VHDL language in order to obtain the control signals to the SEPIC rectifiers. In this context, in order to compose the proposed control, it is necessary to make sampling of the input current $i_{in1}(\omega.t)$ of the $SEPIC_1$ converter, and the output current $i_{Rect-1}(\omega.t)$ of the standard 6-pulses diode rectifier, as shown in Fig. 1, and additionally, to sample the input current $i_{a1}(\omega.t)$ and input voltage $v_a(\omega.t)$ in the phase "a". The basic idea of this control is that the current $i_{in1}(\omega.t)$ follows an imposed reference of current, digitally generated. Thus, the current $i_{a2}(\omega.t)$, when added to $i_{a1}(\omega.t)$, will result in a line input current $i_a(\omega.t)$ with the same theoretical waveform, as shown in Fig. 2. To operate the hybrid rectifier with almost unitary input power factor, it is digitally generated a reference of current $S_{ignal\_Ref\_sin}(n)$, as shown in Fig. 5, to impose the shape of the input current, $i_{a2}(\omega.t)$ according to Fig. 2. Therefore, in order to compose the control logic showed in Fig. 5, it will be necessary two auxiliary logical signals, $C_{ontrol\_Isin}(n)$ and $C_{ontrol\_Ia1}(n)$. These auxiliary signals are generated through an additional auxiliary logical signal $I_{a1\_sensor}(n)$ combined with logical counters (VHDL logic), as shown in Fig. 6. The signal $I_{a1\_sensor}(n)$, given by an analogical sensor, receive logical signal "1" if $i_{a1}(\omega.t)=0$, otherwise $I_{a1\_sensor}(n)$ receive logical signal "0". The width of the logical signals, $C_{ontrol\_Isin}(n)$ and $C_{ontrol\_Ia1}(n)$, depends on the time interval of discontinuity "$\omega.\Delta t(K)$", calculated by equation (3). Thus, according to Fig. 6, the signal $C_{ontrol\_Ia1}(n)$ will receive logical signal "1" if $\{30°+\omega.\Delta t(K)\}<\omega.t<\{150°-\omega.\Delta t(K)\}$ or if $\{210°+\omega.\Delta t(K)\}<\omega.t<\{330°-\omega.\Delta t(K)\}$, otherwise $C_{ontrol\_Ia1}(n)$ will receive logical signal "0".

Furthermore, the signal $C_{ontrol\_Isin}(n)$ will receive logical signal "0" if $30°<\omega.t<\{30°+\omega.\Delta t(K)\}$, or if $\{150°-\omega.\Delta t(K)\}<\omega.t<150°$, or if $210°<\omega.t<\{210°+\omega.\Delta t(K)\}$, or if $\{330°-\omega.\Delta t(K)\}<\omega.t<330°$, otherwise it will receive logical signal "1". In Fig. 5, the input signals are: Control signals, $C_{ontrol\_Ia1}(n)$, $C_{ontrol\_Isin}(n)$ and $V_{a\_sensor}(n)$, and the output current $I_{Rect-1}(n)$. The purpose of the signal $C_{ontrol\_Ia1}(n)$ is to generate a digital current $I_{a1\_\omega\Delta t}(n)$ through the following logic selection. If $C_{ontrol\_Ia1}(n)$="1", $I_{a1\_\omega\Delta t}(n)$ becomes $I_{Rect-1}(n)$, otherwise if $C_{ontrol\_Ia1}(n)$="0", $I_{a1\_\omega\Delta t}(n)$ becomes "00000000". The signal $I_{sin\_unit}(n)$ is a rectified sinusoidal current with unitary amplitude, digitally generated, and synchronized with AC grid by the signal $V_{a\_sensor}(n)$. The signal $V_{a\_sensor}(n)$, given by an analogical sensor, receive logical signal "0" if $v_a(\omega.t)>0$, otherwise $V_{a\_sensor}(n)$ receive logical signal "1". Thus, multiplying the average value of output current $I_{Rect-1}(n)$ by the parameter "K" and $I_{sin\_unit}(n)$, it will result in a rectified sinusoidal signal $I_{sin}(n)$ with amplitude $K.I_{Rect-1}(n)$. The signal $C_{ontrol\_Isin}(n)$ is used to obtain an interval of discontinuity "$\omega.\Delta t(K)$" in the signal $I_{sin}(n)$, resulting in the signal $I_{sin\_\omega\Delta t}(n)$, which is obtained by the following logic selection: If $C_{ontrol\_sin}(n)$="1", $I_{sin\_\omega\Delta t}(n)$ becomes $I_{sin}(n)$, otherwise if $C_{ontrol\_sin}(n)$="0", $I_{sin\_\omega\Delta t}(n)$ becomes "00000000". This way, the control for the line input current THD is achieved only with a desirable specification of the parameter "K", according to theoretical analysis previously discussed. Finally, the reference of current $S_{ignal\_Ref\_sin}(n)$ to the $SEPIC_1$ rectifier is generated by $I_{sin\_\omega\Delta t}(n)-I_{a1\_\omega\Delta t}(n)$, as shown in Fig. 5.

A. Digital Hysteresis Modulation

Digital hysteresis modulation has been widely applied in its standard form, where the switch turns on and turns off when the sampled current differs from its reference, considering a specification for the threshold. This solution, although very simple, has a major drawback due to the frequency jitter associated to the sampling process, causing spectrum components even in the low-frequency range [9]. In this case, the switch turn-on and the switch turn-off not provide that the current commutates exactly at the hysteresis band, resulting an additional variations in the switching frequency. Considering that the turn-on and turn-off times are always a multiple of the sampling period, it can be needed unpredictable switching frequency in order to maintain the desired instantaneous average value of controlled current [9]. The authors in [9] investigated a digital hysteresis modulation based on switching-time prediction, which theoretically avoids frequency jitter and ensures a dynamic performance similar to that obtainable with an analog hysteresis modulation. Besides, it was used a

simple frequency-stabilization algorithm, maintaining the advantages of the PWM technique [10].

Fig. 7 and 8 shows the proposed methodology using the hysteresis modulation to generate the pulses to SEPIC$_1$ rectifier, following partially the concepts applied in [9]. In the proposed hysteresis modulation, the upper reference is eliminated according to Fig. 7. The control of the ripple and frequency range of the input current $I_{in1}(n)$ of the SEPIC$_1$ rectifier can be performed by two distinct forms. The control law of modulation in both cases is given by the states E_0, E_1, E_2, E_3 and E_4, detailed in Fig. 8.

1) Constant turn-on time (t_{on}) and variable turn-off time (t_{off}) and operation frequency: The time t_{on} occurs during the state E_0 and the P_{ulse_PWM} receive logical signal "1". This time interval is controlled by a down-up counter, which determines exactly the instant of the transition to the state E_1, avoiding errors of the comparator associated to sampling process, previously discussed. In the states E_1 and E_3 occurs the switching transitions turn-on to turn-off (P_{ulse_PWM} receive logical signal "0") and turn-off to turn-on (P_{ulse_PWM} receive logical signal "1"), respectively. In these states, also there is not actuation of the comparator, thus, the time intervals are controlled by down-up counters, aiming for avoid an unpredictable operation of the control due the presence of switching noises. The time t_{off} occurs during the state E_2. This time interval is controlled by the comparator within the following logic: If $I_{in1}(n) \geq S_{ignal\_Ref\_sin}(n)$, P_{ulse_PWM} will receive logical signal "0", otherwise, if $I_{in1}(n) < S_{ignal\_Ref\_sin}(n)$), P_{ulse_PWM} will receive logical signal "1" and state change to E_3. Finally, the state E_4 has the function of verify if the signal $S_{ignal\_Ref\_sin}(n)$ changed its value during the state E_3, within the following logic: If $I_{in1}(n) \geq S_{ignal\_Ref\_sin}(n)$, the state change to E_0, otherwise, if $I_{in1}(n) < S_{ignal\_Ref\_sin}(n)$), the state E_3 is maintained. The P_{ulse_PWM} receive only logical signal "1" in the state E_4. Thus, the inherent dynamic performance of the analogic hysteresis modulation is perfectly guaranteed.

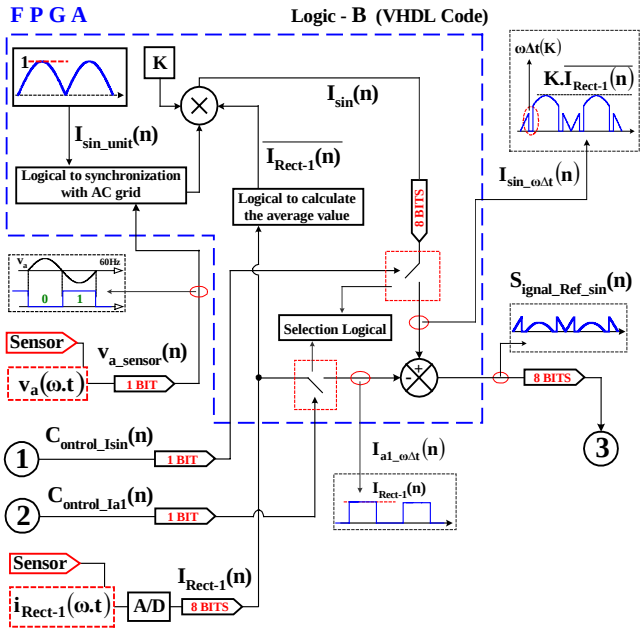


Fig. 5. Details of the logic control to generate the reference current for the SEPIC rectifiers.

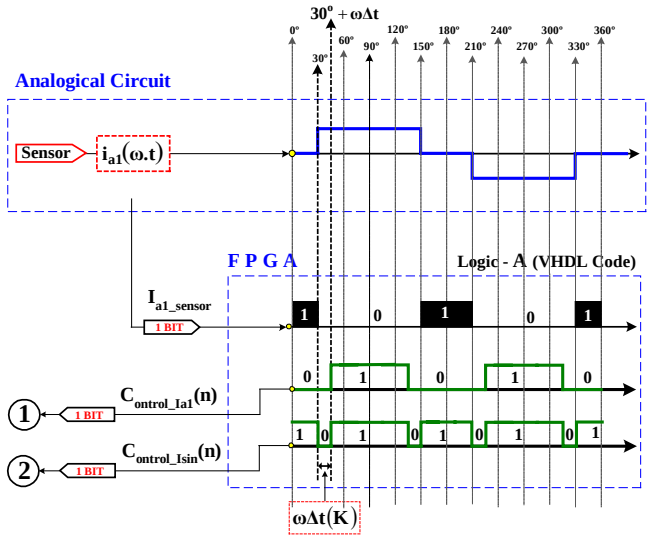


Fig. 6. Auxiliary control for the reference current, in order to generate the pulses to SEPIC rectifier.

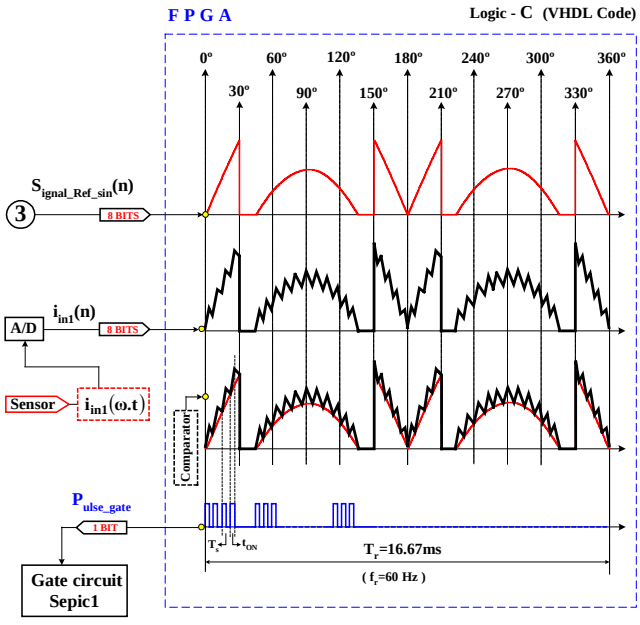


Fig. 7. Methodology to generate the pulses, in order to control the SEPIC$_1$ rectifier.

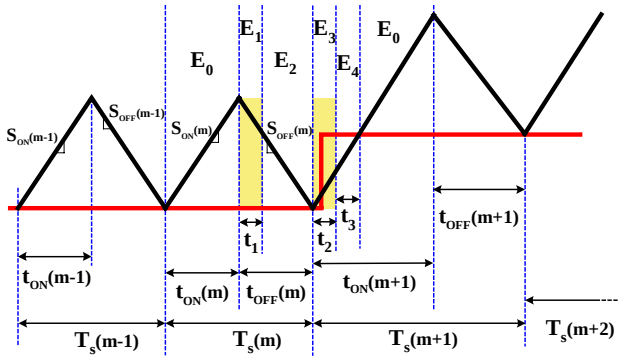


Fig. 8. Details of the methodology to generate the pulses, in order to control the SEPIC$_1$ rectifier.

2) Constant operation frequency and variable turn-on time (t_{on}) and turn-off time (t_{off}): In this operation form is maintained the same control law applied to case 1, previously discussed. Additionally, based on switching-time prediction, the time t_{on} will be calculated to each transition of the state E_2 to E_3, according to equation (4).

$$t_{on}(m) = T_s(m-1) - t_{off}(m-1) \qquad (4)$$

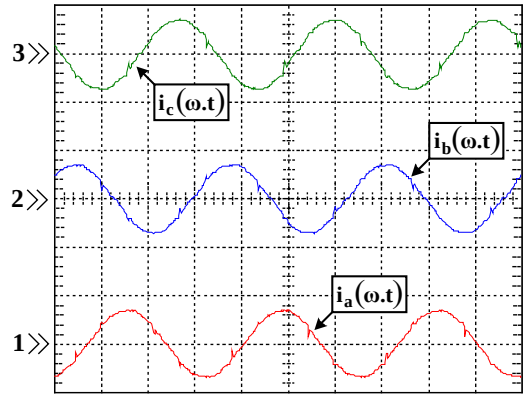
IV. EXPERIMENTAL RESULTS

Considering the theoretical analysis discussed in sections II and III, applied to proposed digital control, a 3.0kW hybrid three-phase rectifier prototype was built, according to circuit depicted in Fig.1. The input and output data, including the designed parameters and components used in the prototype are shown in Table I. The waveforms shown in Figs. 9, 10 and 11, constitute preliminary experimental results of the phases "a", "b" and "c" of the hybrid three-phase rectifier operating near to 33% of load (P_O=1.0kW). Analyzing the results, showed in Fig. 9, through the Tektronix Wavestar software, one can confirm a THD=4.48% to the line input current $i_a(\omega.t)$, THD=4.11% to the line input current $i_b(\omega.t)$ and THD=4.22% to the line input current $i_c(\omega.t)$, given by harmonic spectrum, shown in Figs. 12, 13 and 14, respectively. Therefore, considering the processed line input currents values (i_{arms}=2.62A, i_{brms}=2.70A i_{crms}=2.71A) by the implemented prototype, it can be concluded that the Standard IEC 61000-3-4 is practically obeyed, except to harmonic orders 19, 25, 29 and 31, being a good preliminary results. However, aiming to the application at high power (i_{arms}>16 A), and to comply with the limits imposed by Standard IEC 61000-3-4, in the future version of this paper, the previously commented results will be improved imposing an appropriate synchronism between the uncontrolled $\{i_{a1}(\omega.t)\}$ and controlled $\{i_{a2}(\omega.t)\}$ currents, in order to compose the desired waveform to line input current $i_a(\omega.t)$, in according to Fig. 2, shown in section II.

TABLE I
Parameters of the Hybrid Three-Phase Rectifiers

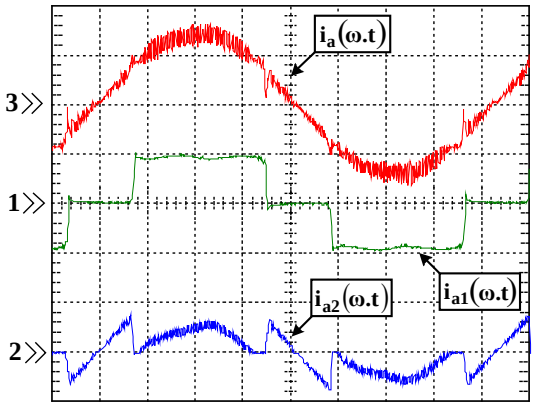
Input - Output Requirements	
Parameter	**Value**
Vin_phase(rms)	70 V
V_{O_DC}	162 V
P_O	3.0 kW
fs maximum	60 kHz
fs minimum	28 kHz

Circuit's Parameters	
Parameter	**Value**
$S_{1,2,3}$	SPW11N60S5
$D_{11,12,13,14,19}$	RHRP860
$D_{20,25,26,27}$	RHRP860
$L_{1,2,4,5,6,7}$	2.5mH – EE55/21
$L_{3,6,8}$	5mH – EE55/21
L_{O1} and L_{O2}	13mH
Co	680uF



5A/div; 5ms/div

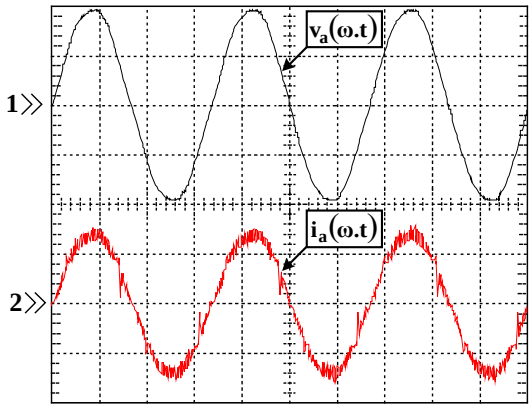
Fig. 9. Input voltage and line input current waveforms, in phases "a", "b" and "c" for the proposed hybrid three-phase rectifier.



5A/div; 2ms/div

Fig. 10. Details of the line input current waveform, in the "phase a", for the proposed hybrid three-phase rectifier.

In Fig. 11, are depicted the phase input voltage $\{v_a(\omega.t)\}$ and line input current $\{i_a(\omega.t)\}$ waveforms, with phase-shift between its fundamental components of 1.15^O. It is important to emphasize that it was verified to the input voltage $v_a(\omega.t)$ a THD=2.52%, by the Tektronix Wavestar software, due to existent harmonic content in the AC grid. Nevertheless, it has caused no problem to operation of the implemented prototype, resulting an almost unitary power factor (PF=0.98).



50V/div; 5A/div; 5ms/div

Fig. 11. Input voltage and line input current waveforms, in "phase a", for the proposed hybrid three-phase rectifier.

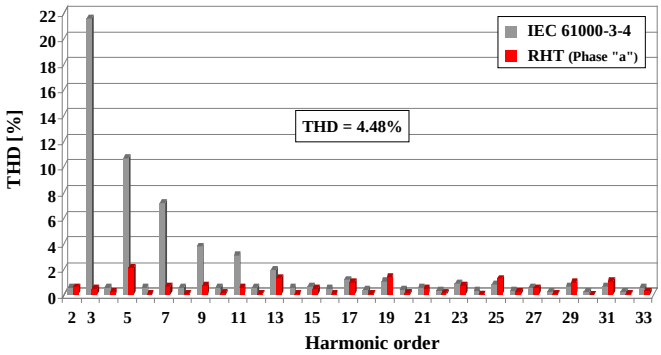


Fig. 12. Frequency spectrum of the line input current $i_a(\omega.t)$, at 33% of load. (% of the fundamental component).

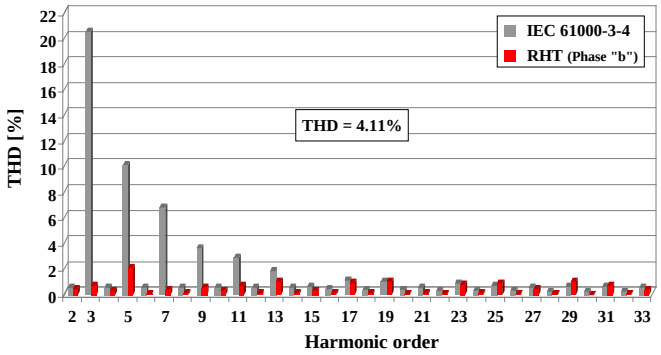


Fig. 13. Frequency spectrum of the line input current $i_b(\omega.t)$, at 33% of load. (% of the fundamental component).

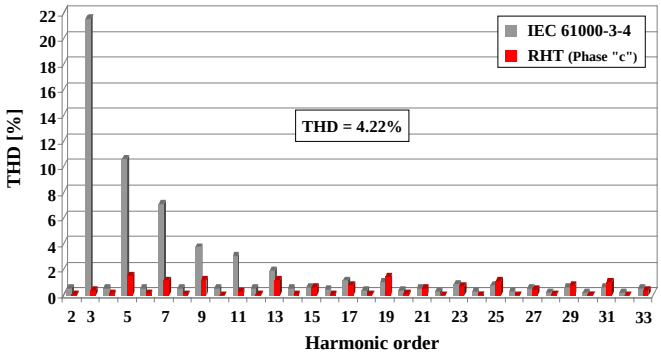


Fig. 14. Frequency spectrum of the line input current $i_c(\omega.t)$, at 33% of load. (% of the fundamental component).

V. CONCLUSIONS

This paper presented the analysis, and preliminary experimental results of the proposed digital control applied at a hybrid three-phase rectifier, capable to impose the line input current THD, resulting in high input power factor for the proposed converter. The digital control using hysteresis modulation was implemented through a FPGA device, using VHDL language. It was verified through analyzed experimental results that the maximum line input current THD was sustained in 4.48%, resulting an almost unitary power factor (PF=0.98), in phase "a". Through the input currents decomposition of the hybrid rectifier, in Fourier series, and using elementary mathematical relations of own circuit, it was defined a design methodology that establishes a relationship between the THD (Total Harmonic Distortion) imposed to line input currents, and the total input and output powers processed by active and passive rectifiers. Therefore, the most important aim of the discussed theoretical analysis was to obtain an maximum THD value to the input currents, whose the corresponding harmonic content is according to the limits imposed by international standards, and consequently a minimum power value processed by active rectifier. Among the advantages of the proposed hybrid three-phase rectifier, are appointed the economic benefits of this topology, which are extremely viable to medium power installations, due to its efficiency and performance. The total active power processed by the switching-mode SEPIC rectifiers is a small fraction of the nominal output active power. The parallel PWM rectifiers, formed by SEPIC converters, operate in continuous conduction mode and PWM modulation, offering reduced volume and weight to the structure. Additionally, using the proposed digital control technique, implemented in a FPGA device, allows an important flexibility and facilities to impose a desirable and specified waveform in the input currents, including sinusoidal waveforms, through VHDL code, performing a true programmable line input current TDH for the proposed hybrid three-phase rectifier.

ACKNOWLEDGMENT

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