A MPPT ALGORITHM IMPLEMENTATION USING FPGA FOR AN EXPERIMENTAL PV SYSTEM

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***Abstract* – This paper presents a MPPT (maximum power point tracking) algorithm implemented with a FPGA (field programmable gate array) for PV (Photo-Voltaic) generation systems. From the many MPPT methodologies found in the literature, the simple P&O (perturb-and-observe) algorithm was chosen and applied in a prototype for validation. The fast prototyping environment provided by the FPGA indicates that such digital devices can be useful not only for this but for other power electronics applications including power electronics education .**

***Keywords* – FPGA (field programmable gate array), MPPT (maximum power point tracking), PV (Photo-Voltaic) generation systems, power electronics education.**

I. INTRODUCTION

This paper presents a MPPT (maximum power point tracking) algorithm implemented with a FPGA (field programmable gate array) for PV (photo-voltaic) generation systems application. From the many MPPT methodologies found in the literature, the simple P&O (perturb-and-observe) algorithm was chosen and applied in a prototype for validation. The fast prototyping environment provided by the FPGA indicates that such digital devices can be useful not only for this but for other power electronics applications including power electronics education.

II. SCOPE OF THE PROBLEM

The application of PV generation systems is increasing due to environmental issues, as well as for application in remote areas not served by electrical utility companies. The intrinsic low efficiency of the most popular poly-crystalline silicon applied in solar cells is lower than 22% even with light intensificators[1]. Other losses are to be considered, like 10% to 15% due to absorption by the ozone layer, water vapor, and carbon dioxide present in the atmosphere. Some 30% to 35% are reflected by atmosphere, which generates the terrestrial brightness. Earth rotation and its axial tilt also contribute for the yearly climate changes and varying insolation levels of the four climate seasons of the year [2]. These global low efficiencies associated to the high initial costs of PV generation systems (and their associated power electronics and battery-based energy storage systems) demand that such systems must operate at their maximum levels of efficiency. The solar cell behavior is also highly dependent on the light irradiation and temperature conditions, as seen in figure 1. The best operation point is in the MPP (maximum power point), which of course changes with temperature and irradiance. Thus, there is the need of a way to track the point of maximum delivered power of the cell.

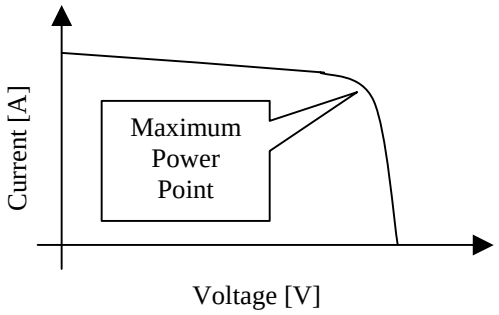

Fig. 1. Characteristic voltage-current curve (IV curve) of a typical solar cell and its maximum power point (MPP), given at a determined level of irradiance and temperature. Curve not in scale.

Figure 2 also shows the output current as a function of the delivered power, put in the same IV curve of figure 1 for the sake of comparison.

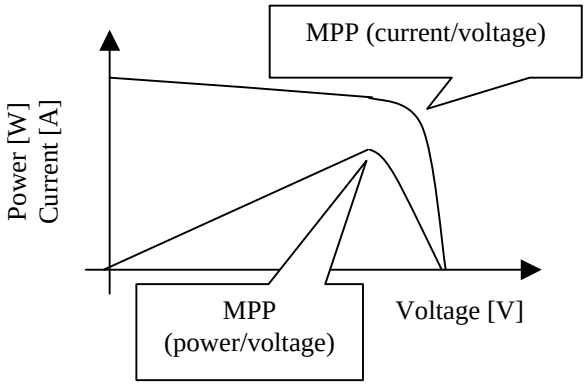

Fig. 2. Characteristic voltage-current curve (IV curve) and power-voltage curve (PV curve) of a typical solar cell and their respective maximum power points (MPP), given at a determined level of irradiance and temperature. Curves not in scale.

Because of the given reasons, the use of a MPPT (maximum power point tracking) control algorithm and associated power electronic system is almost always necessary in a PV generation system.

III. MPPT ALGORITHMS

Based on reference [3], some MPPT algorithms can be described:

1) Perturb and observe (P&O):

In this algorithm, the operating voltage is perturbed by a small amount ΔV and the resulting power difference ΔP is calculated. If the resulting ΔP is positive, successive increases of ΔV are made until the calculated ΔP results negative, showing that the MPP was surpassed. Returning one ΔV leaves the system (almost) at the MPP.

This is one of the most popular MPPT algorithms, because of its easy implementation and simplicity. However, it does not operate exactly on the MPP, but instead oscillates around it, with an error depending on the amount of measurable ΔP and the adopted ΔV value. Also, if the irradiance decreases, the power/voltage MPP characteristic curve flattens, and for a given ΔV the associated ΔP could be very small, to a point that the algorithm could loose the track of the MPP. For the same reasons, rapidly changing levels of irradiance can turn the operation erratic. Improvements can be done, such as the use of variable ΔV (and detected ΔP) around the MPP, as well as the reduction of the ratio of ΔV perturbations if ΔP changes its signal repeatedly, showing that the system is close to the MPP.

2) Incremental conductance (IC)

The IC algorithm differentiates the PV output power with respect to the voltage and sets the result equal to zero.

$$\frac{dP}{dV} = \frac{d(VI)}{dV} = I + V\frac{dI}{dV} = 0 \qquad (1)$$

Rearrange of (1) gives (2):

$$-\frac{I}{V} = \frac{dI}{dV} \quad \left(\frac{dP}{dV} = 0\right) \qquad (2)$$

Equation (2) shows that at the MPP the instantaneous conductance (left side of (2)) is numerically equal to the incremental conductance (right side of (2)) but with opposed signal. A set of equations can determine the direction of the power variation according to the voltage variation:

$$-\frac{I}{V} < \frac{dI}{dV} \quad \left(\frac{dP}{dV} > 0\right) \qquad (3)$$

$$-\frac{I}{V} > \frac{dI}{dV} \quad \left(\frac{dP}{dV} < 0\right) \qquad (4)$$

In (3) the operating point is at the left side of the MPP of the PV curve (figure 2), thus the operating voltage must be increased. In (4) the operating point is at the right side of the PV curve, and the voltage is to be decreased.

3) Parasitic capacitance (PC)

This algorithm is similar to the IC algorithm, but includes the effect of the parasitic capacitance of the PN junctions of the solar cells, thus adding the storage charges on the junctions.

4) Constant Voltage (CV)

This algorithm is based on the approximately constant IV curve behavior from the open circuit point (I=0). The open circuit voltage V_{OC} is measured and the MPP voltage V_{MPP} is taken from equation (5):

$$\frac{V_{MPP}}{V_{OC}} \cong K < 1 \qquad (5)$$

The value of K is between 0.7-0.8 and changes with the temperature and irradiance, making this algorithm poorly efficient if K were not dynamically compensated.

IV. PROTOTYPE IMPLEMENTATION

1) Power converter

For the prototype implementation, the DC/DC converter applied was the conventional boost converter with hard switching. The switch is the MOSFET IRF250 (V_{DSS}*=200V, I_D=30A, $R_{DS(ON)}$=0.085 Ω*) and the diode is the FEP30GP (I_F*=30A, V_{RRM}=400V*).200. The inductor is *L=2.4mH@6A*, output capacitor is *C=560µF@250V*. Switching frequency is *fs=50kHz*.

2) Control hardware

FPGA: a Terasic Technologies TREX C1 Multimedia Development Kit [4] was used as development environment. It has an Altera Cyclone EP1C6Q240C8 FPGA, 8MByte SDRAM (*1M x 4 x 16*), two-40 pin expansion slots, as well as 4-bit DIP switches, eight schmitt-trigger de-bounced push buttons, 4-bit 7-SEG display module etc. It was decided to apply a FPGA platform because of its versatility and the possibility of modularizing the program, facilitating the simulation, debugging and modifications. These characteristics are very attractive in a education environment (undergraduate and graduate) because of the relatively smooth learning curve.

AD converters: The AD7819 (*200 kSBS, 8-bit*) were chosen because of their 200 kSPS capability, which allows four samples for switching period. This apparent oversampling capability simplifies digital filtering of acquired voltage and current, by weighted measurement of the samples.

Figure 3 shows a simplified block diagram of the implemented control hardware.

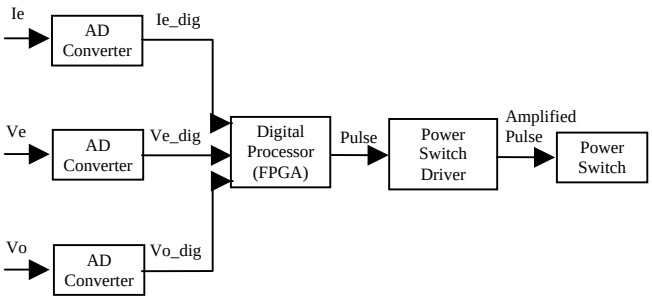

Fig. 3: Control hardware diagram. *Ie* and *Ve* are boost converter current and voltage measurements, and *Vo* is the converter output voltage measurement.

3) System functional overview

The adopted MPPT algorithm is the P&O because of its easy implementation. The FPGA generates discrete switching periods, from 0µs (0% duty-cycle) to 18µs (90% duty-cycle) with 1 µs resolution. DC/DC converter input voltage (*Ve*) and current (*Ie*) (from the output of the PV generator) as well as DC/DC converter output (*Vo*) are measured by using resistive shunts and acquired at 200kSPS rate, and filtered by calculating the mean value each four

samples. The switching instants are displaced from the acquisition ones in order to avoid acquiring switching noise.

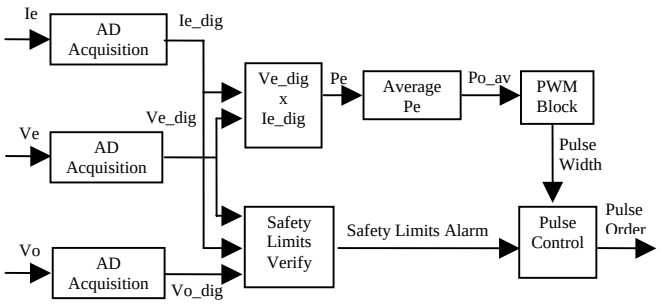

Fig. 4: Control software diagram. *Ie* and *Ve* are boost converter current and voltage measurements, and *Vo* is the converter output voltage measurement.

From figure 4, the acquired values are verified in order to keep the system within its safety operation area, with limits imposed to both output voltage *Vo* and input power *Pe*. Such limits depend on the rated values of the solar cell array and the system load.

V. EXPERIMENTAL RESULTS

System experimental measurements used two sources:

- Voltage source (*20V*) with series resistance (*22Ω*)
- Solar cell array, rated:
  - - *Voc* = 21V (open circuit)
  - - *Isc* = 0,62A (short-circuit)
  - - *Vmp* = 17V (maximum power voltage)
  - - *Imp* = 0,57A (maximum power current)
  - - *Pmp* = 10W (MPP)

1) Voltage source (20V) with series resistance (22Ω)

The purpose of this test was to demonstrate the correct functioning of the control and power converter with a synthetic source. The voltage source in series with the resistance allows a variable input voltage according to the input current. It does no emulate correctly a solar cell, but was of easy implementation for these preliminary tests. Table 1 shows some initial experimental results, and figures 5 to 8 show some waveforms of the power converter.

TABLE I
Results with voltage source (20V) connected to a series resistance (22Ω) feeding a resistive load

Vin [V]	Iin [A]	Pin [W]	Vout (V)	Iout [A]	Pout [W]	Pulse width [µs]	Load [Ω]	Efficiency [%]
11,2	0,42	4,704	21,8	0,20	4,36	10	109,00	92,69
11,0	0,43	4,73	19,1	0,23	4,393	10	83,04	92,88
11,5	0,42	4,83	16,9	0,26	4,394	7	65,00	90,97
12,2	0,41	5,002	14,5	0,31	4,495	5	46,77	89,86
11,0	0,44	4,84	11,9	0,36	4,284	3	33,06	88,51
9,8	0,49	4,802	9,4	0,45	4,23	1	20,89	88,09

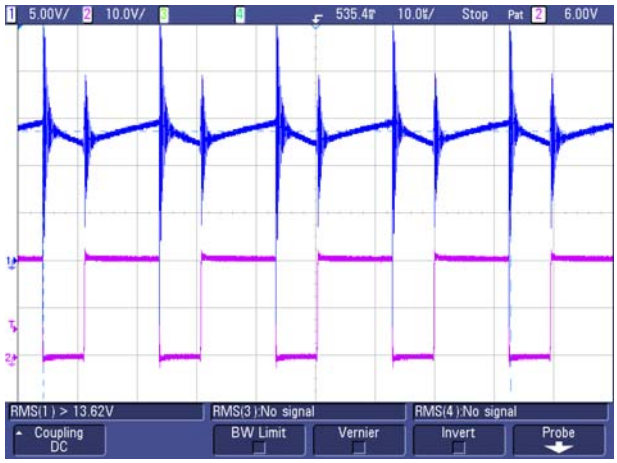

Fig. 5: Voltage source connected to a series resistance - 100 Ω load - input voltage (blue - above), MOSFET drain voltage (cyan - below).

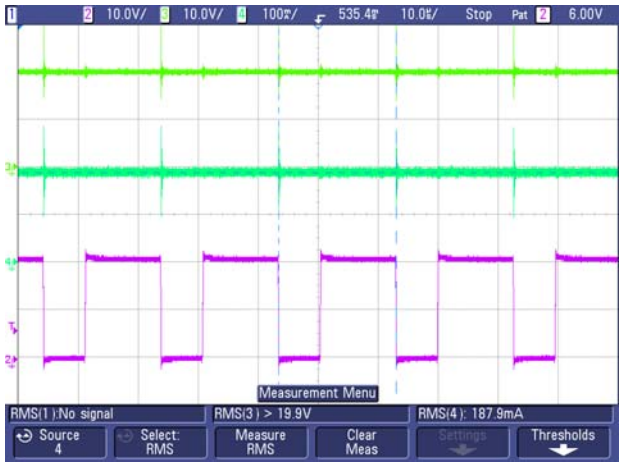

Fig. 6 Voltage source connected to a series resistance - 100 Ω load – load voltage (light green - above), load current (dark green - middle), MOSFET drain voltage (cyan - below).

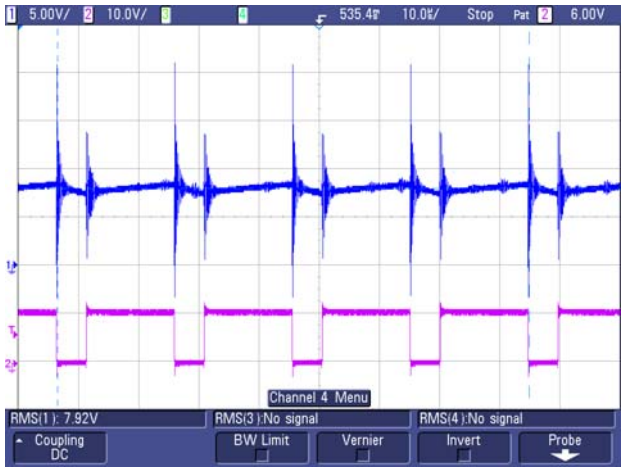

Fig. 7: Voltage source connected to a series resistance - 25 Ω load – input voltage (blue - above), MOSFET drain voltage (cyan – below).

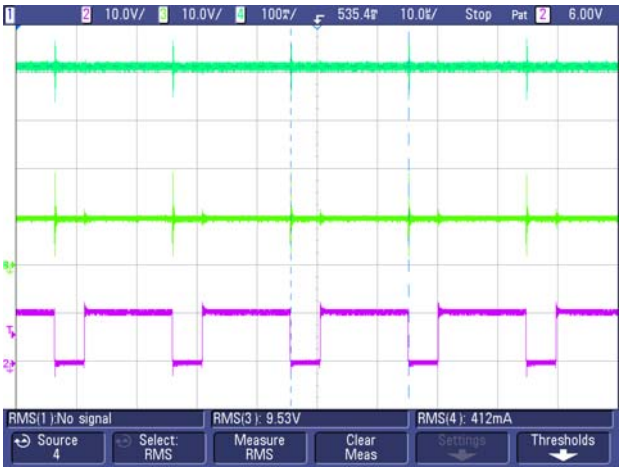

Fig. 8 Voltage source connected to a series resistance - 25 Ω load – load voltage (light green - above), load current (dark green - middle), MOSFET drain voltage (cyan - below).

2) Solar cell array

Table II shows some results with the solar cell array.

TABLE II
Results with solar cell array feeding a resistive load

Irradiation [lux]	Vin [V]	Iin [A]	Pin [W]	Vout (V)	Iout [A]	Pout [W]	Efficiency [%]
5000	9,5	0,09	0,855	10,0	0,08	0,8	93,57%
20000	13,6	0,13	1,768	14,0	0,10	1,4	79,19%
104000	17,1	0,57	9,747	26,9	0,33	8,877	91,07%

VI. CONCLUSION

This paper presented a MPPT algorithm implemented with a FPGA for PV generation system. The simple P&O MPPT algorithm was chosen and applied in a prototype for validation. Experimental results were shown, as well as some implementation details of the algorithm implemented in the FPGA. The fast prototyping environment provided by the FPGA indicates that such digital devices can be useful not only for this but for other power electronics applications including power electronics education.

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