Experimental results for a Low Voltage and High Efficiency Audio Power Amplifier Designed for Hearing Aids Applications

D. P. Mioni [1]; S. Finco [2]; J. A. Pomílio [3]

1, 2 – Centro de Pesquisa Renato Archer, Rod. D. Pedro I SP65, Km 143.6, CEP 13089-500
Campinas SP, Brazil Tel 55–19–3746 6055 www.cenpra.gov.br
3 – Universidade Estadual de Campinas - UNICAMP – Rua: Pandiá Calógeras nº 110 Cidade Universitária Zeferino Vaz, CP6101,
CEP 130830-970 Campinas SP, Brazil, Tel 55-19-3521-3710 www.unicamp.br

***Abstract* - This paper presents the development of a First-Order Sigma-Delta Audio Band Power Amplifier optimized for Hearing Aids (HA) devices. Actually, most of HA carries a 1.1V battery and needs a very low current consumption to improve battery's life. The use of voltage amplifiers and comparators with CMOS Inverter, biased in its linear region, was utilized. CMOS inverters gives a high voltage gain which can substitute operational amplifiers in some applications. An inverter cell supplied with a 1.1V will drain a maximum current of 1,2uA depending on its physical dimensions and it increases exponentially with increasing voltage supply. The circuit was implemented in a monolithic chip with CMOS 0.35um technology and proportionate up to 90% of power efficiency.**

***Keywords* – audio, amplifier, Class D, inverter-based, low voltage, Sigma-Delta.**

I. INTRODUCTION

Since the first electrical HA was developed, operated with granulated carbon microphones (1876) and later with vacuum tubes (1920), the need for miniaturization and lowering power consumption was the mainly objective to attain. The excessive waste of power assigned to inefficient transducers, tubes heating and poor power amplifiers were the main problem and batteries were heavy and large. Obviously battery's technology in this early days made it worse. In the early 1950, with the bipolar transistors developments, the HA became very smaller and efficiency improved. In the Figure 1 shows the evolution of the active components between 1939 and 1958. [5]

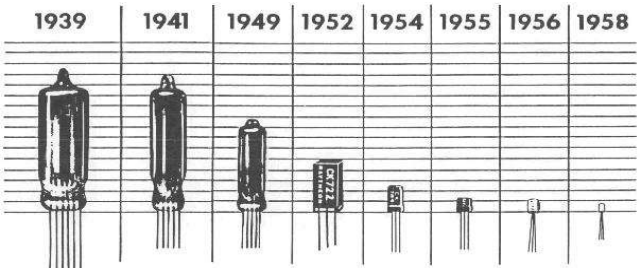

Figure 1 – Chronological development of active components

With innovations in output and input transducers, in the decade of 70, the power amplifier inside the HA began to have considerations relatives to the battery's life [5]. Actually, three basics components inside HA's have relative high power consumption; the microphone (normally pre amplified by a FET transistor operated in Class-A), the DSP and the power amplifier. In this paper is developed a high efficiency low voltage power amplifier modulated with a first order sigma delta which attend to HA's specification of power consumption.

Sigma Delta Modulation

The Sigma Delta Modulation was developed by H. Inose and Y. Yasuda in 1962, in order to improve the Delta Modulation [4]. The idea is to integrate the derived signal in the negative feedback making that resulting error very close to the switching reference, improving it's resolution. The Figure 2 shows the First Order Sigma Delta modulation in basic blocks.

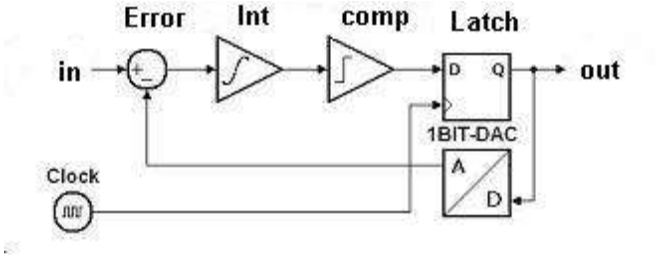

Figure 2 – First Order Sigma-Delta Modulator

The analog input IN is subtracted (derived) from the output modulated, which carries the average input signal. The error integrated is compared with the reference and this signal in bitstream form is latched, giving to the modulated signal, a least significant bit (LSB). The linearized mode of the Sigma-Delta (SDM) can be obtained as seen on Figure 3. The transfer function (1) shows that the noise is high pass filtered while the Input signal has only one bit delay, for this reason SDM is also called as "Noise Shaper".

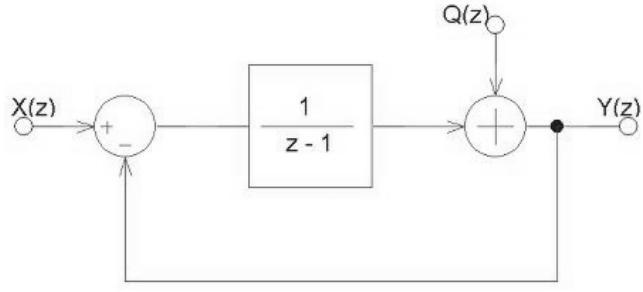

Figure 3 – Linearized model of a SDM

$$Y(z) = \frac{z-1}{z} Q(z) + \frac{X(z)}{z} \quad (1)$$

The Signal to Noise Ratio are obtained by the ratio of the RMS value of the power input signal and the RMS value of the noise power in the audio band [2,4,8]. For a First Order Sigma-Delta this ratio is given by:

$$SNR = (dB) = 9.03r - 3.4 \quad (2)$$

where *r* is the oversampling ratio defined by the relationship of the switching frequency and the highest frequency of the audio band desired. For this design purpose, the band does not need to excced 10KHz, so a SNR of 60dB relative to 20KHz is enough. For this, a 10MHz clock switching is required.

Analog applications with CMOS Inverter

CMOS inverters are designed to invert a logic level, saturating only one of the MOS transistors per logic level with very low power consumption. The higher the gain of the inverter block the higher will be its frequency capability. It is possible to amplifier an analog signal with a CMOS inverter if the input is biased in it's linear region [1]. This region is where both transistors are saturated giving a relative low impedance to ground, so the current drain is high. In Figure 4 is shown a CMOS characteristic voltage transfer for three different voltage sources and it's respective drain currents, for a minimal size in 0.35um technology.

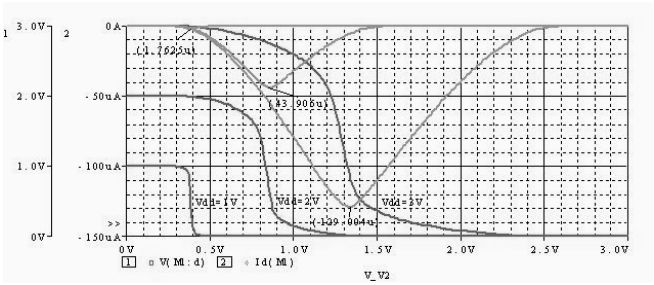

Figure 4 – Voltage Gain curves for 1V, 2V and 3V respectively with their relatives drain currents

Notice that for 3V source, the current in it's linear region, is extremely high (144uA). For a source of 2V the current is still high rounding 55uA. For a 1V, it goes down to 1.23uA which makes it affordable for low power applications.

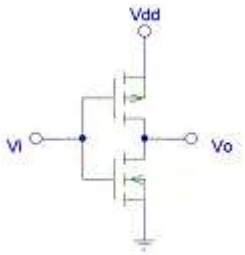

Figure 5 –Basic Inverter Cell

It can also be noted that the curve for 1V is steeper than the others, indicating that it has more open loop gain. One inverter with 1Vdd has a simulated open loop gain of 128, but with 3 inverter in cascade it can reach around 10.000. With this gain, it can substitute an operational amplifier in some applications, where it does not need a differential input [6]. For SDM applications, it is necessary to build a low pass-filter (or integrator for high frequencies), a comparator and a 1BIT D-A Converter. Another great advantage of the CMOS inverter is that it does not carries offset deficiencies as a typical operational amplifier [6, 7]. The low-pass filter was built as a simple RC filter buffered as shown on Figure 6.

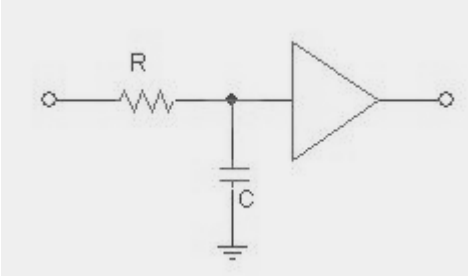

Figure 6 – Low-pass filter used to integrate the modulated signal

The comparator is simply an inverter Cell were the biased signal is just compared with the reference voltage of the comparator, which is the same as the bias of the input signal. The One Bit D/A converter is just another inverter cell. Its application is different whether the reference of the modulator is the ground, so the bitstream would modulate between –Vdd and +Vdd, in this case the reference is rounding 0.5Vdd the bitstream goes directly to the sum with the input.

Output Stage

The Load (receiver) receives the modulated signal by a H-Bridge made with power inverters as seen in the Figure 7.

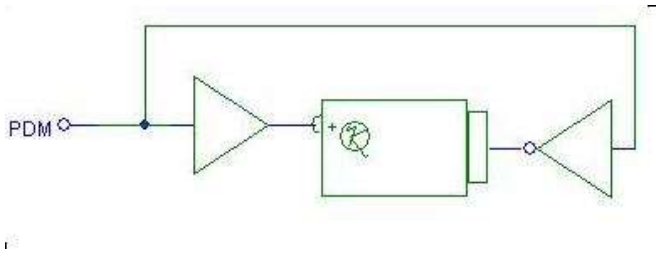

Figure 7 – H-Bridge connected with the Receiver

The modulated signal PDM (Pulse Density Modulation) is applied to it and the H-Bridge applies this PDM directly to the receiver.

The Receiver

In the present design the receiver (output speaker) utilized was the model EF-29802-000 kindly offered by Knowles Electroacoustics [5].

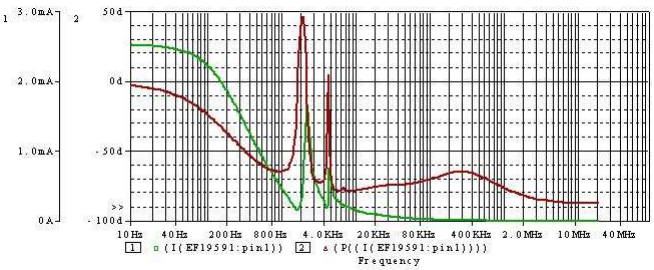

Figure 8 – AC analyze of Knowles Model Impedance and Phase

The receiver's curve simulated and shown in the Figure 8, shows that, in the switching frequency, its impedance is inductive, this means that it can receive directly the Bitstream without any external LC filter.

The Amplifier

The overall amplifier simulation is shown on the Figure 9.

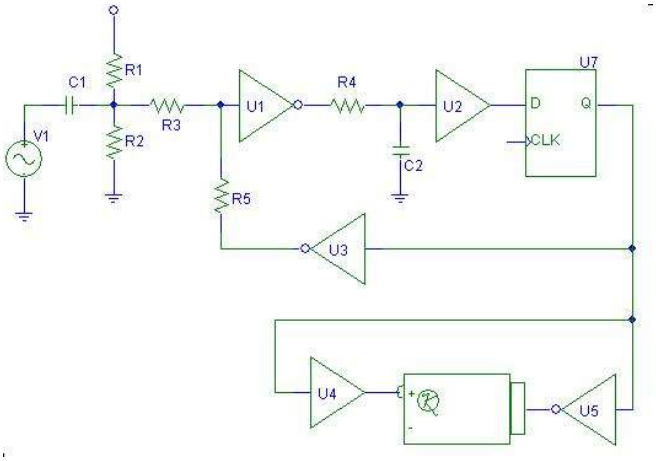

Figure 9 – Overall Power amplifier circuit

V1 is the input signal and it is AC coupled by C1. The input voltage reference is made by R1 and R2, where the input reference of U1 is reached by a thevenin application, taking the average value of the modulated signal of the U3.. The inverter U3 receives the bitstream of the flip-flop and inverts the signal which is summed with input signal by R3 and R5.
The figure 10 shows the input signal compared with the output signal, which is filtered with a simple RC filter.

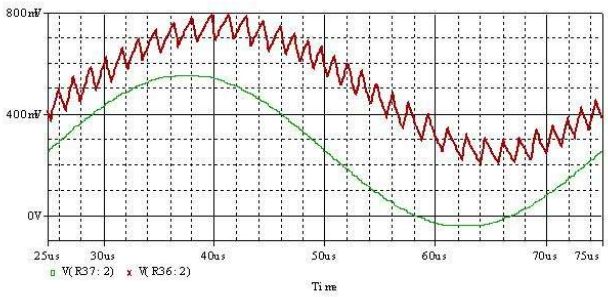

Figure 10 – Input Signal versus RC Filtered Output signal

In figure 11 the input is compared with the error signal. It can be noted that the input signal is added to the inverted output signal.

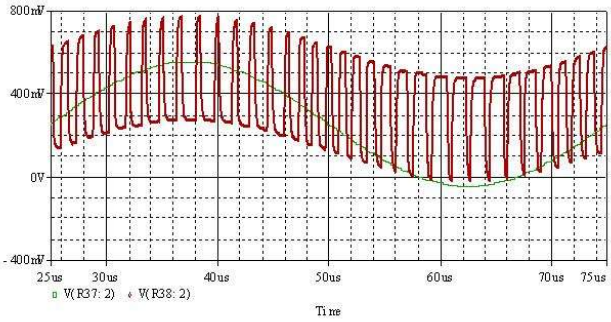

Figure 11 – Input Signal Versus Error of the difference

The integrated error is shown in the Figure 12, where the delay caused by the RC filter makes the difference oscilates around the reference.

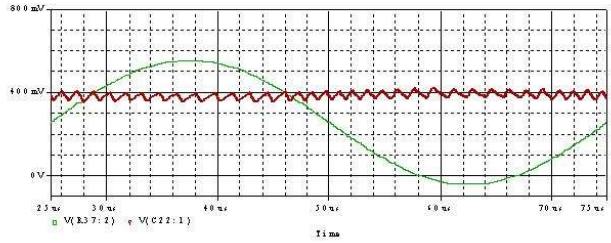

Figure 12 – Input Signal versus Integrated Error

Figure 13 shows the modulated output signal (Bitstream) compared with the input signal. Note that the signal is multiple of the LSB.

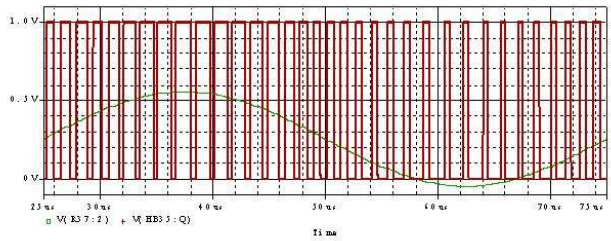

Figure 13 – Input Signal Versus PDM

The power efficiency in simulations reaches 89%, which is a acceptable value for the source supply required. Figure 14 compares the RMS power in the Source with the RMS power in the Load.

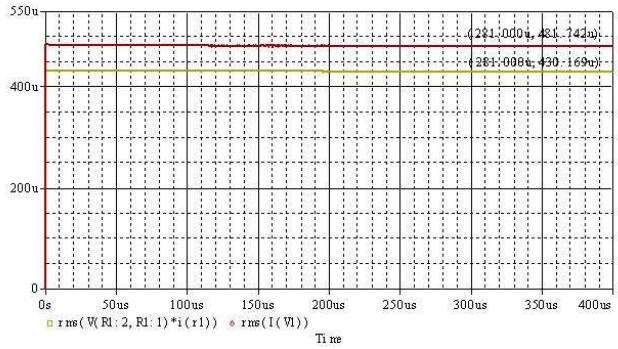

Figure 14 – Source RMS Power Versus Load RMS Power

II. EXPERIMENTAL RESULTS

To obtain some real results from the purpose article before the chip arrives, some tests with discrete components were realized. We utilized CD4069 CMOS Logic family, an octal inverter CI. The circuit was implemented without the use of the flip-flop, which can work very well with some losses in resolution. So, in other words, the analogic signal was modulated just by a ring oscillator. The results of the input signal, compared with the output signal, is shown in the figure 15.

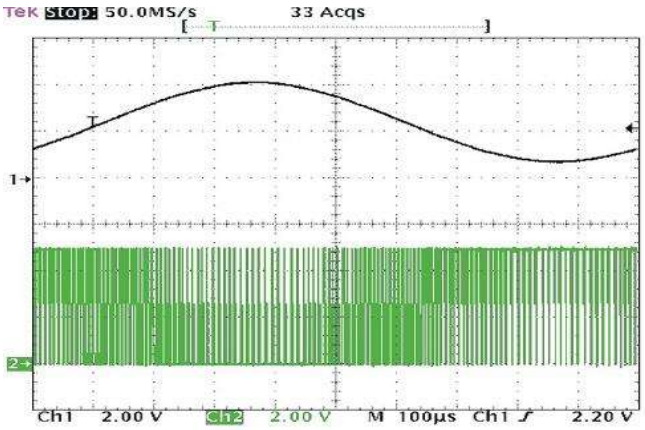

Figure 15 – Input Signal versus modulated output

Figure 16 shows the modulated signal filtered by a simple RC low-pass filter.

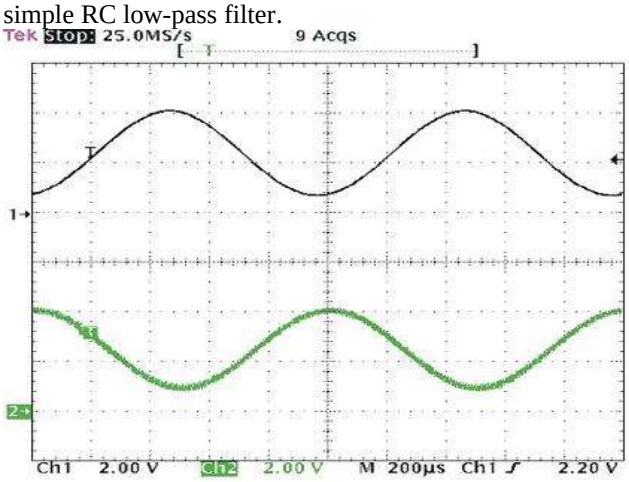

Figure 16 – Input Signal Versus RC filtered output signal

Finally, Figure 17, shows the FFT of the output signal. Note that the most of the quantization energy noise is spread out of the audio band with high-pass characteristics (20dB Dec). And the SNR (Signal to Noise Ratio) measured is rounding 60dB.

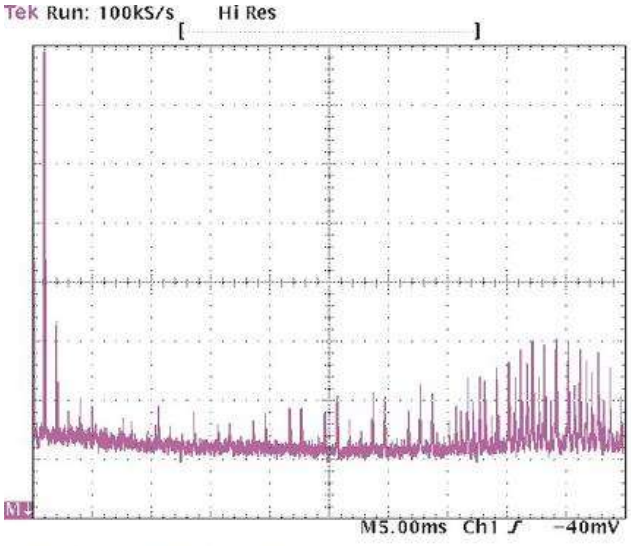

Figure 17 – FFT of the output modulated signal

Chip Measurementes

Figure 18, shows the funcionality of the chip. Waves labeled 1 and 2 are the two single inverted outputs to the differenetial load output with a 1KHz 500mVac source input. The wave labeled M, shows the diference between wave 1 and 2, with a 470R resistive load conected.

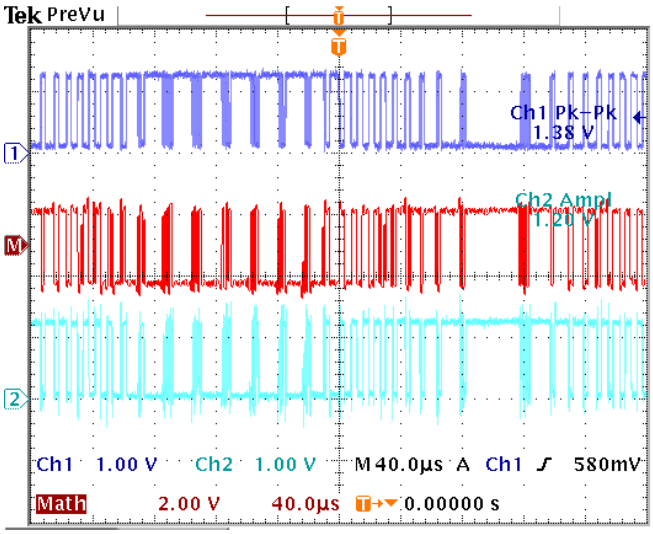

Figure 18 – Single and differential outputs of Class D amplifier

A sprectrum result of the M wave can be observed in the figure 19. The PDM modulation has spreaded the quantization noise out of the base band.

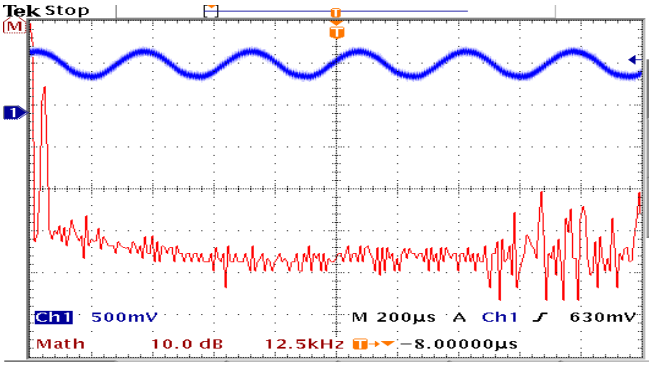

Figure 19 – analog input and FFT of the output waveform

A problem ocourred in the chip was that a delay circuit for the output pulses was not designed in the chip. So, an extra inverter circuit stage with a RC delay were needed to increase the efficience power consuption. The figure 20 shows the RMS value of a differential voltage across a 100 ohms serie resistance inserted in the load and in the source respectively. The efficience, with knowles reciever as a load, with a 1KHz sine wave is 82%.

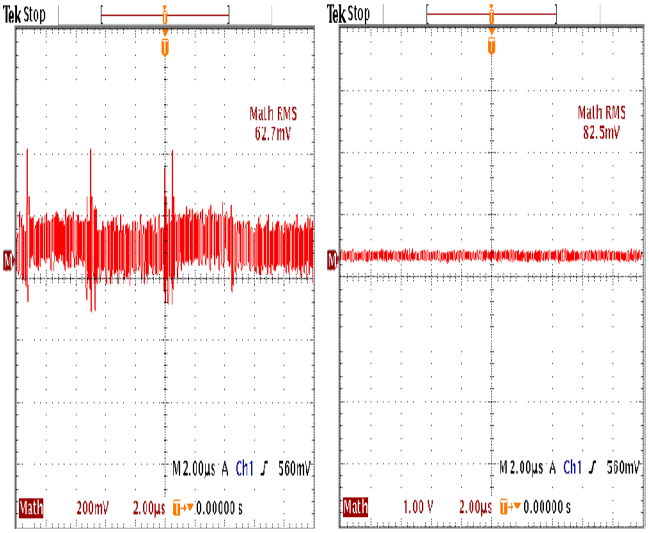

figure 20 – power efficience with an additional RC delay

The IC Layout

The circuit implemented is shown in Figure 21. The total area including pads connections is 1mm², and in Figure 22 the circuit without pads occupies a area of 600um².

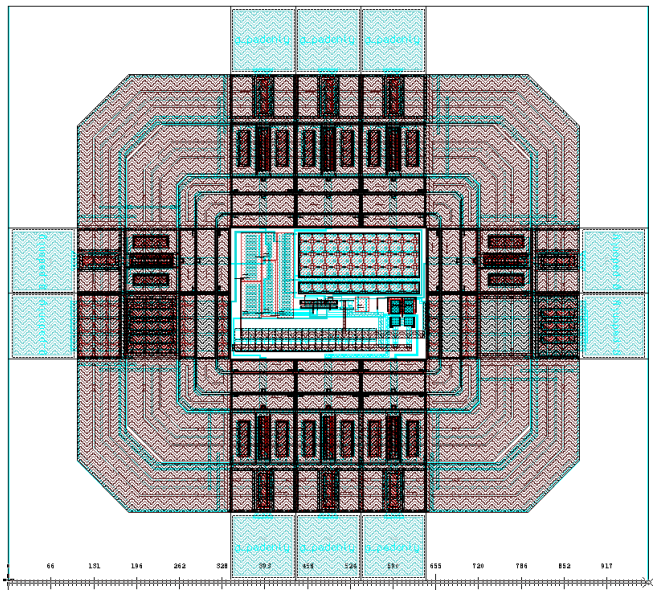

Figure 21 – Circuit's layout with pads

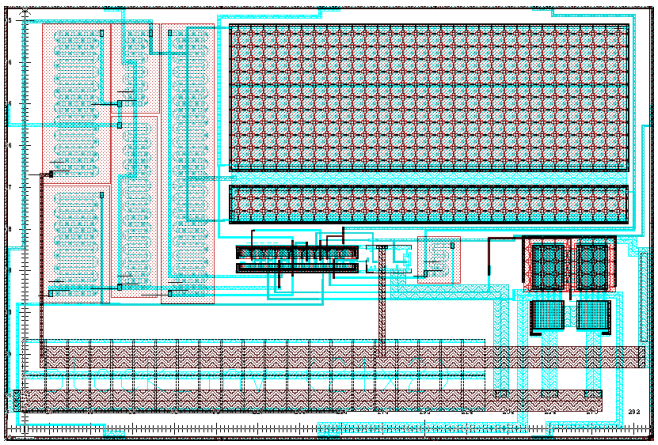

Figure 22 – Circuit's layout without pads

III. CONCLUSIONS

In the usual implementation of SDM, operational amplifiers and comparators consume a significant part of the modulator power.

By eliminating these blocks, in the inverter-based SDM implementation, we achieve increased efficience for the output stage. This results is very noticeable at the power level considered for this work.

Taking a look at the oscilloscope's results it can be noted that the circuit works very well. Just a little losses on SNR of the SDM relative to the low-pass filter. In a typical SDM it has a cut-off frequency below the audio band and in our project was calculated to be 20KHz not to exceed layout silicon area. This cut-off frequency has to integrate the switching frequency and the audio band. This RC filter can be replaced by a transconductance filter technology, which can attain a lower cutt-off frequency improving SNR, not exceeding silicon area. Doing this, makes the error signal closer to the reference giving a better resolution. But, a higher cut-off can make it work as well, for some applications, as in our purpose.

An additional RC delay must be included on the chip for efficiency reasons. It can be noted too, that a better dimensions of the inverters can reduce the noise transistion on the output MOS.

IV. References

Bibliography References

[1] Uyemura J. P. “Circuit design for CMOS VLSI” – First Edition. Kluwer Academic Publishers [1992] ISBN 0-7923-9184-5

[2] Soin R. S. et al. “Analogue – Digital ASICs circuit techniques, design tools and applications” – IEE Circuits and Systems Series 3. [1991] ISBN 0 86341 259 9

[3] Almeida K. and M. C. M. Iorio “Próteses Auditivas Fundamentos Teóricos e Aplicações Clinicas”. Second Edition. Editora Lovise. [2003] ISBN 85-85274-81-6

[4] Raymundo P. G. “Estudo dos limites de Performance dos moduladores Sigma-Delta com Circuitos a Capacitores Chaveados” Dissertation submitted to the University of Campinas – UNICAMP - SP Brazil - Electrical Engineer Department, for master degree.[2001]

Internet References

[5] http://www.knowleselectronics.com/engineering/pdf/Design%20Evolution%20of%20Miniature%20Electroacoustic%20Transducers.pdf#search=%22Design%20Evolution%20of%20Miniature%20Electroacoustic%20Transducers%22

[6] http://www.ele.uva.es/~jesus/inversores.pdf

[7] http://www.ele.uva.es/~jesus/microdelta.pdf

[8] http://paginas.terra.com.br/educacao/audiolist/artigos/sigma_delta_V4.pdf