A SOFT SWITCHING DOUBLE FORWARD CONVERTER OPERATING AS A FULL BRIDGE TOPOLOGY

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***Abstract* — This paper proposes a topology for the association of two forward converters, attached to the same transformer and operating as a full bridge configuration. The transformer and the output filter are designed for twice the switching frequency of a single leg. Each one of the forward converters employs a lossless commutation cell that allows high switching frequency, high power operation and high efficiency for a wide load range. The effect of the leakage inductances of the transformer in the soft commutation is analyzed and possible solutions are also presented. The complete mathematical study, including analytical results to validate the proposal, is carried out.**

***Keywords* - forward converters, parallelism of converters, soft switching.**

I. INTRODUCTION

The development of dc-dc converters with high efficiency, small size and weight, low cost, and high power has been of great interest. In isolated converters, high switching frequency has been employed in order to decrease the transformer size. Moreover, most of such converters require only one cycle of the transformer hysteresis, as the full capacity of the transformer is not used.

Interleaving techniques consist in the interconnection of multiple switching cells for which the operating frequency is the same, but the internal switching instants are sequentially phased over fractions of the switching period. Multiphase parallel operated power converters provide power sharing and reduce input and output ripple currents. Filter components are reduced and the output current response time can be minimized [1].

The structure depicted in Figure 1 can be understood as two forward converters operating alternately, as the output power is twice that of a single topology, if the same transformer is considered. Another important characteristic lies in the reduced blocking voltage across the semiconductor devices. As more power is demanded, two or more double forward converters can be paralleled [2].

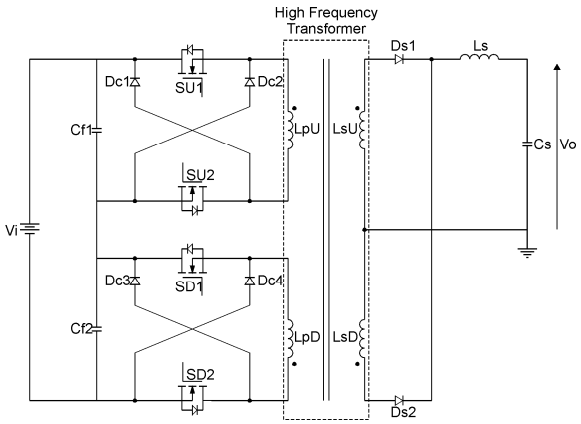


Figure 1. Double forward converter.

The requirement of high frequency operation is evident to reduce of the audible noise, volume and weight of magnetic elements, as well as to improve output voltage quality. However, at high frequency operation, switching losses and electromagnetic interference (EMI) become significant and must be analyzed in detail [3]. Power semiconductor devices commutate under two possible techniques: hard and soft [4]. With hard switching, the devices are required to change their states (on and off), while they are subjected at both finite current and voltage values. High switching stresses produced by an overlapping between voltage and current result in high switching losses. Soft switching aim is to reduce the mentioned overlap between voltage and current during the commutation. Thus it is possible to reduce switching losses, enabling high frequency operation and achieving higher power density.

II. THE PROPOSED TOPOLOGY

The soft switching double forward converter proposed in this paper is shown in Figure 2, where a single transformer with two primary, two secondary and two tertiary windings is employed. Since a full bridge topology has the same characteristics of the proposed one, it can be used as a pattern for eventual comparisons [5].

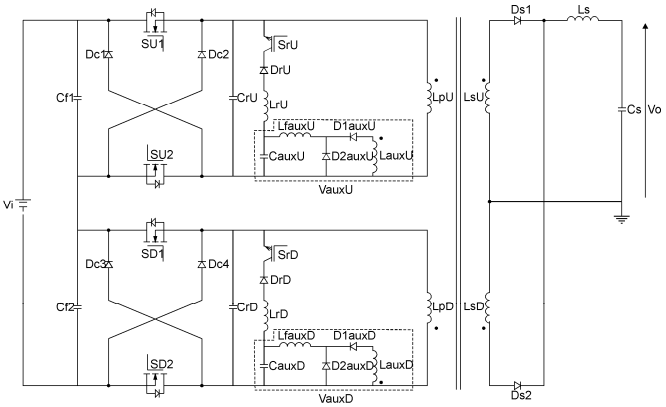


Figure 2. Double forward converter associated with a lossless commutation circuit.

In this converter, auxiliary switches S_{rU} and S_{rD} operate in ZCS mode to charge resonant capacitors C_{rU} and C_{rD}, respectively, in order to provide the commutation of the main switches in ZVS mode. Therefore soft switching is obtained more easily than in full bridge structures. Besides, the control circuit does not require a dead time.

An additional advantage of this converter is the reduced voltage across the main switches, equal to half the input voltage. As the forward topologies operate alternately, the switching frequency of each leg is one half of the total switching frequency i.e. $f_s/2$. Therefore, switching losses are proportionally reduced, although the transformer and the output inductor are designed for one time the switching frequency, implying reduced weigh and size.

As the associated converters are analogous, let us consider, for instance, only the upper soft switching cell, composed by S_{rU}, D_{rU}, L_{rU}, C_{rU}, C_{auxU}, L_{fauxU}, D_{1auxU}, D_{2auxU}, and L_{auxU}. An auxiliary DC voltage source V_{auxU} is required by the resonant circuit, and it is represented by C_{auxU}, L_{fauxU}, D_{1auxU}, D_{2auxU}, and L_{auxU}.

III. MATHEMATICAL ANALYSIS

In order to simplify the analysis of the circuit, the following assumptions are made:
- The input voltage is constant;
- All semiconductor devices are ideal;
- Capacitors C_{f1} and C_{f2} are considered voltage sources;
- The leakage inductance of the transformer is null, and the magnetizing inductance is infinite;
- Inductor L_s is considered a current source;
- Voltages V_{auxU} and V_{auxD} must be at least one fourth of the input voltage, so that the voltages across capacitors C_{rU} e C_{rD} are equal to half the input voltage, causing the zero voltage switching of the main switches;
- The operation of each leg is identical and complementary.

The operating stages are presented in Figure 3, and the main waveforms are shown in Figure 4.

• First stage [t_0-t_1] (Figure 3 (a)) – Linear stage.

Before instant $t=t_0$, diodes D_{s1} and D_{s2} conduct the load current I_L. At t_0, switch S_{rU} is turned on in ZCS mode due to resonant inductor L_{rU}. Current $i_{LrU}(t)$ flows through L_{pu}, and increases linearly from null to I_M i.e. the load current referred to the primary winding. Then energy is transferred to the load and efficiency is not affected. According to (1), the current through resonant inductor L_{rU} is:

$$i_{LrU}(t) = \frac{V_{auxU}}{L_{rU}} \cdot t \tag{1}$$

The time interval that defines the first stage is:

$$\Delta t_1 = t_1 - t_0 = \frac{I_M}{V_{auxU}} \cdot L_{rU} \tag{2}$$

• Second stage [t_1-t_2] (Figure 3 (b)) – Resonant stage.

Current $i_{LrU}(t)$ charges capacitor C_{rU} positively. At the same time, the induced current through winding L_{pD} starts charging capacitor C_{rD} negatively, what occurs while $i_{LrU}(t)>I_M$. This stage finishes when the voltages across C_{rU} and C_{rD} equal $V_i/2$ and $-V_i/2$, respectively, at the same time. Under this condition, switches S_{U1} and S_{U2} can be turned on in ZVS mode. Therefore the following expressions are valid:

$$C_r = C_{rU} + C_{rD} = 2 \cdot C_{rU} = 2 \cdot C_{rD} \tag{3}$$

$$Z_0 = \sqrt{\frac{L_{rU}}{C_r}} \tag{4}$$

$$\omega_0 = \frac{1}{\sqrt{L_{rU} \cdot C_r}} \tag{5}$$

where C_r is the equivalent capacitance, Z_0 is the characteristic impedance, and ω_0 is the resonant frequency.

From (4) and (5), expressions (6) to (8) result.

$$i_{LrU}(t) = \frac{V_{auxU}}{Z_0} \cdot \sin(\omega_0 \cdot t) + I_M \tag{6}$$

$$i_{LpD}(t) = -\frac{V_{auxU}}{Z_0} \cdot \sin(\omega_0 \cdot t) \tag{7}$$

$$i_{CrU}(t) = \frac{V_{auxU}}{Z_0} \cdot \sin(\omega_0 \cdot t) \tag{8}$$

The voltages across capacitors C_{rU} and C_{rD} are given by (9) and (10), respectively.

$$v_{CrU}(t) = V_{auxU} \cdot \left[1 - \cos(\omega_0 \cdot t)\right] \tag{9}$$

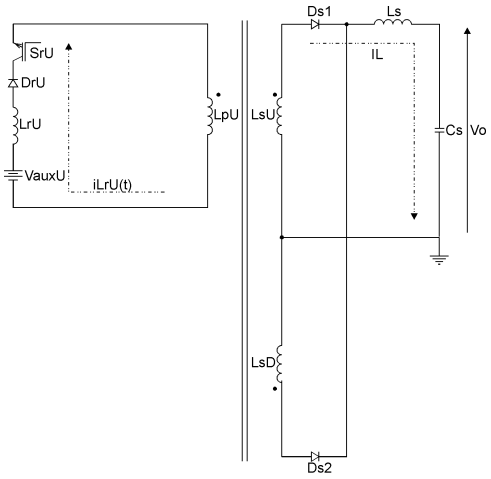
$$v_{CrD}(t) = -V_{auxU} \cdot \left[1 - \cos(\omega_0 \cdot t)\right] \tag{10}$$

The time interval that defines the second stage is:

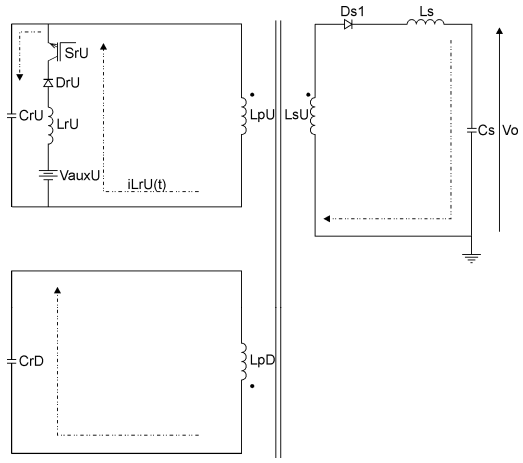
$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_0} \arccos\left(1 - \frac{V_i}{2 \cdot V_{auxU}}\right) \tag{11}$$

To obtain soft switching, the voltage across must become $V_i/2$ before the current through inductor L_{rU} equals I_M. Then the condition in (12) must be observed, as an increase of 10% in V_{auxU} is due to conduction losses.

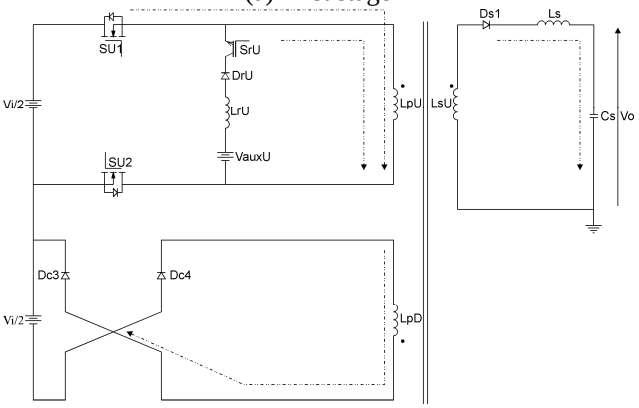
$$V_{auxU} = V_{auxD} \geq 1.1 \cdot \frac{V_i}{4} \tag{12}$$



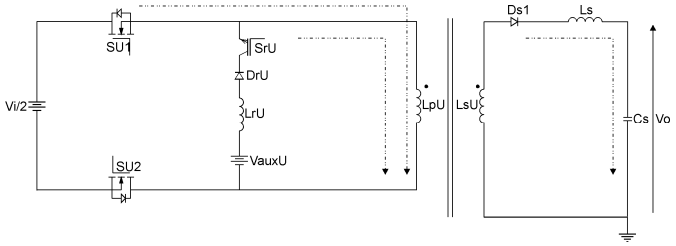
(a) First stage



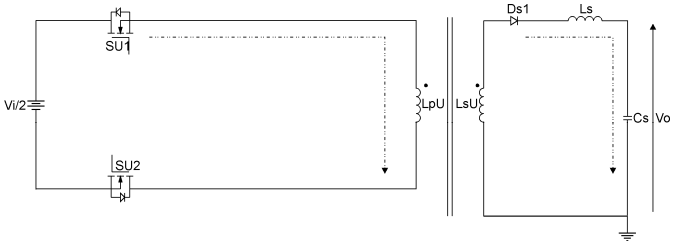
(b) Second stage



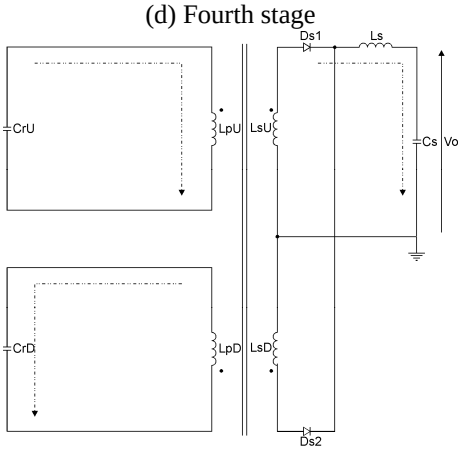
(c) Third stage



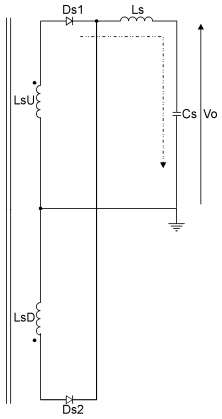
(d) Fourth stage



(e) Fifth stage



(f) Sixth stage



(g) Seventh stage

Figure 3. Equivalent circuits for the operating stages.

• Third stage [t_2-t_3] (Figure 3 (c)) – Linear stage.

At the beginning of this stage, the voltages across the auxiliary sources are less than $V_i/4$ i.e. current $i_{LrU}(t)$ has not reached I_M, and $i_{LpD}(t)$ is not null yet. Therefore this must be considered a stage of transition where the aforementioned conditions are supposed to be achieved.

The current through switches S_{U1} and S_{U2} increases linearly from a negative value to null, and the current through inductor L_{rU} decreases linearly to I_M. Diodes D_{c3} and D_{c4} conduct the remaining current through L_{pD} until it becomes null at the end of the stage.

From the initial condition of the resonant inductors, the currents through L_{rU} and L_{pD} can be obtained as in (13) and (14).

$$i_{LrU}(t) = \frac{V_{auxU}}{Z_0}\cdot\left(2-\frac{V_i}{2\cdot V_{auxU}}\right)+I_M-\frac{V_i/2-V_{auxU}}{L_{rU}}\cdot t \quad (13)$$

$$i_{LpD}(t) = \frac{V_{auxD}}{Z_0}\cdot\left(2-\frac{V_i}{2\cdot V_{auxD}}\right)-\frac{V_i/2-V_{auxD}}{L_{rD}}\cdot t \quad (14)$$

The time interval that defines the third stage is given by:

$$\Delta t_3 = t_3 - t_2 = \frac{V_{auxU}}{Z_0}\cdot\left(2-\frac{V_i}{2\cdot V_{auxU}}\right)\cdot\frac{L_{rU}}{V_i/2-V_{auxU}} \quad (15)$$

• Fourth stage [t_3-t_4] ((d)) – Linear stage.

The current through L_{rU} still decreases linearly, while the current through switches S_{U1} and S_{U2} increases from null to I_M. This stage finishes as $i_{LrU}(t)$ becomes null and switch S_{rU} is turned off in ZCS mode.

The current through L_{rU} is:

$$i_{LrU}(t) = I_M - \frac{V_i/2-V_{auxU}}{L_{rU}}\cdot t \quad (16)$$

The time interval that defines the fourth stage is given by:

$$\Delta t_4 = t_4 - t_3 = \frac{I_M\cdot L_{rU}}{V_i/2-V_{uxU}} \quad (17)$$

• Fifth stage [t_4-t_5] (Figure 3 (e)) – Constant stage.

During this stage, energy is transferred to the load, and it finishes when switches S_{U1} and S_{U2} are turned off in ZVS mode. The PWM controller determines the time interval of this stage.

• Sixth stage [t_5-t_6] (Figure 3 (f)) – Linear stage.

Resonant capacitors C_{rU} and C_{rD} are discharged as the voltages across them become null. Diode D_{s2} is turned on due to the discharge of C_{rD}. The voltages across C_{rU} and C_{rD} are given by (18) and (19), respectively.

$$V_{CrU}(t) = \frac{V_i}{2}-\frac{I_M}{C_{rU}}\cdot t \quad (18)$$

$$V_{CrD}(t) = \frac{I_M}{C_{rD}}\cdot t-\frac{V_i}{2} \quad (19)$$

The time interval that defines the sixth stage is given by:

$$\Delta t_6 = t_6 - t_5 = \frac{V_i\cdot C_{rU}}{2\cdot I_M} \quad (20)$$

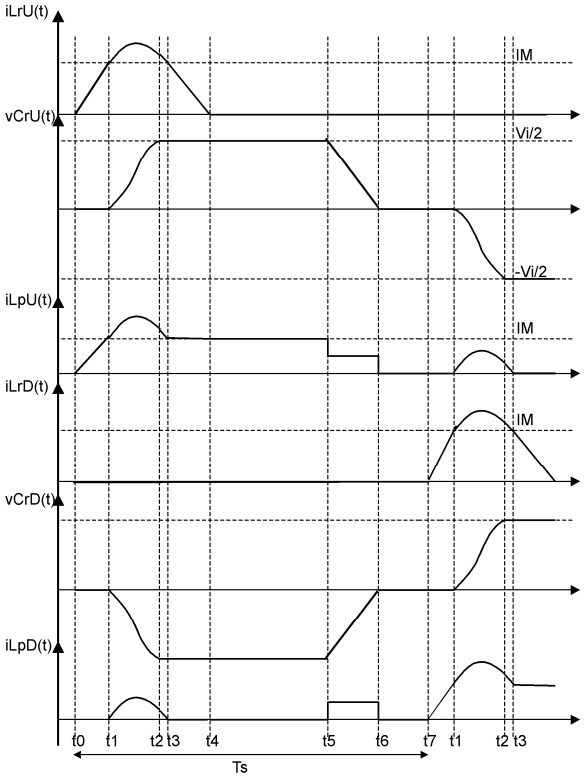


Figure 4. Theoretical waveforms.

• Seventh stage [t_6-t_7] (Figure 3 (g)) – Freewheeling stage.

No more energy is transferred to the load, and the load current is freewheeling through diodes D_{s1} and D_{s2}. The PWM controller determines the time interval of this stage, after which the operation of the lower forward converter begins.

IV. SIMULATION RESULTS

In order to evaluate the proposed converter, the parameters set shown in Table I was employed. Simulation tests were performed considering and neglecting the effects of the leakage inductances of the transformer.

Table I
Parameters set employed in the tests

Parameter	Description
Dc input voltage	V_i=400 V
Switching frequencies	f_{s1}=f_{s2}=75 kHz
Efficiency	η=95%
Filter capacitors	C_{f1}=C_{f2}=330 µF
Resonant capacitors	C_{rU}=C_{rD}=3.3 nF
Resonant inductors	L_{rU}=L_{rD}=4 µH
Primary windings	L_{pU} =L_{pD}=1 mH
Secondary windings	L_{sU}=L_{sD}=600 µH
Tertiary windings	L_{auxU}=L_{auxD}=600 µH
Auxiliary capacitors	C_{auxU}=C_{auxD}=33 µF
Auxiliary inductors	L_{fauxU}=L_{fauxD}=50 µH
Output inductor	L_s=100 µH
Output capacitor	C_s=15 µF
Load voltage	V_o=50 V
Output power	P_o=2000 W
Diodes	HFA08TB60
Main switches S_{U1}, S_{U2}, S_{D1}, S_{D2},	MOSFET – IRFP264
Auxiliary switches S_{rU} and S_{rD}	IGBT – IRG4BC20U

A. Neglecting The Leakage Inductances of the Transformer

Figure 5 depicts the resonant tank waveforms, where it can be seen that the voltage stresses across the resonant capacitors do not exceed $V_i/2$. In Figure 6, one can see that switches S_{rU} and S_{rD} are turned on and off in ZCS mode. The voltage stresses across the switches are greater than $V_i/2$ due to the auxiliary sources. Figure 7 and Figure 8 corresponds to the ZVS turning on and turning off of switches S_{U1}, S_{U2}, S_{D1}, and S_{D2}, respectively.

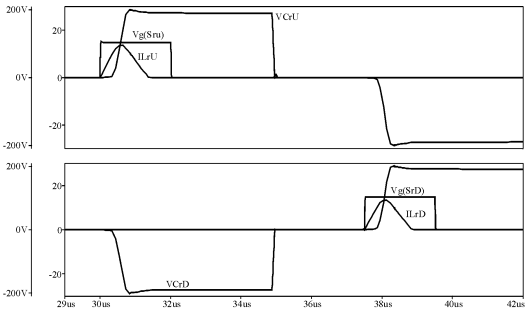


Figure 5. Resonant tank waveforms.

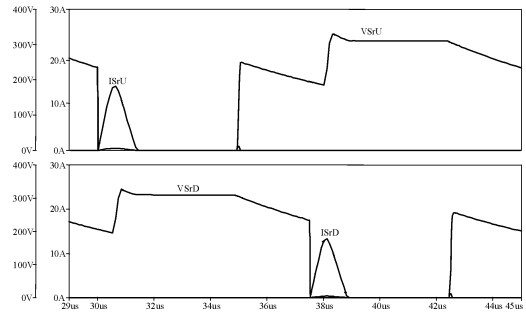


Figure 6. Switching detail in switches S_{rU} and S_{rD}.

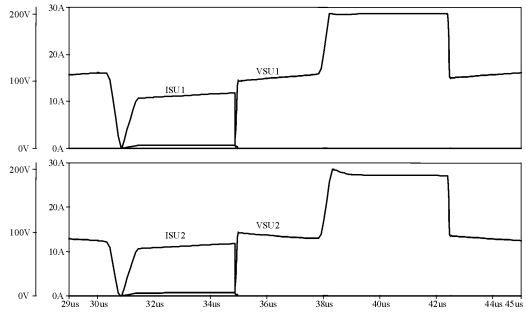


Figure 7. Switching detail in switches S_{U1} and S_{U2}.

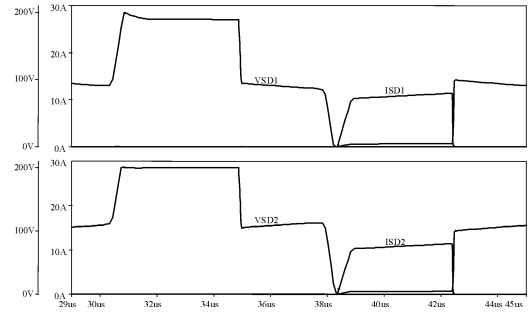


Figure 8. Switching detail in switches S_{D1} and S_{D2}.

B. Considering the Leakage Inductances of the Transformer

Two leakage inductances defined as L_{lkpU} and L_{lkpD} exist in the transformer, and can be added in series with primary windings L_{pU} and L_{pD} in Figure 2, respectively. In the simulation tests, one has considered L_{lkpU}=L_{lkpD}=4 µH.

Figure 9 represents the resonant tank waveforms and the gating signals of auxiliary switches S_{rU} and S_{rD}. It can be seen that the voltages across the resonant capacitors oscillate when a switch is turned on or turned off due to the leakage inductances. Soft switching can not be achieved, as in Figure 10.

In order to overcome this limitation, three solutions can be proposed as follows.

1) Diodes can be placed in series with the primary windings in order to avoid oscillation when the switches are turned off. However, conduction losses are increased, affecting the converter efficiency;

2) The voltages across the resonant capacitors can be clamped to null or $V_i/2$ if the on time of the switches is modified using the phase shift modulation technique [6]. However, it is a complex solution, once that the duty cycle of some switches is greater than 0.5. According to Figure 11, switches S_{U1} and S_{D1} control the energy transferred to the load, and switches S_{U2} and S_{D2} cause the voltages across the resonant capacitors to be clamped;

3) The aforementioned solutions modify the control system and the power stage sensibly, increasing the complexity of the topology. Alternatively, a dual thyristor gate driver can be employed since no drastic changes are introduced. This is not a solution as efficient as those previously presented, although soft switching is also obtained. Therefore, this will be the arrangement adopted in the experimental prototype.

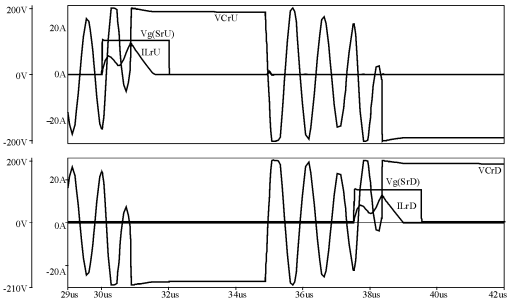


Figure 9. Resonant tank waveforms and gating signals of auxiliary switches S_{rU} and S_{rD}.

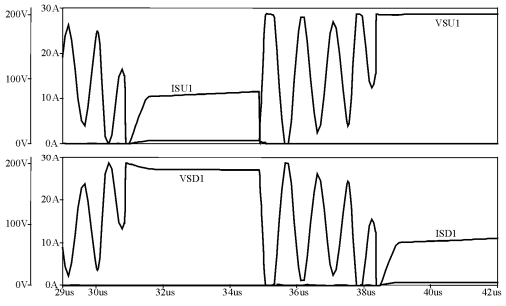


Figure 10. Switching detail in switches S_{U1} and S_{D1}.

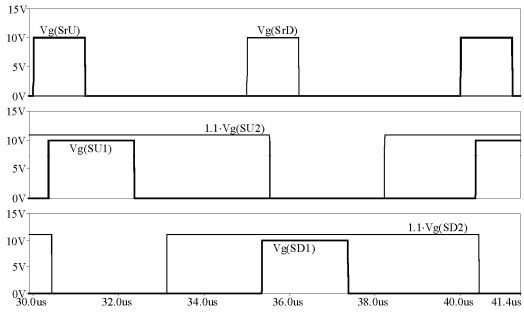


Figure 11. Gating signal of switches using phase shift modulation.

V. EXPERIMENTAL RESULTS

The prototype was implemented using the same parameters set described in Table I.

Figure 12 shows the switching detail in switch S_{rU}. The effect of the leakage inductances in the converter performance is clearly evidenced in the peak resonant current through switch S_{rU}.

Figure 13 represents the switching detail in one of the main switches. As the voltage across switch S_{U1} does not become null at the end of the second stage due to the peak resonant current, a second oscillation is supposed to take the voltage across the resonant capacitor to about $V_i/2$. Therefore the dual thyristor is able to drive the switch with reduced stress.

The efficiency curve of the converter is shown in Figure 14. As expected for soft switching converters, efficiency is reduced when the output power is low because it is necessary to provide energy to the resonant elements. As the output power increases, such amount of energy tends to become less significant in the overall efficiency.

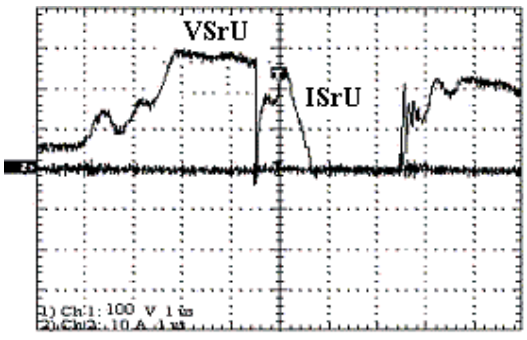


Figure 12. Switching detail in switch S_{rU}.

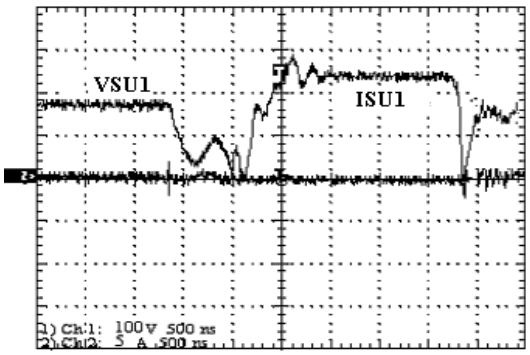


Figure 13. Switching detail in switch S_{U1}.

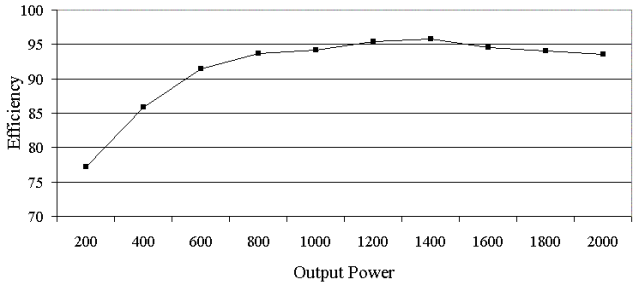


Figure 14. Efficiency as a function of the output power.

VI. CONCLUSION

This paper has proposed a double forward converter employing a soft switching cell which operates as a full bridge configuration. The main advantages over conventional full bridge topologies lie in the decrease of the voltages across the main switches and simplicity of control system configuration.

The influence of the leakage inductances of the transformer in the soft switching was analyzed, and the dual thyristor gate driver is the former choice if simplicity is a mandatory issue. It has been demonstrated by the experimental results obtained from a prototype that the main switches are turned on and off under null voltage. Additionally, the auxiliary switches are switches are turned on and off under null current condition. Therefore high efficiency results since switching losses become negligible.

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