A SIMPLE SELF-CLAMPED HIGH STEP-UP DC-DC CONVERTER EMPLOYING COUPLED INDUCTOR

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***Abstract* – This paper proposes a high-voltage-gain boost-based converter employing a coupled inductor. The proposed circuit presents high efficiency, absence of clamping circuits for limiting the voltage spikes over all semiconductor devices and reduced number of components. Besides employing a coupled inductor, the converter also has two stacked capacitors in its output. Thus, the total voltage gain is defined by the duty cycle, the turns ratio of the coupled inductor and the sum of these two capacitor voltages, resulting in the high gain of the system. It is demonstrated that the efficiency is high, because extreme duty cycle values are avoided. Its steady-state operating principle are presented. So, it can be observed that maximum voltage spikes on the all semiconductors (main switch and diodes) is equal to the output voltage Vo, turning the proposed converter suitable for applications where voltage levels on the load need to be not too high (400 V - 600 V). Finally, experimental results in by open loop control are presented for 30 V and 48 V input voltages, 400 V output voltage, 100 kHz switching frequency and 300 W output power.**

***Keywords* – Boost converter self-clamped; High efficiency; Step-up dc-dc converter.**

I. INTRODUCTION

Electricity, besides observed in nature as a physical phenomenon such as electrostatic discharge, is neither found nor produced so simply. To produce electricity and use it on his own advantage, mankind usually makes use of non-renewable natural resources such as oil, coal and natural gas and renewable sources such as solar, biofuels and water. Given that natural fossil sources are limited and, as far as they are consumed, they cause irreparable harm to the environment and to many forms of life, other renewable sources are also being used more intensively to produce electric energy. According to the U.S. EIA (Energy Information Administration), energy production from alternative sources is expected to increase by an average of 2.3% per year by 2040 [1]. In this sense, it can be said that the generation of energy from renewable sources such as wind, solar and fuel cells is no longer an option but a necessary reality. However, controlling and conditioning the energy provided by these sources are performed by systems that have their own operating characteristics and are subject of study by many experts around the world. One of the main challenges is to get energy to reach its destination loads with minimum waste [2]. Therefore, the use of switching power converters for interconnecting the generation source and the load is the best option to condition and control the flow of energy and achieve the desired efficiency levels [3]-[8].

Regarding the electronic processing of energy from fuel cells and photovoltaic systems, a dc-dc converter operating at high frequency is commonly used [3]-[31]. For achieving a high efficiency, some operating characteristics of the circuit are desirable, like reduced conduction and switching losses, low voltage clamping on the semiconductors, energy regeneration during the switching process without employing auxiliary circuits, supply continuous current from the input power source and low component count. Providing all these characteristics into a unique converter is not an easy task and is hardly achieved. Photovoltaic panels and fuel cells produce energy at very low voltage levels and, generally, it is necessary to process it in order to get far higher levels. In this sense, most proposals employ topologies based on coupled inductors [3]-[18]. It is known that classic step-up converters like the boost is not appropriate in most cases, because the voltage gain depends only on the duty-cycle [3]. In such case, due to non-idealities present in the circuit elements, the global efficiency becomes too low at high duty-cycle values [3]-[7]. On the other hand, due to the leakage inductance, in topologies that employs inductors with two or more coupled windings to rise the voltage gain, auxiliary circuits for clamping the semiconductors voltage spikes are necessary on most cases, which increases the number of components and may reduce efficiency [3]-[7], [11]. Other non-boost-based configurations are also used in order to raise the voltage gain. In such cases, the component count may become expressive, as in circuits that employs voltage multiplying cells [3]-[7], [16]-[17].

In most papers found in the literature, generally in order to obtain high-voltage gain and to avoid voltage spikes on the switches, clamping circuits (passive or active) and power devices such as diodes and capacitors has been added to the switched-mode converters [6],[10],[16],[20]-[21]. The increase of power devices and passive components count, as well as of clamp circuits, can reduce the overall system efficiency. However, in applications where the output voltage levels need not be too high, due to advances of semiconductor technologies which have low drain–source on-state resistance such as CoolMOS™ Silicon (Si), Silicon Carbide (SiC) and Gallium Nitride (GaN) [30], it is possible to employ simple topologies without adding many components such as in the proposed converter. In this work,

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a high gain and high efficiency boost-based dc-dc converter with coupled inductor is proposed. This circuit presents natural voltage clamping on all semiconductor devices (MOSFET and diodes) without needing auxiliary circuits, thus contributing to reducing the total number of components. Furthermore, due to a low blocking voltage level on the main switch during the turn-on transition period, the switching losses are low, helping to increase the overall system efficiency. However, the maximum voltage spikes on all semiconductors are equal to the output voltage and the input source supplies a pulsating current which needs an input filter in some applications. In this case, the component count can be similar to the topologies that performance naturally continuous input current.

Experimental results are presented for an input voltage between 30 V and 48 V, 400 V output voltage, 100 kHz switching frequency and 300 W output power.

II. PROPOSED TOPOLOGY

The proposed topology studied in this work is presented in Figure 1.a. It can be noted that the input stage comprises the coupled inductor primary-side winding, with its magnetizing inductance L_m, and the switch S. The inductance L_k represents the leakage inductance of the coupled inductor. The output stage consists of the coupled inductor secondary-side winding, two diodes D_1 and D_2, and two capacitors C_1 and C_2. By details analysis, some important operational characteristics can be observed, like the definition of V_o as the sum of voltages V_{C1} and V_{C2} and that it can be observed that maximum voltage spikes on the all semiconductors (main switch and diodes) is equal to the output voltage V_o. Due to D_2 connection, the system becomes non-isolated. During the initial period of the converter operation after reaching the steady state, the coupled inductor performs like a conventional transformer, because both primary and secondary windings process energy during the whole interval

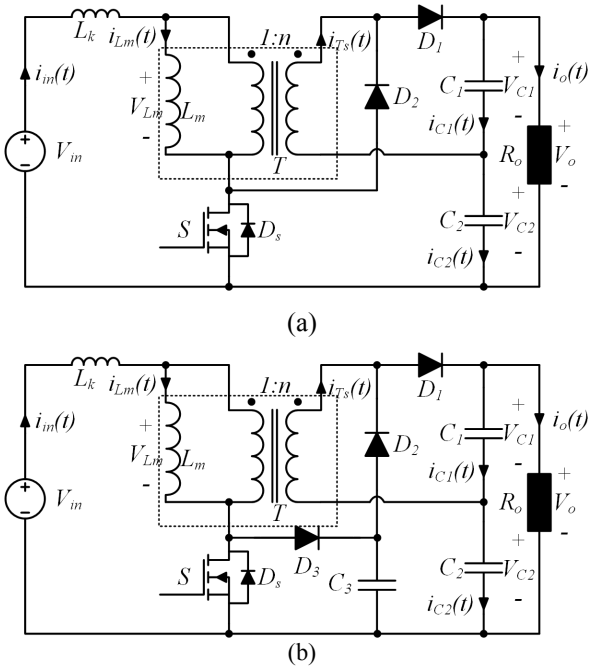

Fig. 1. Proposed topology: (a) Proposed self-clamped high step-up dc-dc converter; (b) alternative proposed high step-up dc-dc converter.

T_s. Then, despite being very similar to the boost-flyback configuration presented by [7], its operation principle, and consequently its mathematical model, are different, thus requiring an exclusive design methodology.

An alternative for reducing the maximum blocking voltage ($V_{DSmax} = V_o$) on the switch S in the circuit shown in Figure 1.a, is by including the capacitor C_3 and the diode D_3, as shown in the Figure 1.b. In this case, compared to the circuit of Figure 1.a, both conduction and switching losses should be lower because R_{DSon} of S is reduced as well as the blocking voltages on all semiconductor devices. However, even though it is an interesting topology which also performs high-step up voltage and high-efficiency, its structure does not satisfy the main scope of this work which it is the use of a circuit made with reduced component counts for applications that requiring output voltage at levels between 400 and 600 volts. Thus, it is possible to employ semiconductor technology previously introduced in the work.

A. Operation Principle in Steady-State

After a detailed analysis of the converter in steady-state, considering the influence of the leakage inductance L_k in the circuit, four operation stages can be verified over a cycle of the switching frequency f_s. During the stages, the following conditions are considered:

1) The voltages across capacitors C_1 and C_2 are assumed constant and ripple-free;

All the semiconductor elements are assumed as ideal;

2) L_k corresponds to the total leakage inductance of the primary and secondary windings.

In the development of the mathematical model that represents the converter behavior in steady state, the following expressions are considered:

$$\Delta t_i = t_i - t_{i-1};\ v_L(t) = L\frac{di_L(t)}{dt};\quad T_s = \frac{1}{f_s};$$
$$\lambda = \frac{L_k}{L_m};\quad M = \frac{V_o}{V_{in}};\ M_{C1} = \frac{V_{C1}}{V_{in}};\ M_{C2} = \frac{V_{C2}}{V_{in}}. \tag{1}$$

Where i is the index that defines the time interval of each stage, which starts at t_{i-1} and ends at t_i.

First operation stage (t_0,t_1): Previous to this stage, switch S and diode D_1 were off, while D_2 was on, thus conditioning C_2 to receive part of energy from the leakage inductance L_k and magnetizing inductance L_m, while C_1 along with L_k and L_m were providing energy to the load. At t_0, S is turned on. From this moment on, the current of L_k (i_{in}) begins to raise linearly, while D_2 is still conducting and D_1 is still blocked. During this interval, C_2 receives energy from input supply V_{in} and from L_m and C_1 supply the load. In this stage, the voltage across L_m is equal to $-V_{C2}/n$, where n is the turns-ratio of primary to secondary windings. This stage ends when the current in L_k equals the current in L_m, and the current in diode D_2 becomes null, and it blocks. Figure 2.a shows this operation stage and equations (2) and (3) the behavior of currents in L_k and L_m, according to Figure 3.

$$I_{k1} = I_{k0} + \left(1 + \frac{M_{C2}}{n}\right)\cdot\frac{V_{in}\cdot\Delta t_1}{\lambda L_m}, \tag{2}$$

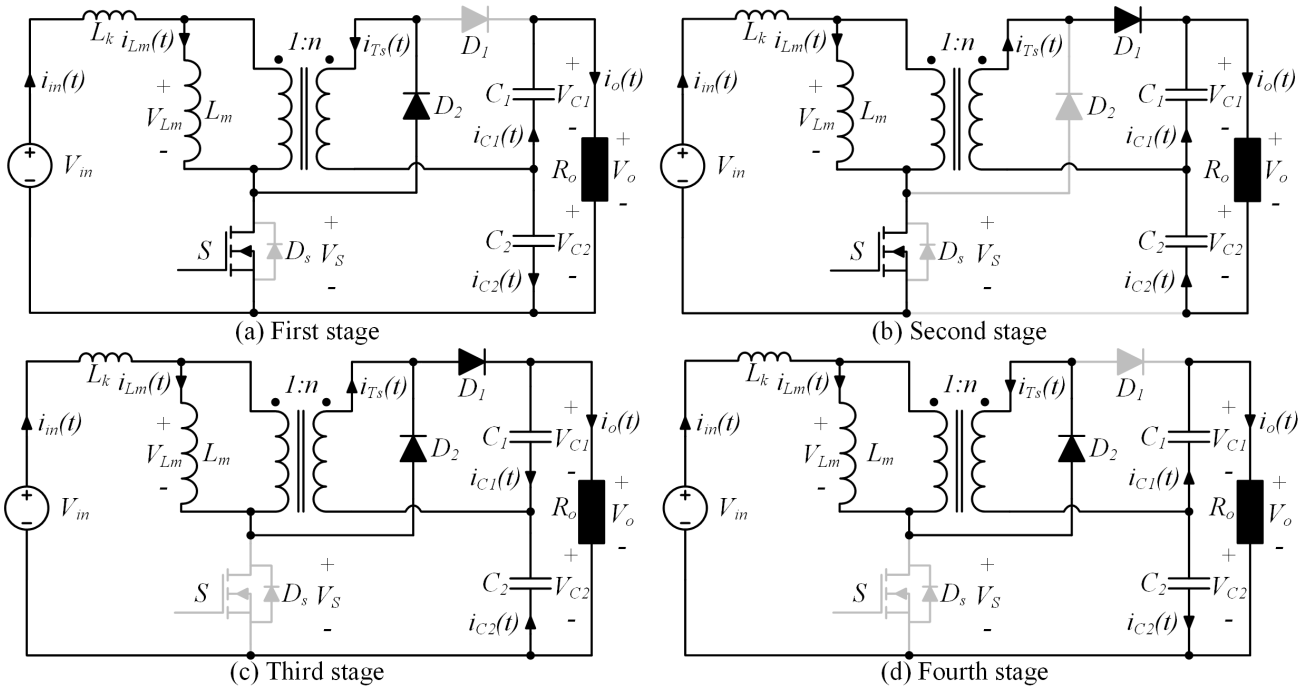

Fig. 2. Operation stages.

$$I_{m1} = I_{m0} - \frac{M_{C2}}{n} \cdot \frac{V_{in} \cdot \Delta t_1}{L_m}. \quad (3)$$

Second operation stage (t1,t2): At t_1, D_2 blocks and D_1 starts conduction. From this moment on, L_m and C_1 receive energy from the input voltage V_{in}, and C_2 provides energy to the load. The voltage across L_m is V_{C1}/n. In this interval, considering the resistance of S (R_{Son}) equal to zero, the leakage inductance L_k stores energy provided by V_{in} and its current increases linearly. Under real operating conditions, the voltage V_{Son} across S might be large enough and the L_k current might decrease rather than increase. This stage ends when S is turned off and D_2 starts conduction again along with D_1. Figure 2.b shows this operation stage and equations (4) and (5) the behavior of currents in L_k and L_m, according to Figure 3.

Third operation stage (t2,t3): At t_2, S turns off and D_2 starts conduction along with D_1, thus ensuring voltage clamping on switch S equal to the output voltage V_o. In this stage, the energy stored in L_k is sent to the capacitors C_1, C_2 and to the load witch also receives energy from V_{in}. During this stage, the voltage across the inductor L_m is still $-V_{C1}/n$. This stage ends when the current of L_k reaches zero, and D_2 blocks. Figure 2.c presents this operation stage and equations (6) and (7) the behavior of currents in L_k and L_m, according to Figure 3.

$$I_{k2} = I_{k1} + \left(1 - \frac{M_{C1}}{n}\right) \cdot \frac{V_{in} \cdot \Delta t_2}{\lambda L_m}, \quad (4)$$

$$I_{m2} = I_{m1} + \frac{M_{C1}}{n} \cdot \frac{V_{in} \cdot \Delta t_2}{L_m}. \quad (5)$$

$$I_{k3} = I_{k2} + \left(1 - M - \frac{M_{C1}}{n}\right) \cdot \frac{V_{in} \cdot \Delta t_3}{\lambda L_m}, \quad (6)$$

$$I_{m3} = I_{m2} + \frac{M_{C1}}{n} \cdot \frac{V_{in} \cdot \Delta t_3}{L_m}. \quad (7)$$

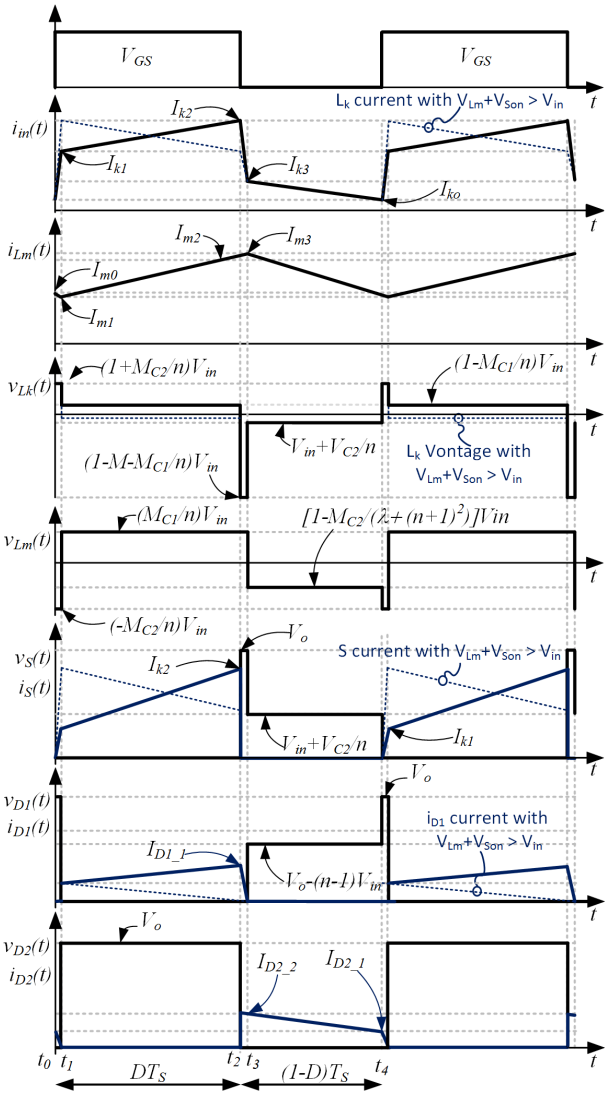

Fig. 3. Theoretical waveforms in steady-state for all four operation stages.

Fourth operation stage (t_3,t_4): At t_3, D_1 blocks and D_2 keeps conducting. The load then receives energy from C_1, while C_2 from L_m. In this stage, the voltage across L_m becomes $-V_{C2}/n$ and the current in L_k is still rising. This stage ends when S is turned on and the first stage starts again. Figure 2.d presents this operation stage and equations (8) and (9) the behavior of the currents in L_k and L_m, according to Figure 3.

$$I_{k0} = I_{k3} + \frac{(1-M_{C2})}{\lambda+(1+n)^2} \cdot \frac{V_{in} \cdot \Delta t_4}{L_m}, \tag{8}$$

$$I_{m0} = I_{m3} + \frac{(1-M_{C2})(1+n)}{\lambda+(1+n)^2} \cdot \frac{V_{in} \cdot \Delta t_4}{L_m}. \tag{9}$$

In short, Figure 3 presents the main theoretical waveforms in steady-state for all four operation stages. Through this graphic, the behavior of the system elements can be observed and, in conjunction with the stages presented in Figure 2, a mathematical model that represents the operation of the proposed converter can be obtained. It is important to observe in the second stage with S turning-on, when condition $V_{Lm}+V_{Son} > V_{in}$ is satisfied, the L_k current slope can be negative.

III. STATIC MODEL

The mathematical model described by equations (2) to (9) defines the fundamental equations of the converter in steady-state. The system has 14 variables, so 14 equations linearly independent are required for solving it. Therefore, in addition to the equations related to the voltages across inductors L_m and L_k under each operation stage and the on and off times of S as function of the duty cycle D presented in equations (10) and (11), a Volt-second balance of inductors L_m and L_k and the Ampère-second balance of capacitors C_1 and C_2 are also needed, provided by equations (12) to (14). The model becomes complete with the sum of voltages across capacitors C_1 and C_2, which are equal to V_o.

$$\Delta t_1 + \Delta t_2 = D \cdot T_s, \tag{10}$$

$$\Delta t_3 + \Delta t_4 = (1-D) \cdot T_s, \tag{11}$$

$$-M_{C2}\Delta t_1 + M_{C1}(\Delta t_2 + \Delta t_3) + \left(\frac{(1-M_{C2})(n+1)n}{\lambda+(n+1)^2} \right) \Delta t_4 = 0, \tag{12}$$

$$\begin{aligned} &(n+M_{C2})\Delta t_1 + (n-M_{C1})(\Delta t_2 + \Delta t_3) + \\ &-M \cdot n\Delta t_3 + \frac{(1-M_{C2})\lambda n}{\lambda+(n+1)^2}\Delta t_4 = 0, \end{aligned} \tag{13}$$

$$\begin{aligned} &n\Delta t_2 \frac{I_{k1}+I_{k2}-I_{m1}-I_{m2}}{2} + n\Delta t_3 \frac{I_{k2}+I_{k3}-I_{m2}-I_{m3}}{2} \\ &-\Delta t_4 \frac{I_{k3}+I_{k0}}{2} + n\Delta t_1 \frac{I_{k0}+I_{k1}-I_{m0}-I_{m1}}{2} = 0, \end{aligned} \tag{14}$$

$$M_{C1} + M_{C2} = M. \tag{15}$$

As can be observed, the obtained equation set is not trivial to solve and does not allow algebraic solution, just numerical. Therefore, in this work a solution is presented assuming the voltages across capacitors C_1 and C_2 are previously known. In this way, by using equations (12) to (14), the time intervals presented in equations (16) to (19) can be derived.

$$\Delta t_1 = \frac{1+MD-M_{C2}}{M} \cdot T_s, \tag{16}$$

$$\Delta t_2 = \frac{M_{C2}-1}{M} \cdot T_s, \tag{17}$$

$$\Delta t_3 = \frac{M_{C2}[D(n+\lambda+1)-\lambda]+Dn(n+1)+\lambda n^2}{(M-1)(n+1)+M_{C1}[n^2(\lambda+1)+n]} \cdot T_s, \tag{18}$$

and

$$\Delta t_4 = \frac{\left[\lambda+(n+1)^2\right]\left[M(1-D)-1\right]}{(M-1)(n+1)+M_{C1}\left[n^2(\lambda+1)+n\right]} \cdot T_s. \tag{19}$$

Once knowing all time intervals Δt_i, the currents which refer to L_k can be derived. So,

$$I_{k0} = \frac{M_{C2}(1+n\lambda)+n}{n^2} \cdot \frac{V_{in} \cdot \Delta t_1}{\lambda L_m}, \tag{20}$$

$$I_{k1} = \frac{M_{C2}(n+\lambda+1)+n(n+1)}{n^2} \cdot \frac{V_{in} \cdot \Delta t_1}{\lambda L_m}, \tag{21}$$

$$I_{k2} = \frac{M_{C2}(n+\lambda+1)+n(n+1)}{n^2} \cdot \frac{V_{in} \cdot \Delta t_1}{\lambda L_m} + -\frac{M_{C1}n+n^2}{n^2} \cdot \frac{V_{in} \cdot \Delta t_2}{\lambda L_m} \tag{22}$$

and

$$I_{d3} = h_2 + \left(1+\lambda n^2 M_{C2}\right)\Delta t_1 + \Delta t_2 + (1-M)\Delta t_3 \cdot \frac{V_{in}}{\lambda L_m}, \tag{23}$$

where

$$h_2 = \left\{\left[M_{C2}(1+n)+n\right]\Delta t_1 - M_{C1}n(\Delta t_2 + \Delta t_3)\right\} \cdot \frac{V_{in}}{n^2}. \tag{24}$$

For solving the whole system, the currents related to L_m need to be obtained too. Therefore,

$$I_{m2} = \frac{M_{C2}(n+\lambda+1)+n(n+1)}{n^2} \cdot \frac{V_{in} \cdot \Delta t_1}{\lambda L_m} + \frac{M_{C1}}{n} \cdot \frac{V_{in} \cdot \Delta t_2}{L_m}. \tag{25}$$

$$I_{m3} = I_{k3}(n+1). \tag{26}$$

After knowing all necessary quantities to define the system elements, we have:

$$L_m = \frac{M_{C1}(\Delta t_2 + \Delta t_3)}{n \cdot \Delta I_{Lm}} \cdot V_{in}, \tag{27}$$

$$C_1 = \frac{(I_{k2}+I_{k3}-I_{m2}-I_{m3}+nI_{k2}+nI_{k3}-2nI_o)\Delta t_3}{2n \cdot \Delta V_{C1}} \tag{28}$$

and

$$C_2 = \frac{(I_{k2}+I_{k3}-2I_o)\Delta t_3}{2\Delta V_{C2}}, \tag{29}$$

where ΔI_{Lm} is the current ripple in L_m, and ΔV_{C1} and ΔV_{C2} the voltage ripples across C_1 and C_2.

It is known that the leakage inductance is influenced by many factors such as core material, turns ratio, winding number, winding technique, tightness between two windings, etc. [27]. That is, the leakage inductance is hard to design except for customization. Hence, in order to verify its influence in the proposed converter, in this work it is assumed that the maximum leakage inductance value is equal to 2 % of L_m. Thus, L_k can be computed through Equation

(1). In practice, the coupled inductor is designed based on the magnetizing inductance, and afterwards the leakage inductance is obtained based on measurements.

A. Static Gain

As presented in the development of the static model, an analytic solution for the system variables could not be obtained. Therefore, the relation between output voltages V_{C1}, V_{C2} and V_o, and the input voltage V_{in}, which define the converter gains M_{C1}, M_{C2} and M, respectively, are presented numerically as function of the duty cycle D for distinct values of n, considering a specific value for λ. In the waveforms presented in Figure 4, a λ=2% is used. Analyzing Figure 4, it is possible to define which operation point the converter must operate. As design procedure, the values for the voltages across capacitors C_1 and C_2 are defined, and the values for n and D can be obtained, or otherwise, obtain the desired voltage values from n and D. In this work, the adopted criterion is to define the operation range where neither D nor n be high in order to achieve a high efficiency of the system

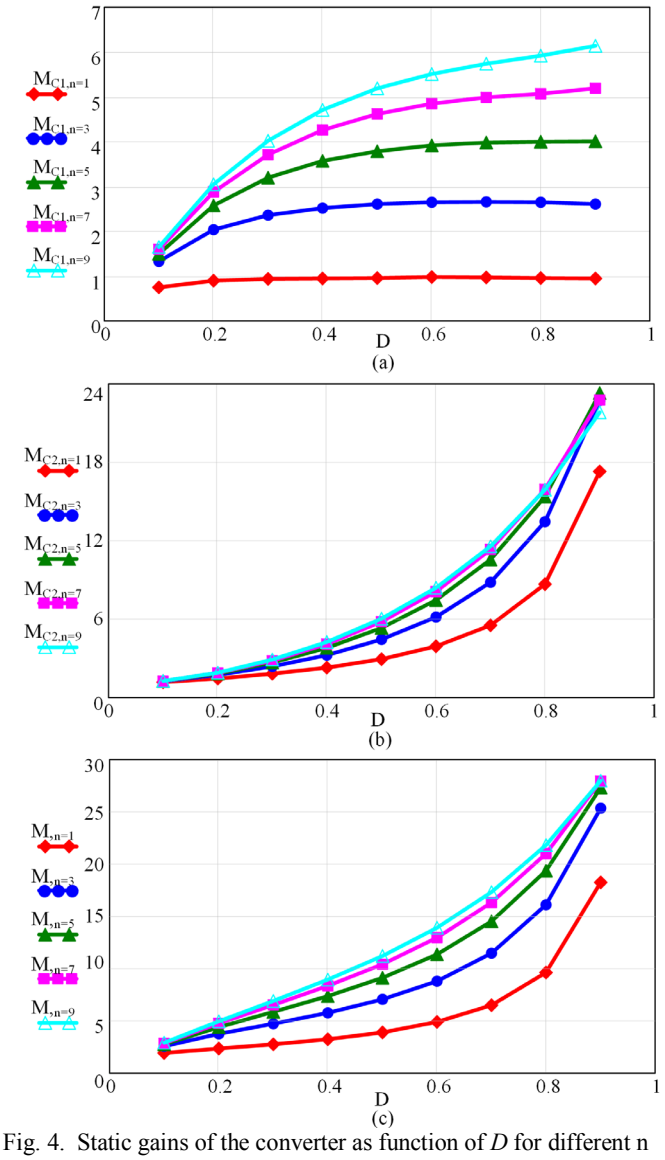

Fig. 4. Static gains of the converter as function of D for different n with λ=2%: (a) M_{C1}; (b) M_{C2}; (c) M.

B. Ideal converter

As discussed previously, when considering the leakage inductance L_k, the static gain of the converter can only be derived from numeric solution. However, it can be demonstrated that the influence of L_k does not affect significantly the total voltage gain M. Therefore, it is also important to present the ideal model of the converter and use it as a design reference for the non-ideal converter. By disregarding inductor L_k, equations for M_{C1}, M_{C2} and M can be defined, as stated in equations (30), (31) and (32). It can be noted that the total gain obtained in Equation (32) is greater than the one presented in [7].

$$M_{C1} = n. \tag{30}$$

$$M_{C2} = 1 + \frac{D(n+1)}{(1-D)} \tag{31}$$

$$M = \frac{n+1}{1-D}. \tag{32}$$

Figure 5 shows the curves of gain M as function of D, for $\lambda = 0$, $\lambda = 1$ % and $\lambda = 2$ %. It can be observed that with duty cycle D neither too high nor too low ($0.2 \le D \le 0.8$), the gain M presents few differences between the ideal and non-ideal models. In such conditions, it can be stated that when the system operates in closed loop these differences can be easily compensated, without large control efforts.

For $\lambda = 0$, equations for L_m, C_1 and C_2 can be derived too, as seen in Eqs. (33), (34) and (35).

$$L_m = \frac{V_{in} D}{\Delta I_{Lm} f_s} \tag{33}$$

$$C_1 = \frac{P_o (1-D)}{M V_{in} \Delta V_{C1} f_s} \tag{34}$$

$$C_2 = \frac{P_o D}{M V_{in} \Delta V_{C2} f_s}. \tag{35}$$

By disregarding L_k, there are no voltage spikes and the blocking voltage levels across the semiconductors during a switching period are:

$$V_{DS} = \left(1 + \frac{M_{C2}}{n}\right) \cdot V_{in} \tag{36}$$

$$V_{D1} = (M - n + 1) \cdot V_{in} \tag{37}$$

$$V_{D2} = M \cdot V_{in}. \tag{38}$$

To finish the theoretical analysis of the proposed

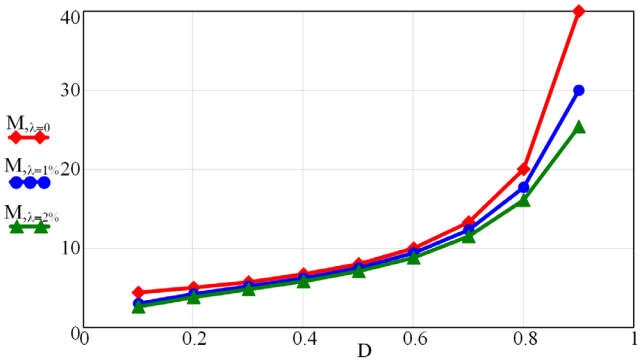

Fig. 5. Static gains of the ideal converter as function of D for λ=0 %, 1% and 2 % with n=3.

Table I
Performance Comparation With Others Single Switch Converters

Coupled-inductor Based Circuit	Ideal Voltage Gain (V_o/V_{in})	Voltage stress on the main switch	No. of Semiconductors		No. of Passive Components		Clamp circuit
			Diode	Switch	Inductor	Capacitor	
Proposed Converter	$\frac{1+n}{1-D}$	$M \cdot V_{in}$	2	1	1	2	No
Converter in [4]	$\frac{1+n}{1-D}$	-	3	1	1	3	No
Converter in [9]	$\frac{1+nD}{1-D}$	$\frac{nD}{1-D} \cdot V_{in}$	2	1	1	2	Yes
Converter in [11]	$\frac{1+nD}{1-D}+n$	$\frac{(M-n)}{1+n} \cdot V_{in}$	4	1	1	4	No
Converter in [18]	$\frac{1+D}{1-D} \cdot n$	$\frac{V_{in}}{1-D}$	3	1	1	3	Yes
Converter in [19]	$\frac{1+D}{1-D} \cdot n$	$\frac{V_{in}}{1-D}$	5	1	2	4	No
Converter in [21]	$\frac{D}{1-D} \cdot (1+n)$	$\frac{V_{in}}{1-D}$	2	1	1	2	Yes

converter, a comparative performance with other converters based on the boost topology employing coupled inductor is presented in the Table I. The chosen initial criteria for comparison are the single switch and the pulsating input current performed by all circuits. The proposed circuit in [4] is based on in [9], however employing voltage multiplier and consequently naturally clamp on diodes, thus the components count is higher. The converters of [9] and [21] have the same components count than the proposed converter, but their voltage gains are lower and a clamp circuit to avoid voltages spikes on the semiconductors is necessary in both circuits. Regarding to the proposed circuits in [11], [18] and [19], all employ more components than the circuit in this work, however the voltage gains are higher.

IV. DYNAMIC MODEL

Through the static model of the converter it is possible to define a design procedure and specify all the elements of the system. However, when external disturbances or a variation on the input voltage occur, to guarantee the output voltage at its nominal value, the converter must operate in closed loop. Therefore, the dynamic model must be developed too. In this work, the derived small-signal model does not consider operation stages 1 and 3, presented in Figure 2, because their time intervals are too small and does not affect significantly the system dynamics. The technique used to derive the small-signal model of the proposed converter is the state-space averaging approach, presented by [32], then the transfer functions can be determined according to equations (39) and (40), which represent the relations $I_{Lm}(s)/D(s)$ and $V_o(s)/I_{Lm}(s)$, respectively. The numeric values in these equations agree with the design values presented in the experimental results. Figure 6 shows the behavior of the system (in red: theoretical results, according to equations (39) and (40); in blue: simulation results) when a disturbance occurs in D, as seen in Figure 6.a, or in I_m, as seen in Figure 6.b. It can be observed that the theoretical results are similar to the simulation results, thus validating the presented dynamic model.

$$\frac{I_{Lm}(s)}{D(s)} = \frac{3.20 \cdot 10^{-19} s^2 + 4.08 \cdot 10^{-5} s + 0.04}{6.25 \cdot 10^{-11} s^2 + 1.86 \cdot 10^{-8} s + 4.83 \cdot 10^{-4}} \quad (39)$$

$$\frac{V_o(s)}{I_{Lm}(s)} = \frac{5.59 \cdot 10^{-17} s^2 + 8.48 \cdot 10^{-5} s + 9.34 \cdot 10^{-4}}{-3.2 \cdot 10^{-19} s^2 + 4.08 \cdot 10^{-5} s + 0.035}. \quad (40)$$

IV. DESIGN PROCEDURE

The main condition considered in the design procedure adopted in this work is to avoid excessive losses both in conduction and in switching. For this, the converter must operate with the duty cycle D neither too high nor too low, even when subjected to an input voltage variation. Therefore,

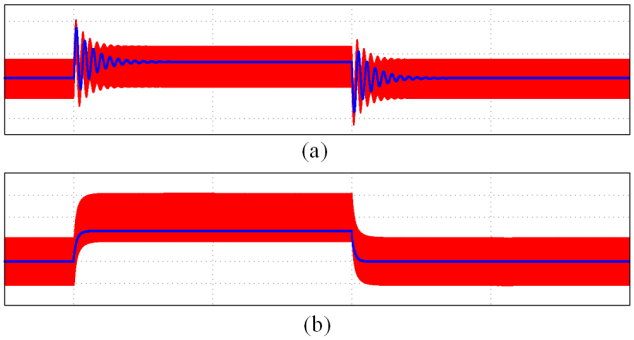

Fig. 6. Dynamic response of the system as function of external disturbances: (a) response of I_{in} as function of a 4% variation in D; (b) response of V_o as function of a 4% variation in I_{in}.

the undermentioned design steps 1 to 6 can be followed to define the parameters of the proposed converter assuming that the input source voltage varies between predefined minimum and maximum values. However, in the case the design considers the non-ideal converter, one must first assume a value for λ. The design procedure follows these steps:

1 – Define the ideal duty cycle D operation range as a function of input voltage source variation ΔV_{in};

2 – Obtain n for the minimum input voltage by using (32);

3 – Calculate ideal M_{C1} and M_{C2} through (30) and (31), respectively;

4 – Assuming a λ value, estimate D_{max} and $D_{mín}$ through Figure 5;

5 – Obtain the system variables presented in equations (16) and (26) by using ideal values for M, M_{C1}, M_{C2} and n;

6 – Calculate non-ideal L_m, C_1 and C_2 using (27), (28) and (29), respectively, for the minimum and maximum values of V_{in} and use the result that has the higher value.

When applying the design data presented in Table II, the converter parameters presented in Table III can be found. From Table III it is possible to specify the semiconductors and obtain the numerical values of the transfer functions to be used in the controller design, according to equations (39) and (40).

Table II
Design Specifications

Parameter	Description	Value
V_{in}	Input Voltage	30 V - 48 V
f_s	Switching frequency	100 kHz
P_o	Output power	300 W
V_o	Output Voltage	400 V
D	Real duty cycle	0.720 – 0.56
λ	Leakage factor	1.8 %
M	Voltage gain	13.33 - 8.33 V
ΔI_{Lm}	Current ripple in L_m	20 % of I_{in}
ΔV_{C1}	Voltage ripple in C_1	1 % of V_{C1}
ΔV_{C2}	Voltage ripple in C_2	1 % of V_{C2}

Table III
Calculated Parameters

Parameter	Ideal Values	Non-ideal Values
n	3	3
M_{C1}	3	2.63 - 2.76
M_{C2}	10.33 - 5.33	10.7 - 5.562
V_{C1}	90 V - 120 V	89.35 - 143 V
V_{C2}	310 V - 280	314 - 261.1~ V
I_{Lm}	10.57 - 6.25 A	6.61~11.12 A
L_m	202 µH	200.2 µH (E65/32/27) n_p=14; n_s=42
C_1	2.55 µF	3 µF
C_2	1.55 µF	2 µF
D_1-D_2	C3D10060A	600 V / 10 A
S	SPW47N60C3	650 V / 47 A

V. EXPERIMENTAL RESULTS

In order to verify the presented design methodology, experimental tests in open loop control were performed in a 300 W prototype of the proposed converter using data presented in TABLE II and III.

Figures 7.a and 7.b present the voltage waveforms on the C_1, C_2 and on the load, for V_{in} = 48 V (Figure 7.a) and V_{in} = 30 V (Figure 7.b). It can be observed that for a low value of V_{in}, V_{C2} increases, because it is directly related to the duty cycle D. On the other hand, V_{C1} decreases, because it depends only on V_{in} and on the turns ratio n.

Figures 8.a and 8.b present the current waveforms in the coupled inductor primary-side winding and in L_m, for V_{in} = 48

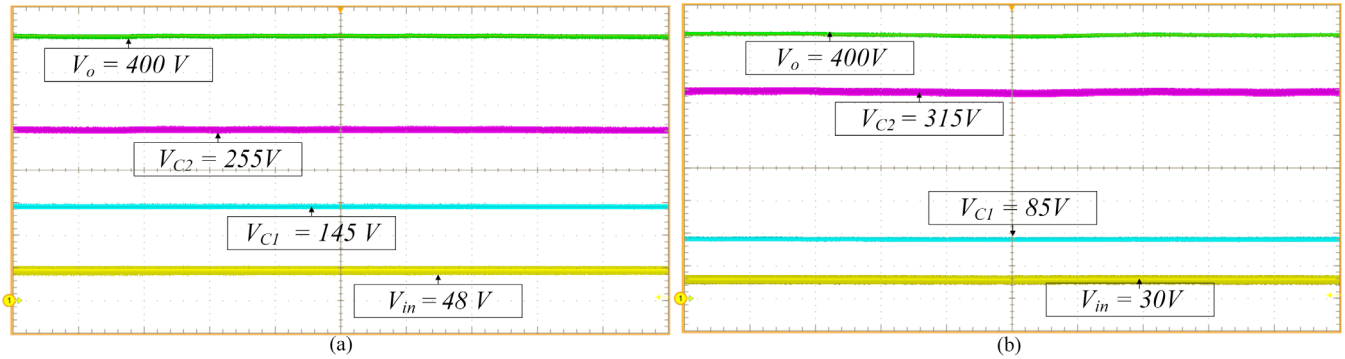

Fig. 7. Voltages on the capacitors C_1 and C_2 and on the load: (a) V_{in} = 48 V; (b) V_{in} = 30 V. (Scales: v = 50 V / div; t = 10 ms / div).

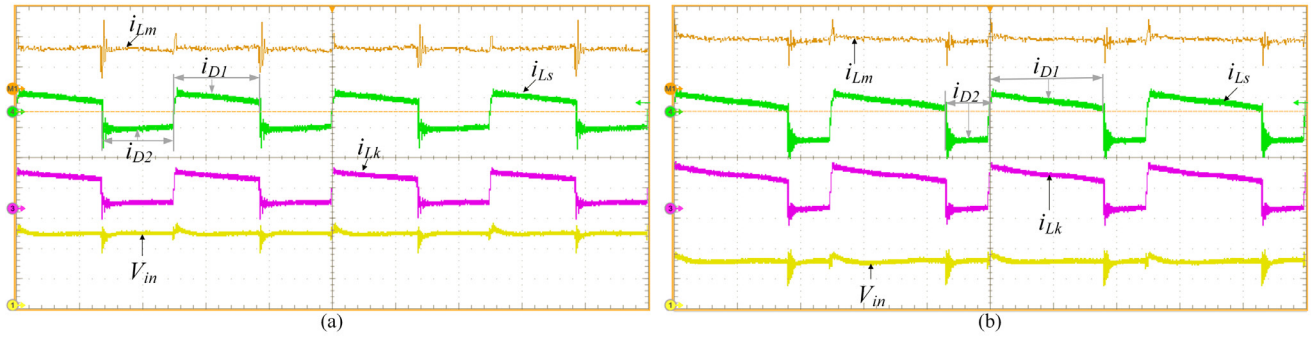

Fig. 8. Currents on inductors L_d, L_s and L_m: (a) V_{in} = 48 V; (b) V_{in} = 30 V. (Scales: CH1 = 50 V / div; CH3 = 10 A / div; M1 = 5 A / div; t = 4 µs / div).

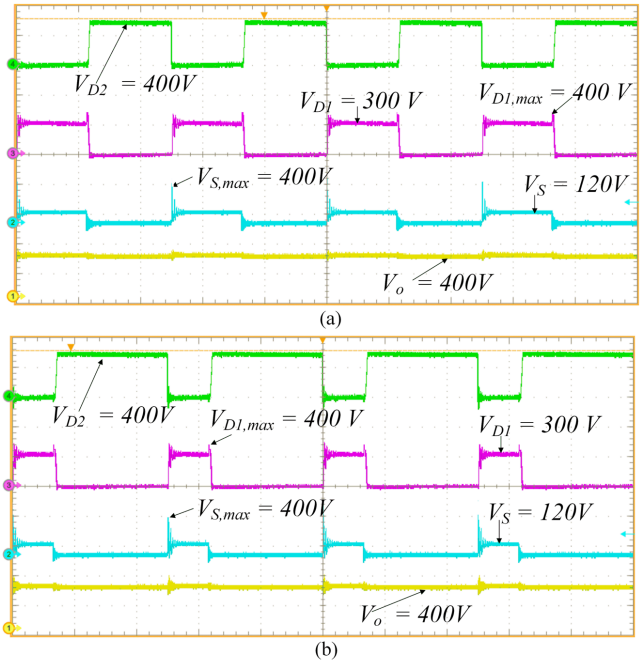

Fig. 9. Voltages across the switches used in the prototype: (a) V_{in} = 48 V; (b)V_{in} = 30 V. (Scales: v = 300 V / div; t = 4 µs / div).

V (Figure 8.a) and V_{in} = 30 V (Figure 8.b). In this measurement, the current i_{Lm} was acquired by using the scope's math resources, where $i_{Lm} = i_{Lk} - i_{Ts} \cdot n$. It can be seen that the converter operates with pulsating current in the input source. Therefore, in applications where a considerably high voltage gain is required, the efficiency may be impaired. Figures 9.a and 9.b show the waveforms of the voltages on the semiconductors S, D_1 and D_2 and on the load, for V_{in} = 48 V (Figure 9.a) and V_{in} = 30 V (Figure 9.b). It can be observed that none of the voltage spikes exceed the output value (400 V) and the blocking voltage values are close to those defined by (36), thus contributing to enhance the overall efficiency.

Figure 10 demonstrates the switching instants on S. Even though the ZVS not being achieved, as can be seen in the Figure 10.a, the switching losses are low because in the region which there are simultaneous voltage and current, both values are low and the transient time is too short. As can be observed in the Figure 10.b, the switching losses are more expressive during turn-off instant time and the voltage spike on the switch is around 400 V.

Figure 11 presents the system efficiency measured with a Yokogawa W500 precision wattmeter. As can be noted, the efficiency of the converter operating with V_{in} = 30 V is not so high when compared to the result obtained for 48 V that has presented a maximum efficiency of 95.2 %.

The efficiency curve under duty cycle D variation is presented in the Figure 12 witch along with Figure 11 suggests that the proposed topology is more indicated for applications where extreme duty cycle values must be avoided to increase the system static gain. However, it may be necessary to carry out a more precise evaluation in the process of energy transference between input and output stages analysing the influence of the turns ratio n where it should be considered that its increase implies in more leakage inductance and consequently in a lower static gain. Thus, to maintain the output voltage, the duty cycle should

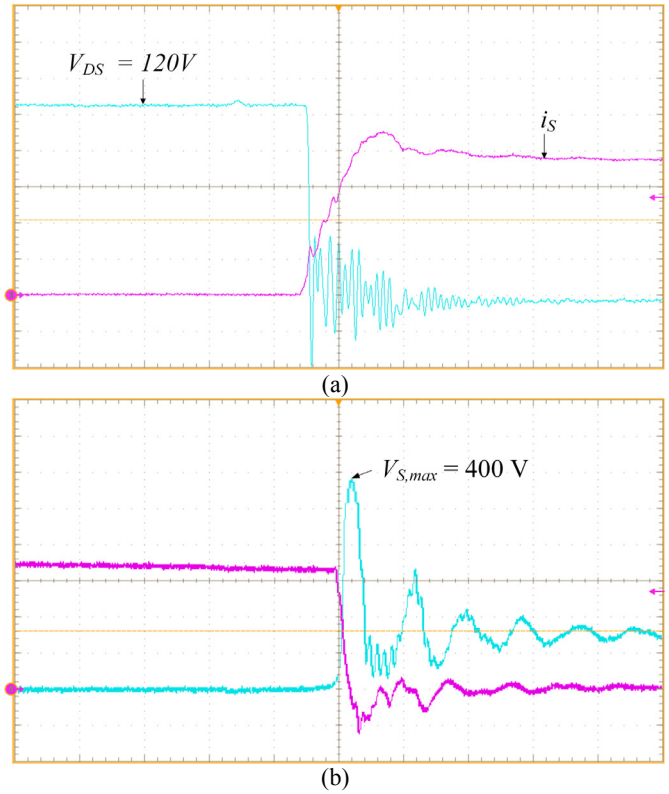

Fig. 10. Turn-on and turn-off transient instants of switch S. (Scales: (a):v = 20 V / div; i: = 3 A / div; t = 160 ns / div); (b):v = 70 V / div; i: = 3 A / div; t = 160 ns / div);

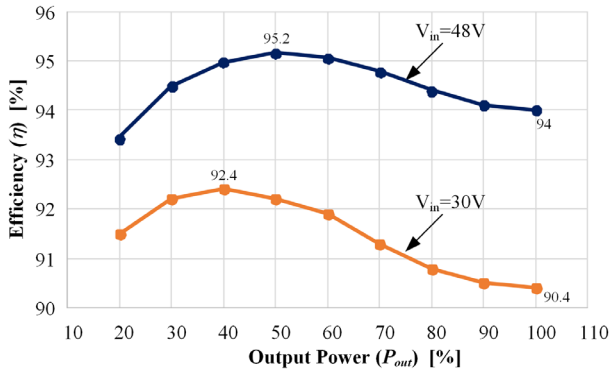

Fig. 11. Efficiency curves as function of the variation of the output power.

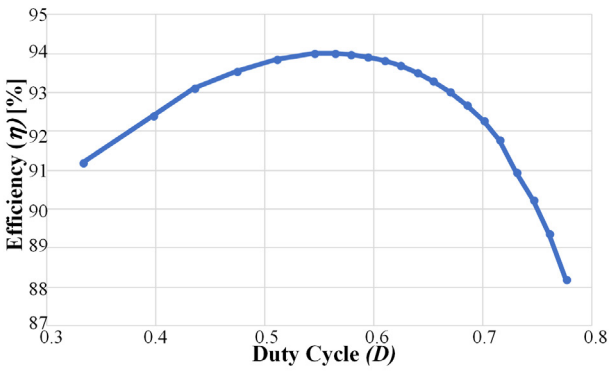

Fig. 12. Efficiency curve as function of the variation of the duty cycle D.

also be increased. On the other hand, no doubt that conduction losses are predominant for any input voltage

level, indicating that the proposed circuit presented in Figure 1.b can be a good solution to improve the overall system efficiency, even for low and high duty cycle values.

VI. CONCLUSION

This paper presents a high-voltage-gain dc-dc converter based on the boost converter employing coupled inductor. The main positive characteristics of the proposed topology is the elevated efficiency, natural voltage clamping in all semiconductors without using snubber circuits and reduced component count. The negative characteristics are the pulsating current on the input source which require a filter on applications that need reduced current ripple, and the maximum voltage spikes on semiconductors are equal to the output voltage.

From the operation stages and waveforms in steady state, considering the leakage inductance influence, a mathematical analysis was developed, thus the static and dynamic models of the converter were obtained. These models are required to specify all elements employed in the power circuit as well as to design control. The ideal converter model was also introduced and it can be observed that within a range operation of the duty cycle, there is no relevant influence of the leakage inductance, allowing the converter to be designed employing its ideal model. Thus, the design procedure can be considerably simplified without significant influence on the results.

Aiming to validate the proposed design methodology, experimental results in open loop control with a prototype of 300 W output power, 400 V output voltage and input voltage range of 30 V to 48 V, with the converter operating at 100 kHz were presented. Examining the efficiency curves obtained from measurement on the prototype, one can see that the best converter performance occurs for a voltage around 48 V, when maximum and nominal efficiencies of 95.2 % and 94 %, respectively, were achieved.

The obtained results show that the voltage spikes on all semiconductors were clamped with its maximum value equal to the output voltage, demonstrating that no auxiliary clamping circuits are necessary. Furthermore, new technologies of semiconductors, such as CoolMOS™, can easily handle such voltage levels, like the observed ones.

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