HIGH-VOLTAGE-GAIN INTEGRATED BOOST-SEPIC DC-DC CONVERTER FOR RENEWABLE ENERGY APPLICATIONS

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Abstract – This paper presents the analysis of a non-isolated high-voltage-gain single-switch dc-dc converter based on the integration of the boost and SEPIC topologies. The converter employs a voltage multiplier at the output of the SEPIC stage, which is connected in series with the output of the boost stage, aiming a high step-up ratio operation with limited duty cycle values. An accurate steady state analysis considering the influence of the leakage inductance of the SEPIC coupled inductor in the energy transfer process is detailed in the paper. The several theoretical results are then used to derive a design methodology for the circuit. Experimental results for a 500 W, 48 V input voltage, 400 V output voltage, 96.3% peak efficiency and 100 kHz switching frequency prototype are provided to demonstrate the feasibility of the proposed scheme and to validate the mathematical analysis carried out.

Keywords – High voltage gain, integrated boost-SEPIC, snubberless converter, renewable energy systems.

I. INTRODUCTION

According to the U.S. EIA (Energy Information Administration), the worldwide energy consumption will be increased by approximately 30% until 2040. Non-renewable sources, such as natural gas, coal and oil, are responsible for 70% of the overall energy production. In addition to the concern with energy scarcity due to the limited availability of the sources, fossil resources are also known to have the negative impact of polluting the environment and thus contributing for global warming [1]. Although fossil resources remain as the predominant energy sources in the present, it is expected that the energy production from renewable sources increases at the average rate of 2.3% per year until 2040 [1]. In this sense, it is crucial that the electronic systems used for energy processing exhibit an increased efficiency and reduced cost.

Concerning renewable sources, such as fuel cell and photovoltaic, systems processing power levels in the order of hundreds of Watts are usual and energy is made available at low voltage levels. Therefore, dc-dc converters operating with high voltage gain become a necessity. In this sense, it is known that the conventional boost converter would be the straightforward choice for non-isolated applications, but its efficiency tends to be drastically reduced as the voltage gain is increased [2]–[4]. In order to overcome this issue, numerous solutions have been proposed in the literature [2]–[27]. As addressed in [2]–[4], most of them are based on the boost converter using a two-winding coupled inductor for achieving a high step-up ratio with limited duty cycle values. However, some problems related to the blocking voltage on the semiconductors and high input current ripple can reduce the overall system performance and increase the component count. According to [3], the key characteristics of a high step-up dc-dc converter for renewable energy applications are: (a) high efficiency; (b) low component count; (c) reduced cost and size; and (d) low-ripple input current. Aiming to meet the most these characteristics, high-voltage gain dc-dc converters based on the SEPIC have been proposed, as can be seen in [5]–[14]. The circuits proposed in [7],[10],[12]–[14] employ coupled inductor and voltage multiplier cells to obtain high-voltage gain, while in [5],[8],[9],[11] only coupled inductor is used. Other examples of high step-up dc-dc converters based on the conventional boost or SEPIC converters can be found in [15]–[25]. In [16], the boost-flyback converter is proposed, which requires a dissipative circuit to clamp the voltage on the output diode and also a high number of turns ratio to achieve high voltage gain. The boost-based circuits introduced in [17]–[19] also employ voltage multiplier cells, while the topologies presented in [20]–[25] use more than one active switch to perform interleaved operation ([20]–[22]) and soft switching on the devices ([23]–[25]). In [26], a high efficiency two-switch buck-based solution exhibiting a linear voltage gain and with soft-switching capability was proposed. Another two-switch topology was introduced in [27], based on the conventional boost-flyback converter.

In the circuit presented in this work, which has been previously studied in [7] employing a quasi-resonant strategy, the blocking voltage of all semiconductors is naturally clamped, thus not requiring the addition of auxiliary snubber or clamping circuits in a practical implementation.

A detailed qualitative and quantitative description of the circuit operation is provided in this paper, along with a step-by-step design procedure and experimental verification of the key theoretical results. Finally, the analysis is validated through experimental tests performed with a 500 W prototype operating at a switching frequency of 100 kHz.

II. HIGH-VOLTAGE-GAIN BOOST-SEPIC DC-DC CONVERTER

The power stage of the high step-up boost-SEPIC dc-dc converter using a voltage multiplier cell (IBS-VM), firstly introduced in [7] under a quasi-resonant operation, is shown in Figure 1. The circuit is the result of the integration
between the boost and SEPIC topologies, in which the shared elements are the input inductor $L_m$ and the switch $S$. The elements $C_1$, $C_2$, $C_3$, $C_4$, $T$, $D_1$ and $D_2$ compose the remaining SEPIC stage, while $D_3$ completes the boost segment.

In addition to increasing the voltage gain, this configuration prevents voltage ringing to occur on diodes $D_1$ and $D_2$, since their blocking voltages are clamped by capacitors $C_2$ and $C_3$. Hence, no additional snubber or clamping circuit must be included in the system to limit the voltage spikes on these components. It is also noteworthy that using the voltage multiplier configuration completely changes the operating principle of the coupled inductor $T$, given that the average value of its magnetizing current must be null at steady state. Consequently, the coupled inductor operates as a conventional transformer and do not require gap to prevent core saturation.

III. OPERATING PRINCIPLE AT STEADY STATE

In order to perform the analyses performed in this paper, two simplifying assumptions are made:

1) The voltages on $C_1$, $C_2$, $C_3$, $C_4$ and the current through $L_m$ are considered ripple free (treated as constants);
2) All semiconductors are treated as ideal elements.

The qualitative analysis of the IBS-VM converter reveals the existence of five distinct operating stages within a switching cycle in the continuous conduction mode (CCM), as depicted in Figure 2. The CCM operation in the IBS-VM converter is defined on $i_{Lm}$, which never becomes null during the switching period. A brief explanation on each operating stage is given as follows:

**First stage ($t_0$ to $t_1$) [cf., Figure 2(a)]:** starts when the switch $S$ is turned on at $t = t_0$. The input voltage source transfers energy to $L_m$ and the inductance $L_k$ is discharged. Energy is also being transferred to the output capacitor $C_2$. As soon as $L_k$ is completely discharged, this stage ends.

**Second stage ($t_1$ to $t_2$) [cf., Figure 2(b)]:** as soon as $i_k$ has its direction reversed, at the beginning of the second stage, diode $D_1$ blocks and $D_2$ becomes forward biased. In this stage, energy is still transferred to $L_m$. Regarding the output stage, only $C_3$ receives energy. At $t = t_2$, the switch $S$ is turned-off, thus finishing this stage.

**Third stage ($t_2$ to $t_3$) [cf., Figure 2(c)]:** the blocking of $S$ makes diode $D_1$ to become forward biased. This stage is of great importance in the converter operation, since it prevents the leakage inductance of the transformer to generate a voltage spike on the switch by providing a current path towards the output capacitor $C_4$. This stage is completed when $i_k$ becomes positive.

**Fourth stage ($t_3$ to $t_4$) [cf., Figure 2(d)]:** at $t = t_3$, $i_k$ becomes positive, implying that $D_1$ and $D_2$ become forward and reverse biased, respectively. During this stage, energy is transferred to the output capacitors $C_2$ and $C_4$. At $t = t_4$, $D_1$ blocks since $i_k$ becomes equivalent to $i_{Lm}$, thus finishing the fourth stage.

**Fifth stage ($t_4$ to $t_5$) [cf., Figure 2(e)]:** during fifth and last operating stage, the current through $L_k$ is maintained equal to $I_m$. The only output capacitor receiving energy is $C_2$. As soon as the switch $S$ is turned on, this stage ends and the switching cycle is over.

Based on the description of the five steady-state operating stages of the converter, whose equivalent circuits are
presented in Figure 2, one can derive the voltage/current waveforms on every element of the circuit. The key waveforms regarding the operation of the IBS-VM converter at steady state are given in Figure 3.

IV. MATHEMATICAL ANALYSIS AT STEADY STATE

In this section, an accurate mathematical analysis considering the influence of the leakage inductance $L_k$ in the energy transfer process is performed for the converter using the proposed non-resonant scheme. This accurate analysis provides the means to quantify the influence of $L_k$ on the static gain and to demonstrate that $D_1$, $D_2$ and $D_3$ turn off with ZCS. Some initial definitions are made as follows:

$$
\Delta t_k = t_k - t_{k-1} : f_s = \frac{1}{T_s} ; \alpha = \frac{f_s L_k}{R_o} ; \\
M = \frac{V_o}{V_m} ; q_2 = \frac{V_{C2}}{V_m} ; q_1 = \frac{V_{C1}}{V_m} ; q_4 = \frac{V_{C4}}{V_m}.
$$

Where: $\Delta t_k$ corresponds to the duration of the $k$th operating stage; $T_s$ and $f_s$ refer to the switching period and switching frequency, respectively; $\alpha$ is a factor involving the switching frequency, the leakage inductance $L_k$ and the output resistance $R_o$; $M$ is the static gain and $q_2$, $q_1$ and $q_4$ are the partial static gains.

On analyzing the five operating stages, one can determine the set of equations

$$
I_{in} = \frac{(nV_m + V_{C2})}{nL_k} \Delta t_1 = 0, \\
I_{i,min} = -\frac{(nV_m - V_{C3})}{nL_k} \Delta t_2 = 0, \\
I_{i,max} = -\frac{(nV_m - V_{C4})}{nL_k} \Delta t_3 = 0, \\
I_{o} = -\frac{(nV_m - V_{C4} - V_{C3})}{nL_k} \Delta t_4 = 0
$$

and

$$
I_{i} = -\frac{(nV_m - V_{C4} - V_{C2})}{nL_k} \Delta t_5 = 0
$$

that must hold whenever the converter operates at steady state, where $n$ corresponds to the primary to secondary number of turns ratio of the transformer. The parameters $I_{in}$ and $I_{i,min}$ are unknown current levels indicated in Figure 3 to be determined at the end of the analysis. Similarly, the partial output voltages $V_{C2}$, $V_{C3}$ and $V_{C4}$ are unknowns to be found in order to completely quantify the steady-state energy transfer behavior of the IBS-VM converter.

The output voltage can be varied by means of duty cycle adjustment in the pulse-width-modulation (PWM) applied to the switch $S$. From the key waveforms depicted in Figure 3, it is possible to verify that

$$
\Delta t_1 + \Delta t_2 = \frac{D}{f_s}
$$

and

$$
\Delta t_3 + \Delta t_4 + \Delta t_5 = \frac{(1-D)}{f_s}
$$

relate the durations of the five operating stages of the IBS-VM converter with the duty cycle set in the PWM.

The last set of equations necessary to solve the problem is obtained from the Volt-second balance on the magnetizing inductance $L_m$ and the Ampère-second balance on the output capacitors $C_2$, $C_3$ and $C_4$ as given by

$$
V_{C2} (\Delta t_1 + \Delta t_2 + \Delta t_3) - V_{C3} (\Delta t_3 + \Delta t_5) = 0
$$

and

$$
in_{I_m} (2 \Delta t_1 + \Delta t_4) + n_{I_{i,max}} \Delta t_3 + \\
- \Delta t_5 (\Delta t_1 + \Delta t_4 + 2 \Delta t_2) = 0
$$

in order to guarantee that the average value of the voltages on $L_m$, $L_k$ and $L_o$ are all null in steady state.

Finally, in general, it is interesting to have the results in terms of the output voltage, which is

$$
V_o = V_{C2} + V_{C3} + V_{C4}
$$

in this converter, given that the output capacitors are associated in series.

On solving the system formed by the set of equations (2)–(10) and (12), the values of $I_{in}$, $I_{i,min}$, $V_{C2}$, $V_{C3}$, $V_{C4}$, $\Delta t_1$, $\Delta t_2$, $\Delta t_3$, $\Delta t_4$ and $\Delta t_5$ can be calculated and a complete mathematical description of the converter is achieved. However, given the extension of the solution, the results are not provided in this paper, but with the aid of a computer software one could easily solve the equations for any set of parameters.

Finally, the average value of the output current is given by

$$
I_o = \frac{V_o}{R_o} = \frac{1}{f_s} \left[ \frac{1}{2} I_{in} (2 \Delta t_1 + \Delta t_4) + I_{i,max} \Delta t_3 \right].
$$

At this point, it is important to mention that further analyses, such as voltage/current stresses, conduction losses, switching losses, small-signal dynamic modeling and even an optimization of the converter would require these results to be carried out. However, they are not performed in this paper for the reason of being beyond the scope of this research.

A. Input Current Ripple

The choice of $I_{in}$ has a direct impact on the input current ripple, as given by
\[ \Delta V_{\text{in}} = \frac{DV_{\text{in}}}{f_1 I_{1n}} \]  

(14)

Therefore, it is possible to determine the value of \( I_{\text{in}} \) such that input current ripple is limited to some desired value, which is an important theoretical result for the adequate design of the converter.

**B. Voltage Ripples on \( C_1, C_2, C_3 \) and \( C_4 \)**

In this section, the voltage ripples on the capacitors contained in the power stage of IBS-VM converter are derived. These results are fundamental to determine the capacitance values that keep the voltage ripples limited to maximum specified values. It is noteworthy that the voltage ripples on \( C_2, C_3 \) and \( C_4 \) depend on the load characteristics, which is here considered purely resistive. However, based on the content of this paper, the reader can easily derive these ripples for other kinds of load.

The voltage ripple on \( C_1 \) is computed based on the current waveform depicted in Figure 4. The highlighted area is the region correspondent to the discharge of \( C_1 \). Thus, the voltage ripple \( \Delta V_{C_1} \) can be determined by

\[ \Delta V_{C_1} = -\int_{t_1}^{t_2} dv_{C_1} = -\frac{1}{C_1} \int_{t_1}^{t_2} i_{C_1} dt = -\frac{(A_1 + A_2)}{C_1}. \]  

(15)

Computing the values of the areas \( A_1 \) and \( A_2 \) and substituting the values of \( I_{\text{in,min}}, \Delta t_2 \) and \( \Delta t_1 \) into (15) yields

\[ \Delta V_{C_1\%} = \frac{\Delta V_{C_1}}{V_{\text{in}}} = \frac{q_2^2}{2n^2 f_1^2 L_1 C_1 q_1 (q_2 + q_1)^2}, \]  

(16)

which provides the voltage ripple on \( C_1 \) as a percentage of the input voltage \( V_{\text{in}} \) and in terms of the definitions established in (1).

By proceeding in a similar way, the voltage ripples on \( C_2, C_3 \) and \( C_4 \) can be computed. Figure 4 also presents the waveforms of the currents through \( C_2, C_3 \) and \( C_4 \), highlighting the charging regions of these capacitors. The analysis of these waveforms results in the percent voltage ripples given by

\[ \Delta V_{C_{1\%}} = \frac{\Delta V_{C_2}}{V_{\text{in}}} = \frac{n}{2C_2 I_{\text{in}} V_{\text{in}}} \left( \frac{I_{\text{in,min}} - I_0}{n} \right)^2 (\Delta t_2 + \Delta t_3) + \frac{2I_{\text{in}}}{2C_1 I_{\text{in}} V_{\text{in}}} \Delta t_4, \]  

(17)

\[ \Delta V_{C_{3\%}} = \frac{\Delta V_{C_3}}{V_{\text{in}}} = \frac{n}{2C_3 I_{\text{in}} V_{\text{in}}} \left( \frac{I_{\text{in,min}} - I_0}{n} \right)^2 (\Delta t_2 + \Delta t_3) \]  

(18)

and

\[ \Delta V_{C_{4\%}} = \frac{\Delta V_{C_4}}{V_{\text{in}}} = \frac{n}{2C_4 I_{\text{in}} V_{\text{in}}} \left( \frac{I_{\text{in,min}} - I_0}{n} \right)^2 (\Delta t_2 + \Delta t_3) + \frac{1}{2C_1 I_{\text{in}} V_{\text{in}}} \Delta t_4. \]  

(19)

where: \( I_0 \) corresponds to the constant output current drained by the output resistance \( R_{\text{os}} \).

The results (17) and (18) could also be written in terms of the definitions established in (1). However, due to the extension of the resulting equations, they are provided in terms of the auxiliary parameters used in the mathematical analysis.

**C. Static Gain**

On solving the set of equations (2)–(10) and (12), it is possible do demonstrate that the ideal static gain (considering \( \alpha \to 0 \)) of the IBS-VM converter is given by

\[ M_{\text{ideal}} = \frac{1 + n}{1 - D}. \]  

(20)

There is no closed-form solution for the static gain of the IBS-VM converter considering nonzero values for \( L_k \). However, with the aid of a computer program, the set of equations provided in the mathematical analysis can be solved and the static gain can be evaluated for any operating condition.

In order to demonstrate how \( L_k \) affects the static gain, some graphs are provided next. It is noteworthy that the load characteristic and switching frequency have influence on the static gain whenever \( L_k \neq 0 \). It means that \( M \) is also dependent on the values of \( R_{os} \) and \( f_s \), and consequently on \( \alpha \), in addition to \( D \) and \( n \). Figure 5 shows static gain curves for some values of \( \alpha \) considering \( n = 2 \), which is drawn from the numerical solution of the system formed by the set of equations (2)–(10) and (12).

**D. ZCS on Diodes \( D_1, D_2 \) and \( D_s \)**

The existence of the inductance \( L_s \) in the circuit allows

Fig. 5. Static gain curves versus duty cycle for some values of \( \alpha \) considering \( n = 2 \).
limiting the derivatives of the current through the coupled inductor. Consequently, the slew rates of the currents on $D_1$ and $D_2$ are also limited. It means that if $L_0$ is high enough, ZCS is achieved on these diodes. In order to verify the switching conditions on $D_1$ and $D_2$, the slew rate of the current through these elements must be computed prior to their blocking. The blocking of $D_1$ and $D_2$ occurs at the end of the first and third stages, respectively. The slew rate (SR) of their current prior to the blocking event is given by

$$SR_{D1} = \frac{\left(nV_m + V_{c2}\right)}{n^2L_0} \tag{21}$$

and

$$SR_{D2} = \frac{\left(nV_m - nV_m + V_{c3}\right)}{n^2L_0} \tag{22}$$

respectively.

The same reasoning applies to $D_3$, the current of which decreases with a slew rate of

$$SR_{D3} = \frac{\left(nV_m - nV_m - V_{c2}\right)}{nL_2} \tag{23}$$

before it turns off at the end of the fourth stage.

The results (21)–(23) allow the designer to verify whether the switching losses of $D_1$, $D_2$ and $D_3$ are as low as desired. If these losses must be further reduced, a small external inductor can be added to the circuit to lower the slew rate of the currents through the diodes. Alternatively, the coupled inductor could have its construction oriented to increasing the currents through the diodes. In order to verify the ZCS is achieved on these diodes. In order to verify the existence of a single switch and low-ripple input current performed by all circuits. The converters of [10] and [11] have the same components count, voltage gains and voltage stress on the main switch of the IBS-VM converter, but the sum of the voltage stress on the diodes of [11] is higher. Comparing only with [10], the sum of the energy stored in the four capacitors is lower in the IBS-VM converter, and thus the proposed solution potentially requires a lower volume of capacitive elements. Regarding the circuits proposed in [12] and [13], they employ more components than the IBS circuit studied in this work, however their voltage gains are higher. Both circuits present lower voltages stress on the main switch, while the sum of the voltages on the diodes of [12] and [13] is similar and higher than that verified in the IBS-VM converter, respectively.

V. STEP-BY-STEP DESIGN METHODOLOGY

In this section, a step-by-step design procedure for the high step-up integrated boost-SEPIC converter based on the mathematical analysis performed in section IV is detailed. This is done by gathering the main results derived in section IV and then proposing sequential steps to determine the values of the converter’s parameters that meet a set of design specifications. The suggested steps are as follows:

1) Specify the desired distribution of the output voltage $V_o$ between the partials $V_{c2}$, $V_{c3}$ and $V_{c4}$ in accordance with (12);
2) Find $I_{in}$, $I_{min}$, $\Delta t_1$, $\Delta t_2$, $\Delta t_3$ and $\Delta t_4$ in terms of $D$, $n$ and $L_4$ using the set of equations (2)–(8);
3) Solve numerically the system of equations (9), (10) and (13) and determine the values of $D$, $n$ and $L_4$ that satisfy the design specifications;
4) Calculate the value of $L_{in}$ using (14);
5) Compute the values of $C_1$, $C_2$, $C_3$ and $C_4$ using (16), (17), (18) and (19), respectively;
6) Determine the RMS values of voltages and currents on the primary and secondary windings of the coupled inductor $T$. The voltages can be determined from the analysis of the equivalent circuits provided in Figure 2 and the current stresses can be computed from the waveform of $i_d$ depicted in Figure 3. These values are necessary to the physical design.

### TABLE I

Comparison with Other SEPIC Based Single-Switch Converters

<table>
<thead>
<tr>
<th>Boost-SEPIC Based Circuit</th>
<th>Ideal Voltage Gain ($V_o/V_{in}$)</th>
<th>Voltage Stress on the Main Switch</th>
<th>$\Sigma V_{diodes}$</th>
<th>No. of Diodes</th>
<th>No. of Passive Components</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBS-VM [7]</td>
<td>$\frac{1+n}{1-D}$</td>
<td>$\frac{M+V_o}{1+n}$</td>
<td>$(1+2n)\frac{V_o}{1+n}$</td>
<td>3</td>
<td>1 single 1 coupled 4</td>
</tr>
<tr>
<td>in [10]</td>
<td>$\frac{1+n}{1-D}$</td>
<td>$\frac{M+V_o}{1+n}$</td>
<td>$\frac{(1+2n)M}{1+n}$</td>
<td>3</td>
<td>1 single 1 coupled 4</td>
</tr>
<tr>
<td>in [11]</td>
<td>$\frac{1+n}{1-D}$</td>
<td>$\frac{M+V_o}{1+n}$</td>
<td>$&gt;2MV_o$</td>
<td>3</td>
<td>1 single 1 coupled 4</td>
</tr>
<tr>
<td>in [12]</td>
<td>$\frac{2+n+D}{1-D}$</td>
<td>$\frac{M+V_o}{3+n}$</td>
<td>$\frac{(3+2n)(M+1)}{3+n}$</td>
<td>4</td>
<td>1 single 1 coupled 5</td>
</tr>
<tr>
<td>in [13]</td>
<td>$\frac{2+n+D(1-n)}{1-D}$</td>
<td>$\frac{M+V_o+1}{1+2n}$</td>
<td>$\frac{(5+3n)(M+n+1)}{1+2n}$</td>
<td>4</td>
<td>1 single 1 coupled 5</td>
</tr>
</tbody>
</table>
of this magnetic element;
7) Calculate the voltage and current stresses on the semiconductors using the several results obtained from the theoretical analysis (the equations regarding the stresses have not been included in section IV due to their extension).

VI. EXPERIMENTAL RESULTS
Aiming to validate the theoretical analysis carried out, a 500 W prototype of the IBS-VM converter with the specifications listed in Table II was built and tested in laboratory. The design procedure discussed in the previous section was used to determine the parameters values shown in Table III. It is noteworthy that including an external inductance to increase the value of \( L_e \) lead to a slight modification on the distribution of the output voltage between \( V_{C2} \), \( V_{C3} \) and \( V_{C4} \), as highlighted in Table II. Figure 6 exhibits a picture of the IBS-VM converter prototype built for the experimental tests.

Key experimental waveforms were taken at the nominal operating condition to validate the theoretical analysis performed in this paper. Output voltage and current and input voltage and current waveforms are depicted in Figure 7(a), in which an input current ripple of 24% is verified. The output voltage \( V_o \) and its respective partials \( V_{C2} \), \( V_{C3} \) and \( V_{C4} \) are shown in Figure 7(b). Measurements indicate 154.4 V, 136.6 V and 110 V for \( V_{C2} \), \( V_{C3} \) and \( V_{C4} \), respectively, which are close to their specified values. As can be seen in Figure 7 (c), a duty cycle value of 0.558 was necessary to ensure the operation with a constant output voltage value of 400 V, being this value higher than the 0.518 predicted in the theoretical analysis. This difference is due to the losses on the components that have been disregarded in the mathematical analysis. The blocking voltages \( V_s \), \( V_{D1} \), \( V_{D2} \) and the currents \( i_s \), \( i_{D1} \), \( i_{D2} \) and \( i_{D3} \) are shown in Figure 8(a) to Figure 8 (c). A higher voltage spike in \( V_s \) is observed on Figure 8(a) than in Figure 7(c), since a wire loop was inserted in the prototype to acquire the waveform of \( i_s \).

TABLE II
Design Specifications for the 500 W Prototype of the IBS-VM Converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{in} )</td>
<td>500 W</td>
</tr>
<tr>
<td>( V_{in} )</td>
<td>48 V</td>
</tr>
<tr>
<td>( V_r )</td>
<td>400 V</td>
</tr>
<tr>
<td>( V_{C2} )</td>
<td>150 V (151 V)*</td>
</tr>
<tr>
<td>( V_{C3} )</td>
<td>150 V (137 V)*</td>
</tr>
<tr>
<td>( V_{C4} )</td>
<td>100 V (112 V)*</td>
</tr>
<tr>
<td>( f_r )</td>
<td>100 kHz</td>
</tr>
<tr>
<td>( \Delta I_{LV} )</td>
<td>20%</td>
</tr>
<tr>
<td>( \Delta V_{LV} )</td>
<td>10%</td>
</tr>
<tr>
<td>( \Delta V_{CM} )</td>
<td>2%</td>
</tr>
<tr>
<td>( \Delta V_{CM} )</td>
<td>2%</td>
</tr>
<tr>
<td>( \Delta V_{CM} )</td>
<td>1%</td>
</tr>
</tbody>
</table>

*Values considering the inclusion of an external inductance of 1 \( \mu \)H to increase \( L_e \).

TABLE III
Parameters Values for the 500 W Prototype of the IBS-VM Converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M )</td>
<td>8.333</td>
</tr>
<tr>
<td>( q_1 )</td>
<td>3.146</td>
</tr>
<tr>
<td>( q_2 )</td>
<td>2.854</td>
</tr>
<tr>
<td>( q_3 )</td>
<td>2.331</td>
</tr>
<tr>
<td>( n )</td>
<td>3.25</td>
</tr>
<tr>
<td>( D )</td>
<td>0.518</td>
</tr>
<tr>
<td>( L_{so} )</td>
<td>113 ( \mu )H, APA401P69</td>
</tr>
<tr>
<td>( L_e )</td>
<td>2.3 ( \mu )H (leakage of the primary winding of ( T ) + an external inductance of 1 ( \mu )H)</td>
</tr>
<tr>
<td>( T )</td>
<td>ETD39, 3C95, 8/26 turns, Litz 38AWG, ( L_{so} = 301 ) ( \mu )H</td>
</tr>
<tr>
<td>( C_1 )</td>
<td>9.4 ( \mu )F (2 x 4.7 ( \mu )F in parallel)</td>
</tr>
<tr>
<td>( C_{2e}, C_7 )</td>
<td>2.2 ( \mu )F</td>
</tr>
<tr>
<td>( C_{3e}, C_4 )</td>
<td>3 ( \mu )F (2 x 1.5 ( \mu )F in parallel)</td>
</tr>
<tr>
<td>( D_1, D_2 )</td>
<td>STTH20R04</td>
</tr>
<tr>
<td>( D_3 )</td>
<td>MBR40250TG</td>
</tr>
<tr>
<td>( S )</td>
<td>IRFP4668PBF</td>
</tr>
</tbody>
</table>

Fig. 6. Picture of the 500 W IBS-VM prototype built to perform the

Fig. 7. Key experimental results at \( P_{in} = 500 \) W: (a) Input voltage \( V_{in} \), input current \( i_{in} \), output voltage \( V_r \) and output current \( i_r \); (b) output voltage \( V_o \) and partial output voltages \( V_{C2}, V_{C3} \) and \( V_{C4} \); (c) drain-to-source voltage \( V_S \) and gate-to-source voltage \( V_{GS} \) on \( S \).
The measurements indicate $SR_{D1} = -17.65\ \text{A}/\mu\text{s}$, $SR_{D2} = -16.67\ \text{A}/\mu\text{s}$ and $SR_{D3} = -5.1\ \text{A}/\mu\text{s}$, while the theoretical predictions are $-12.64\ \text{A}/\mu\text{s}$, $-14.20\ \text{A}/\mu\text{s}$ and $-7.6\ \text{A}/\mu\text{s}$, respectively. The difference observed can be justified by the voltage ripple on $C_1$ and on the parasitic elements that have been disregarded during the analysis. However, the theoretical predictions are sufficiently accurate to serve as the basis to guarantee ZCS on $D_1$, $D_2$ and $D_3$ during the design of the IBS-VM converter. Well behaved waveforms were verified for $V_{D1}$ and $V_{D2}$ without adding any auxiliary clamping circuit to the converter, being this a key difference between the proposed solution and the conventional integrated boost-SEPIC converter presented in [5]. It is important to observe that the blocking voltage of every semiconductor has a lower value than the output voltage (400 V).

Figure 9(a) presents the voltage on $C_1$ along with the input voltage, proving the validity of (11). It also verified that the ripple on $V_{C1}$ is in accordance with the design specifications. The waveform of the current through $L_k$ is depicted in Figure 9(b). Some resonance is observed in this waveform caused by the existence of a nonzero voltage ripple on $C_1$, which has been disregarded in the theoretical analysis. However, this resonance plays a minor role in the energy transfer process, given the good agreement between the measurements and the design specifications.

Finally, efficiency measurements for several values of output power are shown in Figure 10. The measurements were performed maintaining the output voltage fixed at 400 V. A maximum efficiency of 96.3% was observed at 40% of the rated output power. At nominal conditions, the converter exhibited an efficiency level of 95.3%. It is noteworthy that the efficiency is above 94.9% for the entire range of 10-100% of output power. In order to verify the performance of the IBS-VM converter under input voltage variations,
In this paper, the operation of a snubberless high-voltage-gain dc-dc converter based on the integrated boost-SEPIC was investigated. Differently from the conventional IBS converter reported in [5], the use of a voltage multiplier cell at the output of the SEPIC stage enables the circuit to operate with a higher voltage gain and also prevents the coupled inductor to have a dc level on its magnetizing current. Moreover, the leakage inductance of the coupled inductor, which usually generates voltage spikes during switching in many coupled-inductor based converters, plays an important role in providing ZCS to diodes $D_1$ and $D_2$ in the IBS-VM converter.

An accurate mathematical analysis considering the influence of the leakage inductance on the energy transfer process was detailed. Based on these results, the designer is able to determine the set of parameters that ensures the operation of the IBS-VM converter under pre-specified conditions. Moreover, the results could be used for an optimized converter design, since they provide the basis to compute all voltage and current stresses on the elements of the circuit. Experimental results validated the theoretical analysis and demonstrated the good performance of the IBS-VM converter over a wide output power range.

Overall, the IBS-VM converter using a voltage multiplier cell has demonstrated potential for application in systems requiring a high-step-up dc-dc converter at power levels of hundreds of Watts, mainly due to its low input current ripple, high voltage gain with reduced duty cycle levels, high efficiency and need for only a single active switch.

VII. CONCLUSION

The efficiency measurements were taken considering an input voltage range of 30–48 V and $P_{out} = 500$ W, as depicted in Figure 11. As expected, an efficiency drop is verified as the input voltage is decreased due to higher current stresses. The efficiency values were obtained using the precision power analyzer Yokogawa WT500 and the waveforms depicted in Figures 7, 8 and 9 were acquired with the digital oscilloscope Tektronix DPO 7254.

REFERENCES


BIOGRAPHIES

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