ASYMMETRICAL MULTILEVEL HYBRID INVERTER - ANALYSIS AND EXPERIMENTATION

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***Abstract* – This paper describes a voltage-fed asymmetrical hybrid inverter based on a symmetrical hybrid multilevel DC-AC converter for high voltage/high power applications. The proposed inverter is controlled by two types of modulation patterns: low frequency (single pulse) and high frequency (sinusoidal PWM), responsible for obtaining a reduced harmonic distortion in the output voltage. Furthermore, the converter is asymmetrically powered, being fed by two sources with distinct values, obtaining seven levels phase voltage output. The results are presented with two pulse width modulation strategies, aimed at reducing the harmonic distortion in the voltage output. The operation of single-phase and three-phase circuits was verified by means of simulations and results obtained with an experimental prototype operating at a frequency switching of 1.5 kHz with a fundamental frequency of 50 Hz.**

***Keywords* – Asymmetrical multilevel converters, DC-AC converters, Hybrid inverters, Modulation.**

NOMENCLATURE

4LSC	Four level switching cell.
A_m	Modulating signal amplitude.
CSV	Centered space vector.
f_c	Commutation frequency.
f_m	Modulating signal fundamental Frequency.
GTO	Gate turn-off thyristor.
IGBT	Insulated gate bipolar transistor.
IGCT	Integrated gate-commutated thyristor.
$J(\cdot)$	Bessel function.
L_o	Load inductance.
m_i	Modulation index.
P_o	Output power.
PD	Phase disposition.
R_o	Load resistance.
RMS	Root mean square.
S_x	Electronic switch x.
THD	Total harmonic distortion.
V_{ab}	Phase-to-phase voltage.
V_{an}	Phase-to-neutral voltage.
V_M	Modulating signal.
V_t	Carrier signal.

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I. INTRODUCTION

Over the past few decades, the use of multilevel inverters for high voltage applications has become popular. Lipo and Manjrekar [1] were the first to present the asymmetrical hybrid multilevel topology.

It is widely known that multilevel inverters are appropriate for medium voltage (600 V–69 kV) and high voltage (69 kV–230 kV) applications due to the reduced voltage stress on the semiconductor devices involved in the energy conversion [2]–[10].

Asymmetrical multilevel inverters can achieve a higher number of voltage levels with a reduced number of semiconductors when compared to symmetrical topologies, as the number of levels increases at an exponential rate when DC buses with different voltage values are employed. However, these differences in the bus voltage lead to different levels of voltage and current stresses in semiconductor devices, especially in motor driver applications, where the modulation index has a wide excursion range. This drawback can be overcome in symmetrical multilevel converters with a proper modulation strategy, as all DC voltages are equal and the converter has higher redundancy, i.e., a higher number of different switching states which results in the same output voltage.

The main advantage of an asymmetrical converter is the higher number of voltage levels when compared to a symmetrical converter with the same topology, which implies in a reduced number of redundant states. Resulting in a reduction in the total harmonic distortion (THD) of the output voltage, assuming an adequate modulation strategy is employed.

The proposed voltage source inverter belongs to the hybrid multilevel family, i.e., it combines distinct semiconductor technologies (for instance, MOSFET, IGBT and GTO). Also, it is said to be asymmetrical due to the employment of DC voltage sources with different values. Hence, this paper proposes a circuit where the voltage sources have binary values. In comparison to the topology described by Lipo and Manjrekar' [1], the number of semiconductors of the proposed topology increases at a lower rate compared to the number of levels, and there is a single insulated DC voltage source for each phase.

The proposed topology has been described in a previous publication [11], operating with the phase disposition (PD) modulation. In this paper, a centered space vector (CSV) modulation is also proposed for the asymmetrical multilevel

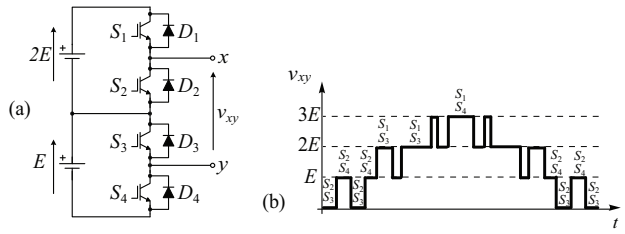

Fig. 1. (a) Bidirectional four-level dc-dc switching cell (4LSC) and (b) waveform voltage to the cell four levels.

inverter, and a comparison of the two modulation schemes is provided.

The topology in this study represents an alternative to those discrebed in [1] and [12]. Two different pulse width modulation (PWM) strategies are proposed: level-shifted phase disposition (PD-PWM) [13] and the centered space vector (CSV-PWM) [14], [15].

The proposed topology is suitable for high power and medium/high voltage applications, with a motor drive or medium voltage line compensator.

II. PROPOSED CIRCUIT DERIVATION

In [16], a topology derived from a three-level voltage DC-DC buck converter is proposed. The current proposal differs from the classical three-level buck converter cell since asymmetrical voltage sources are used. Figure 1(a) shows the topology and the distribution of the asymmetrical voltage sources.

In general, the voltage synthesized by the inverter is governed by equation (1), where n is the quantity of sources employing the bidirectional four-level DC-DC switching cells (Figure 1(a)) with an increasing value for the source voltage (E, $2E$, $4E\ldots$).

$$L = 3 \cdot n + 1 \tag{1}$$

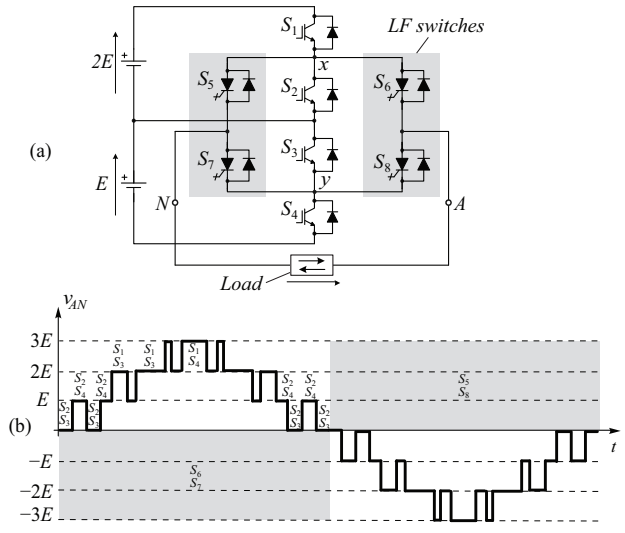

Fig. 2. (a) Single-phase asymmetrical multilevel inverter. (b) The waveform of the load voltage.

III. ASYMMETRICAL HYBRID MULTILEVEL INVERTER

A. Single-phase seven-level inverter

The waveform obtained at the output of the bidirectional 4-level DC-DC switching cell (4LSC), between points x and y, varies from 0 to $3E$ with discrete voltage levels (with voltage steps equal to E).

Figure 1(b) shows the voltage obtained on the 4LSC. To obtain the AC voltage, an H-bridge inverter is connected between points x and y, as shown in Figure 2(a). With an adequate modulation strategy, an AC output signal between points A and N is obtained. The switches S_1, S_2, S_3, and S_4 generate a multilevel unipolar waveform, while the switches S_5, S_6, S_7, and S_8 generate an alternate output for each switching period of the switches. Figure 2(b) shows the output signal for this inverter, obtaining seven levels of voltage.

Similarly to the multilevel hybrid symmetrical inverter [16] the switches S_5, S_6, S_7, and S_8 support the total bus voltage ($3E$), while in 4LSC the switches S_1, S_2 support a voltage of $2E$ and S_3, S_4 support a voltage of E.

The advantage is that the switches S_1, S_2, S_3, and S_4 can operate at high frequencies with lower voltage levels, and thus MOSFETs or IGBTs can be employed. On the other hand, S_5, S_6, S_7 and S_8 operate with higher voltage levels, but at low frequency (load frequency), and so slower switches, like GTOs or IGTCs, are employed.

B. Modulation Strategy

In general, inverters employ pulse width modulation (PWM), and it is necessary to compare a modulating signal (V_M) with a carrier (V_t). Usually, for $'m'$ level voltage inverters $m-1$ carriers are required. Every carrier is defined with the same frequency (f_c) and the same peak-to-peak amplitude (A_c). The modulating signal amplitude is defined as A_m with frequency f_m. The basic principle of PWM involves continuously comparing the modulating signal (reference) with the carriers. When the modulating signal is greater than the carrier the output signal is high and when it is smaller than the carrier the output signal is low.

Equation (2) provides the conventional modulation index, when there is only one carrier, for instance, in two level converters, while the modulation index given by equation (3) relates to multilevel modulation, considering the amplitude of multiple carriers (typically level-shifted) with respect to the modulating signal. This index (m_a) is always between one and zero.

$$m_i = \frac{A_m}{A_c} \tag{2}$$

$$m_a = \frac{A_m}{(m-1)A_c} \tag{3}$$

Figure 3 shows the PD-PWM strategy. Figure 3(a) shows the carriers and modulating signal and Figure 3(b) the gate pulses for the switches S_1, S_3 and S_5.

In order to generate the correct output voltage, given in Table I, which shows the voltage output based on the converter switching state, a logical circuit is implemented employing

TABLE I
Switching States and Voltage Levels

$S_1, \bar{S_3}$	$S_3, \bar{S_4}$	$S_5, S_6, \bar{S_7}, \bar{S_8}$	V_{xy}
1	0	1	+3E
1	1	1	+2E
0	0	1	+E
0	1	1	+0
0	1	0	+0
1	1	0	-E
0	0	0	-2E
1	0	0	-3E

'exclusive-ors' as shown in Figure 3(c), which is responsible for generating the gate signal to trigger the switches.

For certain modulation index values it is not possible to maintain all of the voltage levels in the load. This occurs when the modulating signal has a lower amplitude than n-1 times the amplitude of the carriers. Equation (4) defines the minimum modulation index ($m_{a_{min}}$), that can be obtained in a seven-level inverter.

$$m_{a_{min}} = \frac{m-3}{m-1} \tag{4}$$

For the proposed seven-level inverter, the minimum index of modulation occurs at 0.66, when it loses two voltage leves (one positive and one negative). When the modulation index become smaller than 0.33, it loses two more levels, and in this case the output voltage has only three levels.

There is another concept, involving the frequency ratio given by equation (5), and this is defined as the frequency ratio of the carriers with respect to the modulator. This index is always greater than one.

$$m_f = \frac{f_c}{f_m} \tag{5}$$

For the modulation strategy, the PWM sinusoidal modulation technique with level-shifted phase disposition (PD) [13], [17] was used, which requires $m-1$ carriers to obtain m voltage at the cell output. Each one of these carriers

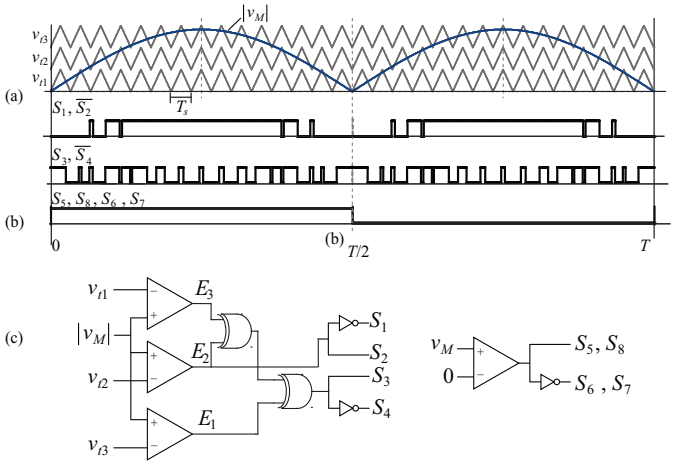

Fig. 3. Modulation strategy - (a) carriers and modulating signal, (b) gate pulses and (c) modulation logic circuit.

TABLE II
Amplitude of the Load Voltage Harmonic Components

Harmonic	Amplitude	Frequency
Fundamental A_1	$A_1 = Em_i$	ω_1
Components $A_{n,v}$ $n = 2,4,6\ldots$	$\frac{2E}{n\cdot\pi} \cdot J_n(v, n\cdot\pi\cdot m_i)$	$(v\omega_1 \pm n\omega_s)$

is in phase, but the level is shifted with an offset equal to its maximum amplitude value.

C. Three-phase extension

Figure 4 shows the three-phase extension of the proposed converter. The modulating signal for each phase is shifted by 120 electrical degrees generating the three-phase voltage output.

Seven voltage levels can be generated per converter leg, namely: $-3E$, $-2E$, $-E$, 0, $+E$, $+2E$ and $+3E$ as seen in Table I. Thus, as in this case of a cascaded full-bridge converter, 127 space vectors (cf. Figure 5) can be generated by the three-phase system.

IV. SPECTRAL ANALYSIS OF THE LOAD VOLTAGES

A. PD-PWM Single-Phase Load Voltage Analysis

In order to analytically define the harmonic spectrum of the load voltage and its THD, this section shows the derivation of the expressions for both phase voltage (v_{an}) and line voltage (v_{ab}). In this analysis it was assumed that the carriers have a 120 degree delay between each other. It can be observed that the mathematical outcomes provide a good approximation with the results obtained. Simulation and experimental results are provided, showing the validity of the analysis. From the analysis, based on [16], the load voltage was obtained for the single-phase multilevel converter, which is given by:

$$v_{an}(t) = E\,m\sin(\omega_1 t) + \sum_n \sum_v \frac{2E}{n\pi} J_n(v, n\pi m_i)\,[\sin(v\,\omega_1 t + n\,\omega_s t) + \sin(v\,\omega_1 t - n\,\omega_s t)], \tag{6}$$

Where $J(\cdot)$ represents the Bessel function of v order.

In equation (6), it can be noted that harmonic components exist in side-bands ($v\omega_1$) around multiples of the switching frequency ($n\omega_s$).

Figure 6(a) is a plot of the previous equation normalized with respect to E. The peak amplitude of the harmonic components of the inverter output voltage and their harmonic frequencies are given in Table II and are graphically shown as a function of the modulation index *mi*. The harmonics components are obtained from $h = n \cdot m_f \pm v$.

B. PD-PWM Three-Phase Load Voltage Analysis

The analysis was also carried out for the line voltages, to obtain an expression for them. The expression that defines line-to-line voltage is given by equation (7).

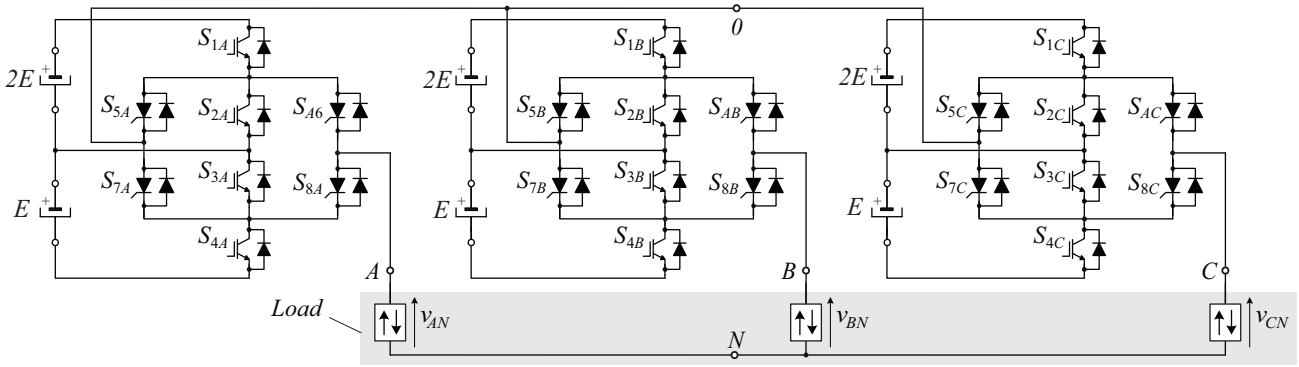

Fig. 4. Proposed three-phase asymmetrical hybrid seven-level DC-AC converter.

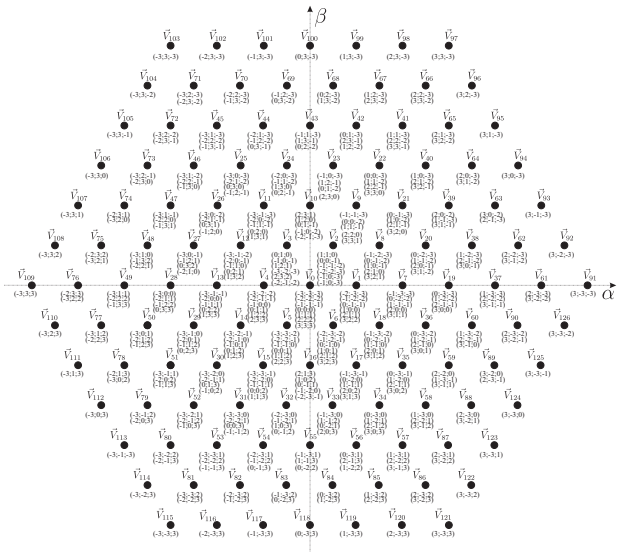

Fig. 5. Space vector diagram for the proposed three-phase asymmetrical hybrid seven-level DC-AC converter.

$$v_{ab}(t) = \sqrt{3}\sin\left(\omega_1 t - \frac{\pi}{6}\right) + \sum_{n=1}^{\infty}\sum_{v=1}^{\infty}\frac{2}{n\pi}J_v(n\pi m_i)\left[N_P\sin(v\omega_1 t + n\omega_s t + \alpha_P) + N_N\sin(v\omega_1 t - n\omega_s t + \alpha_N)\right], \quad (7)$$

with $n = 1,2,3,\ldots$; $v = 1,3,5,\ldots$;

$$N_P = \sqrt{2(1-\cos\gamma(v+n))}, \quad (8)$$

$$N_N = \sqrt{2(1-\cos\gamma(v-n))}, \quad (9)$$

$$\alpha_P = \arctan\left[-\cot(\gamma(\frac{v+n}{2}))\right], \quad (10)$$

$$\alpha_N = \arctan\left[-\cot(\gamma(\frac{v-n}{2}))\right], \quad (11)$$

$$\gamma = \frac{2}{3}\pi.$$

Figure 6(b) shows a plot of equation (7) normalized with respect to E. The peak amplitude of the harmonic components of the line-to-line voltage and their frequencies can be seen in Table III and are displayed as a function of the modulation index m_i.

TABLE III
Amplitude of the line-to-line voltage harmonic components

Harmonic	Amplitude	Frequency
Fundamental A_1	$A_1 = \sqrt{3}Em_i$	ω_l
Components $B_{n,v}, A_{n,v}$	$A_{n,v} = \frac{2E}{n\pi}\cdot\lvert J_v(v, n\cdot\pi\cdot m_i)\rvert N_P$	$(v\omega_1 + n\omega_s)$
$n = 1,2,3\ldots$ $v = 1,3,5\ldots$	$B_{n,v} = \frac{2E}{n\pi}\cdot\lvert J_v(v, n\cdot\pi\cdot m_i)\rvert N_N$	$(v\omega_1 - n\omega_s)$

Also, the total harmonic distortion expressions were determined from the single-phase and line-to-line voltage expressions. Equation (12) gives the THD for the line-to-line voltage and equation (13) the THD for the single-phase load voltage and the results are reported in Figure 7(a) and (b). Although the plots are similar, a lower distortion in the line voltage compared with the phase voltage can be observed.

$$THDV_{UV} = 100\cdot\sqrt{\sum_n\sum_V\frac{(\frac{2}{n\pi}\cdot J_n)^2\cdot(N_P^2+N_N^2)}{(\sqrt{3}\cdot m_i)^2}} \quad (12)$$

$$THDV_{UN} = 100\cdot\sqrt{\sum_n\sum_V\frac{(\frac{2}{n\pi}\cdot J_n)^2\cdot(M_P^2+M_N^2)}{(\frac{1}{3}\cdot m_i)^2}} \quad (13)$$

Where $J_n = J_n(v,n,\pi,m_i)$, $N_P = N_P(v,n)$, $N_N = N_N(v,n)$, $M_P = M_P(v,n)$ and $M_N = M_N(v,n)$.

C. Centered Space Vector (CSV) Modulation

The centered space vector PWM originates from the study reported in [14], [15], and consists of having $N-1$ carrier signals with the same amplitude, frequency and phase, where N represents the number of levels of the inverter. The reference signals are superposed over the carrier signals, and the intersection point of the two signals determines the voltage level of the switches at the output, for each transition cycle or operating state.

The phase disposition modulation can be extended to $CSV-PWM$, initially adding an offset that contains all of the zero sequence components for the voltage references, V_k, $(k = a,b,c)$ and thus:

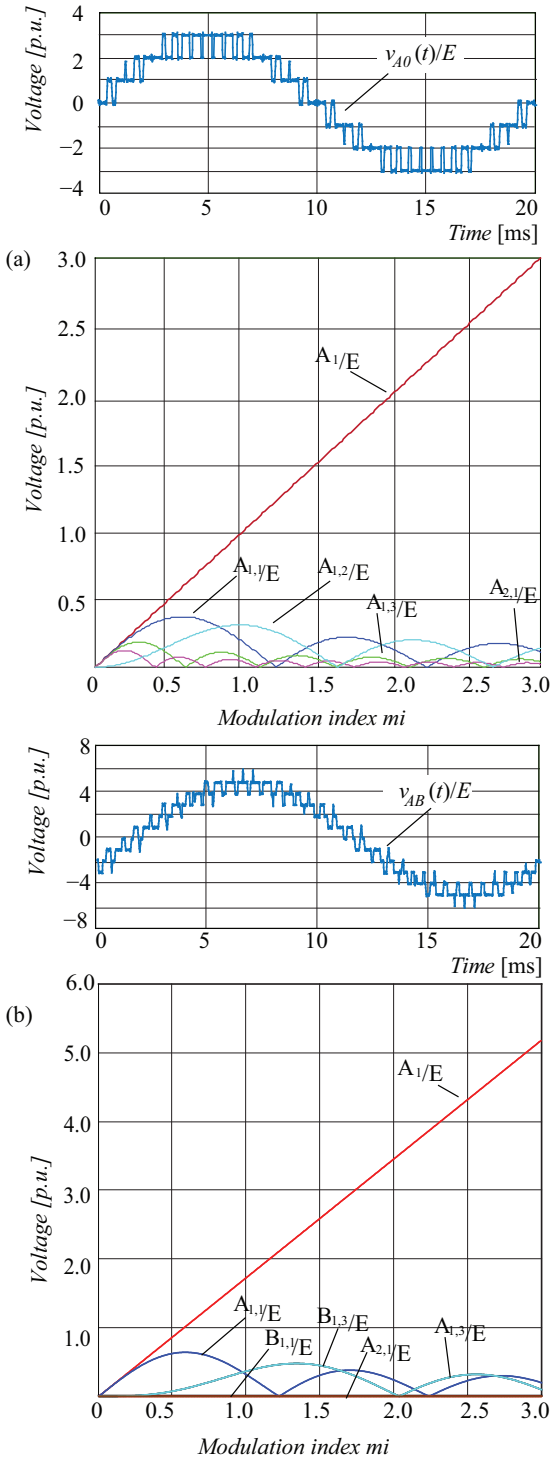

Fig. 6. (a) Single-phase output voltage of the inverter for mf = 32, graph obtained from equation (6), taking account up to n=30 and v=31, i.e., h = 991 and the amplitude of the harmonic components of the voltage V_{AB}: A1 = fundamental component, An; v= frequency harmonic; n = 2;4;6;... v = 1;3;5;... It can be seen that $A_{1,1}$ represents the harmonics h = 31 and 33, these being the lower order. (b) Line-to-line voltage of the inverter for mf =32, graph obtained from equation (7), taking account up to n = 100 and v = 41, i.e., h = 3241 and amplitude of the harmonic components of the line-to-line voltage inverter: A1 = fundamental component, $A_{n,v}$ = harmonics at the frequency, $B_{n,v}$ = ; n = 2;4;6...; v = 1;3;5;... $A_{1,1}$ represents the harmonic 33 and $B_{1,1}$ the harmonic 31.

$$V'_k = V_k - \frac{[\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)]}{2} \tag{14}$$

A modulus function that identifies which of the reference signals is responsible for the first and last transition is given by:

$$V''_k = \left[V'_k + \frac{(N-1)V_{DC}}{2}\right] mod(V_{DC}) \tag{15}$$

Equation (15) is used because in multilevel inverters it is necessary to identify which reference signal is responsible for the beginning of the vector sequence that is present in each semi-cycle of the carrier signal.

The absolute value of the offset guarantees that half of the spatial vectors remain centered during the operating period of the switch. Finally, the reference signal that incorporates the offset optimizing the spectrum in certain regions [18] is defined by:

$$V_{REF\_K} = V''_k + \frac{V_{DC}}{2} - [\frac{\max(V''_a, V''_b, V''_c) + \min(V''_a, V''_b, V''_c)}{2}] \tag{16}$$

The generation of the carriers is then performed, which consist of four triangular signals that have the same amplitude, frequency and phase disposition, as mentioned above. The multilevel waveform in each phase is then generated by comparing the reference to each carrier and summing the four 2-level results to obtain a seven-level signal. As explained in [18], this 7-level signal can be used as an input for a state machine. It should be noted that only this part of the controller is specific to the hybrid multilevel inverter. The only input of this state machine is the multilevel waveform, and all the transitions in it are defined by the comparison of the input signal with thresholds 0.5, 1.5, 2.5, 3.5 and 4.5.

V. SIMULATIONS OF THE ASYMMETRICAL HYBRID MULTILEVEL INVERTER

A. PD-PWM

The simulations carried out for the three-phase converter with PD-PWM are described in this section. All of the components are considered ideal and the main waveforms are shown. The simulation specifications are given in Table IV.

To evaluate the operation of the asymmetrical hybrid multilevel inverter, simulations were conducted with the proposed modulation. In Figure 8 (a) it can be observed that the single-phase voltage has seven levels: $-1.5kV$, $-1kV$,

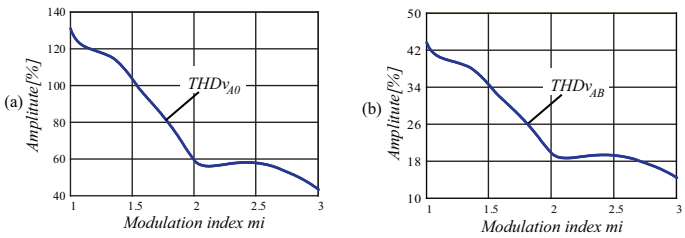

Fig. 7. (a) THD for single-phase voltage and at (b) THD for line-to-line voltage of the inverter.

$-0.5kV$, $0kV$, $0.5kV$, $1kV$ and $1.5kV$. The magnitude of the fundamental component is $1.27kV$ with a THD of 23.3%. The harmonic spectrum is shown in Figure 8(b), where a higher order components appear at $1.5kHz$ and only in side-bands at multiple frequencies of the carrier frequency.

The simulation results for the three-phase 7-level converter are also reported. The simulation specifications are the same as those given previously, except that the total output power is multiplied by three. The phase voltage v_{A0} at the load presents seven levels, as seen in Figure 8(a), while the line voltage v_{AB} presents eleven levels (Figure 8(b)). According to the simulation, the line-to-line voltage has a THDv of 19.10% and the load-phase voltage has a THDv of 21.58%, considering a maximum of 100 harmonics.

B. CSV-PWM Strategy

Using the same design parameters applied in the previous simulation, considering ideal devices, the results obtained in the digital simulation for the CSV-PWM are reported in this section.

Figure 9(a) shows the phase-neutral output voltage and its respective frequency spectrum. It can be observed that the THD_v is 31.40%, due to the fact that this signal has all zero-sequence components. The THD was calculated considering up to the 500$^{\text{th}}$ harmonic, however, the figures show only up to the 240$^{\text{th}}$ harmonic. Figure 9(b) shows the line-to-line voltage and the frequency spectrum for the output voltage, for which the THD_v value is 12.54%.

VI. EXPERIMENTAL RESULTS

A. PD-PWM

To validate the operation of the inverter, an scale experimental prototype of the multilevel asymmetrical inverter was built with the following specifications: $2E = 100V$ and $E = 50V$, output power of $300W$, operating with a switching frequency of 1.5 kHz and fundamental frequency of 50 Hz. The switches used for the switching cell were IRF840A MOSFET and the bridge IRGP30B60KD-E. The modulation strategy was based on the conventional phase disposition (PD) PWM and was implemented using a Texas Instruments digital signal processor (DSP) from the C2000 real-time control family.

Figure 10 (a) and (b) show the results obtained experimentally for both modulations. Figure 10 (a) shows the waveforms for PD-PWM and Figure 10 (b) for CSV-PWM.

Regarding the current sharing, the RMS current levels in the

TABLE IV
Specifications for the Converter Simulation.

Specification	*Symbol*	*Value*
Output power	P_o	54 kW
Dc-link voltage	$3E$	1.5 kV
Load voltage frequency	f_o	50 Hz
Fundamental load voltage (RMS)	$V_{AN,(1)}$	2 kV
Load displacement factor	$\cos(\phi)$	0.9
Modulation index	m_i	0.94
Frequency index	m_f	30
Commutation frequency	f_c	1.5 kHz
Load resistance	R_o	12.0 Ω
Load inductance	L_o	18.51 mH

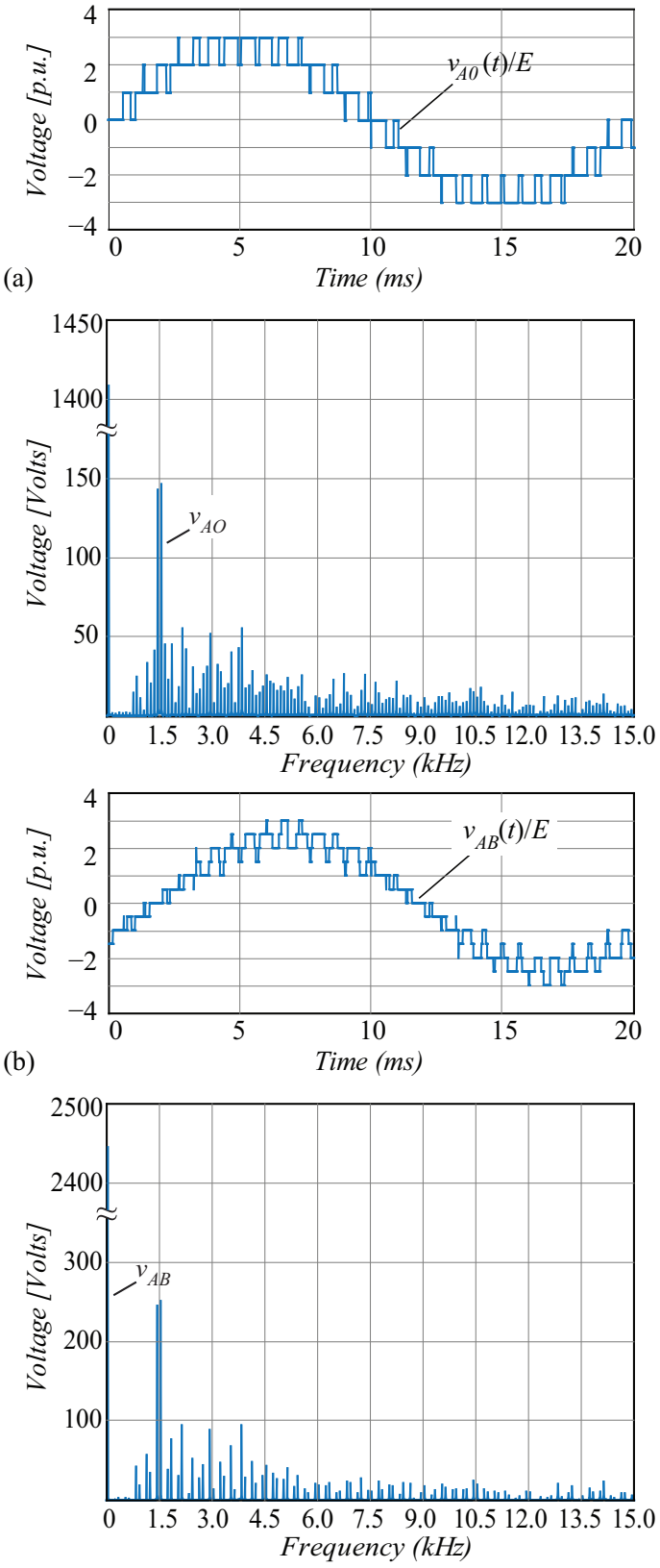

Fig. 8. PD-PWM, (a) phase-load voltage and harmonic spectrum and (b) line-to-line voltage of the three-phase inverter and harmonic spectrum.

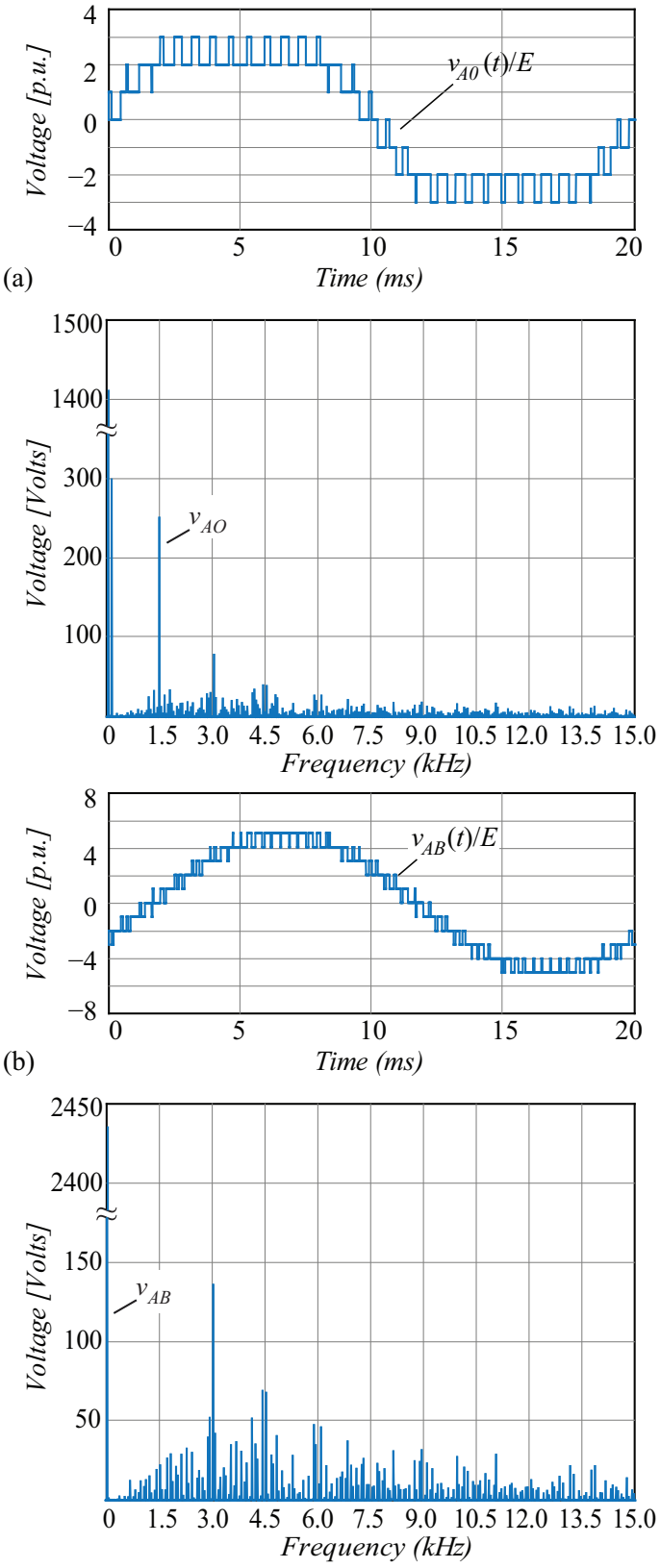

Fig. 9. CSV-PWM, (a) Phase-neutral source voltage with its corresponding frequency spectrum, (b) Line-to-line voltage with the frequency spectrum.

switches are a function of the load angle. For resistive loads the current sharing becomes asymmetrical and the switches, S1 and S3, carry a large percentage of the total current. The current distribution among the fast switches (S_1, S_2, S_3 and S_4) become more even for inductive loads.

For the H-bridge switches, the current distribution is a function of the load angle, however it is more symmetrical due to the symmetry of the output voltage semi-cycles.

Switch S1 has higher conduction loss, since it has to withstand 2/3 of the DC-link voltage and also it conducts a significant share of the load current.

Figure 11(a) shows the measured voltage frequency spectrum, for the phase (V_{AO}) and line (V_{AB}) voltages.

The voltage output for the prototype operating with the PD-PWM was phase-to-neutral (V_{AN}) with a THD_v value of 21.81%, while for the line-to-line voltage (V_{AB}) the THD_v value was 20.55%. Thus, the theoretical and simulated results were consistent.

B. CSV-PWM Strategy

To validate the CSV-PWM strategy, the prototype and specifications were the same as those described for PD-PWM. The results are reported in Figure 10(b).

Figure 10(b) shows the waveforms for the voltage on the converter switches: the H-bridge switch voltage, the voltage on the upper cell switches and the voltage on the lower cell switches.

It can be noted that the voltage stresses of the switches differ. The fast switches (S1 and S2) must withstand a voltage of 2E, S3 and S4 must withstand E. On the other hand, the H-bridge switches (S_5, S_6, S_7 and S_8) must block a voltage level of 3E. However, these switches operate only in one cycle of the output voltage, that is, they operate at low frequency commutation at zero voltage. Basically, the voltage stress in the semiconductors is equal to the DC source it is associated with, and the low frequency switches have to support the total voltage in the DC bus.

Figure 11(b) shows the frequency spectra for the phase voltage and line-to-line voltage. In contrast to Figure 11(a), there is only one harmonic in the phase voltage spectrum, at around 3.0 kHz. This harmonic is generated by the switching, and because the carriers are all in phase, its amplitude is maximized and its phase is directly imposed by the carriers. Since the same carriers are used for the three phases of the converter, this component is present in all phases and cancels in the line-to-line voltage, which can be seen in the same figure.

It is observed for the two modulations that the voltages in the switches S1 and S3 are very different, which leads to different conduction times. Allied to the different voltages between the DC voltage buses, this leads to different levels of power drained for each DC source, which causes an imbalance in the DC bus voltages. In the case of the symmetrical multilevel inverter, as in [16], the voltage balance can be achieved with an appropriated modulation, in other words, the voltage bus is naturally balanced in the symmetrical multilevel inverter.

On applying the CSV-PWM, the THD_v value obtained for the output phase-to-neutral voltage (V_{AN}) was 32.53%, while

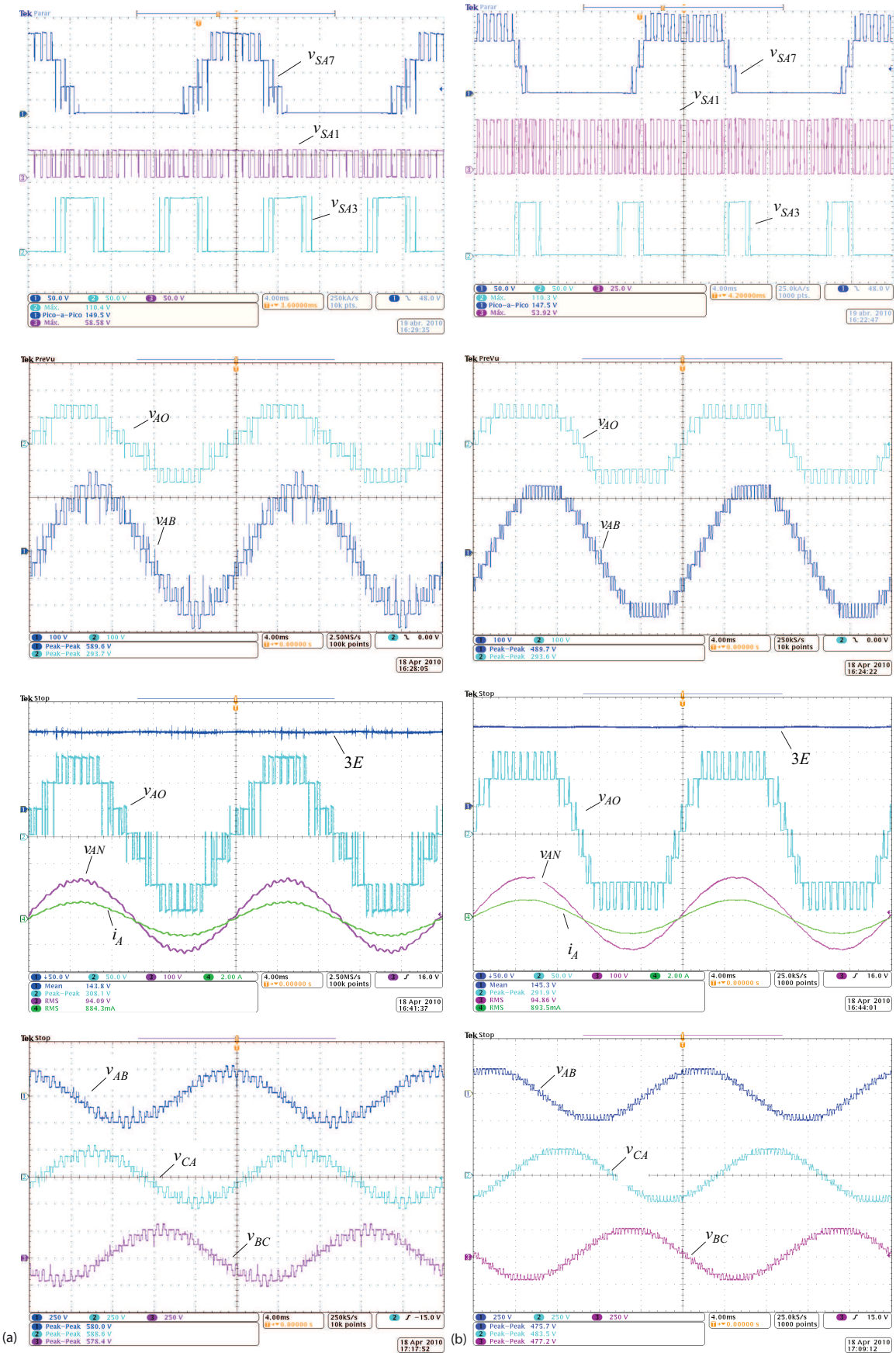

Fig. 10. PD-PWM (a), CSV-PWM (b) - Voltages on the switches (S_7, S_1 and S_3), phase-line (V_{A0}), line-to-line voltage (V_{AB}), DC-link voltage, phase voltage (V_{A0}), current (i_A) , load voltage (V_{AN}) and line voltages $V_{(AB,AC,BC)}$.

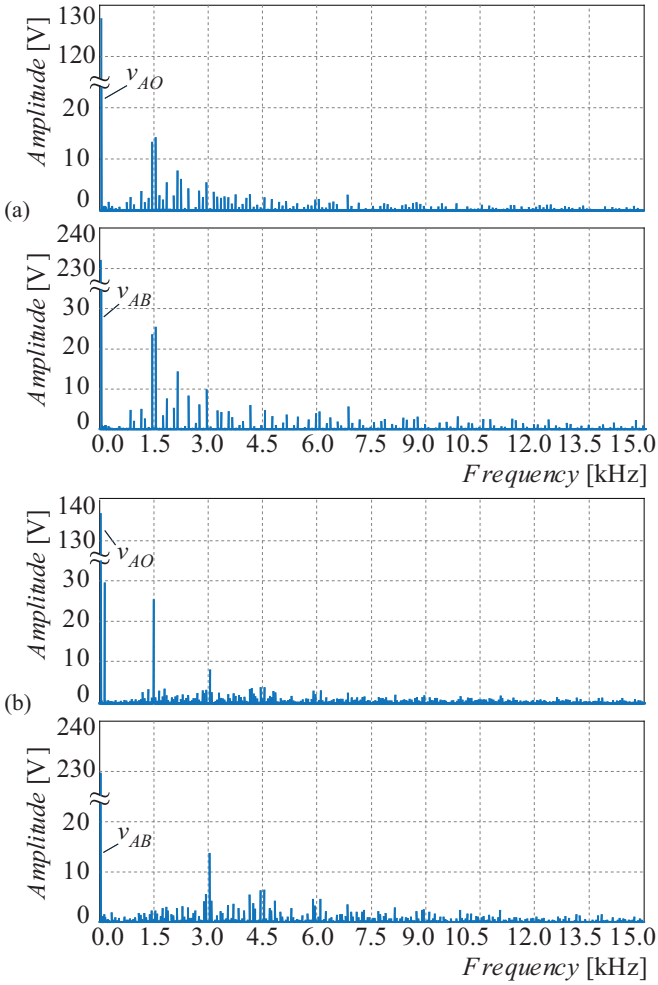

Fig. 11. PD-PWM (a), CSV-PWM (b) - Experimental harmonic spectrum of the phase and line-to-line voltages.

TABLE V
Output voltage THD results for $m_i = 0.94$.

Modulation		Theoretical	Simulation	Experimental
PD-PWM	Phase THD	21.10%	21.58%	21.81%
	Line THD	19.07%	19.10%	20.55%
CSV-PWM	Phase THD	30.57%	31.40%	32.53%
	Line THD	13.09%	12.54%	12.45%

the line-to-line voltage (V_{AB}) had a THD_v value of 12.45%. The THD for the output voltages obtained in the theoretical calculations and the simulation and experimental results are summarized in Table V. All results were obtained with a modulation index of 0.94.

VII. CONCLUSIONS

The results obtained for an asymmetrical multilevel inverter circuit applying two modulation strategies (PD-PWM and CSV-PWM) are reported herein. The switches that form the cell (4LSC) support different voltages depending on which voltage sources are connected and can withstand a voltage of $2E$ or E. The switches on the H-bridge support the total output of the DC-link, which is $3E$.

The voltage obtained at the output of the inverter consists of seven levels with a low harmonic distortion. In the case of conventional PWM this generates high frequency components in the sidebands around multiples of the frequency index, which can be eliminated by a small output filter.

It is important to bear in mind that the appropriated carrier frequency should be chosen, so that the output voltage does not have even harmonic components, given that the values for the index pairs of frequencies do not comply with half-wave symmetry and generate odd and even harmonics.

In the case of CSV-PWM, a seven-level phase-voltage output was obtained and there was an improvement in the inverter output voltage THD, compared with PD-PWM. On comparing these two modulation strategies, it can be seen in the time domain as well as in the frequency domain that CSV-PWM provides better results than PD-PWM.

The main disadvantage of an asymmetrical multilevel inverter, in relation to the symmetrical multilevel inverter [16], is that the natural balance of the voltages in the capacitors is lost. Thus, it is necessary to control these voltages to maintain the balance.

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