MODELING AND DESIGN OF A FAST-DYNAMIC RESPONSE PHASE-LOCKED LOOP BASED ON MOVING AVERAGE FILTER

Fernando O. Martinz [1], Rayra Destro[1], Naji R.N. Ama[2], Kelly C.M. de Carvalho[1], Wilson Komatsu[1], Lourenço Matakas Junior[1]

[1] Polytechnic School of the University of São Paulo, São Paulo - SP, Brazil

[2] Dom Bosco Catholic University, Campo Grande - MS, Brazil

e-mail: fernando_martinz@yahoo.com, matakas@pea.usp.br

***Abstract* – Phase Locked Loops (PLLs) with in-loop Moving Average Filter (MAF) and a Proportional Integral (PI) controller are effective methods to achieve synchronization in grid-connected converters, since they have simple implementation, low computational burden and excellent filtering capability. However, they are known to be slow. The reasons are the MAF time delay and the PI controller tuning method, which makes the design of a fast control loop challenging. This paper demonstrates that the second-order Padé approximation is enough to achieve an accurate model for the MAF, and presents a controller design technique that results in the minimum settling times achievable for a MAF-PLL with a PI controller. Simulation and experimental results validate the proposed approach.**

***Keywords* – Grid Synchronization, Moving Average Filter, Padé Approximation, Phase Locked Loop, PI Controller.**

I. INTRODUCTION

Synchronism systems are essential to allow grid connection of power converters, especially for distributed generation and renewable energy applications [1]-[4]. If synchronism is achieved, the inverter can be connected to the grid and it can synthesize voltage and currents to inject active power into the system. Moreover, grid codes require the inverters to provide fault-ride-through capability during voltage sags or swells, voltage support by means of reactive power control, and frequency support by means of active power injection [5], [6]. The most common synchronization solution to perform these tasks is the Phase-Locked Loop (PLL), which detects the phase angle and the frequency of the AC grid fundamental component for single-phase systems [7], or the phase angle and the frequency of the grid positive-sequence component for three-phase systems [4], [7], [8].

According to Figure 1.a, the classical PLL is composed of a Phase Detector (PD), a Controller (C) and a Voltage Controlled Oscillator (VCO) [9]. In PLLs of grid-connected converters the PD block usually consists of a multiplier type phase detector [4], [7], [8]-[28], which may be followed by a filter $F(s)$ inside the PLL loop or preceded by a filter outside the PLL loop. The first published literature about these PLLs did not apply additional filters [21], [26]. This strategy usually resulted in poor attenuation of the low order harmonics of v_f, increasing the oscillations in output frequency ω_o, and consequently augmenting the distortion in output voltage $\bar{v}_o$. This is the reason why nowadays most PLLs of power electronics applications incorporate filters.

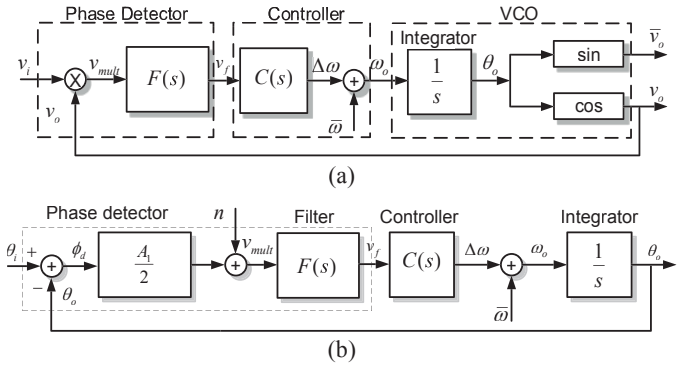

Fig. 1. Classical single-phase PLL. (a) Nonlinear model. (b) Linearized model.

In this way, literature presents many types of filters inside or outside the PLL loop, such as Notch Filters [8], Delayed Signal Cancellation (DSC) [20], Second-order Generalized Integrator (SOGI) [1], [3], [4], Non-Autonomous Adaptive Filter [13], and Moving Average Filters (MAF) [8], [10]-[19], [23], [25], [27], [28]. Among the possibilities to implement these filters, the MAF is a simple with low computational complexity solution that achieves low output distortion. The MAF may have a low computational burden if implemented according to [15]. Some authors locate the MAF outside the PLL loop, where it acts as a pre-filtering stage [25]. However, typically the MAF is inside the PLL loop, which is the case of [8], [10]-[12], [14]-[19], [23], [27], [28], and of the PLL analyzed in this paper.

Authors of [1] and [8] stated that the main disadvantage of in-loop MAF-PLLs consists in its slow-dynamic response, especially for frequency jump cases. The reasons for the slow dynamic behavior are: i) the MAF time delay, which makes the design of a fast control loop challenging, and ii) the controller type and its design procedure adopted. Consequently, several strategies have been presented in literature to solve this problem. Authors of [16] used a Proportional Integral Derivative (PID) controller and proposed pole-zero cancellation in the design of the PLL, (settling time of 3.68 grid cycles). In [18] a phase lead compensator is inserted before the PI controller to reduce the

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phase delay caused by the MAF, and the resulting structure is denominated MPLC-PLL (1.79 cycles). The quasi type-1 PLL (QT1-PLL) is presented in [17], where the PI controller is substituted by a simple gain, and feedforward and feedback loops are added to the system (1.5 grid cycles). Since the QT1-PLL response is poor when DC offset and odd harmonics occur in the PLL input, [19] proposes the hybrid PLL (H-PLL), which consists of a QT1-PLL with DSC filters before the PLL loop to eliminate these components (2.0 cycles). Finally, the differential MAF-PLL (DMAF-PLL) of [27] improves the dynamic response by reducing the MAF window size to one sixth of the fundamental period and by adding derivative filters to eliminate second harmonic components in the PLL input (1.27 cycles). However, the performance of the DMAF-PLL is restricted to specific grid harmonics sequences, i.e., -5th, +7th, -11th, +13th, etc. The performances of MPLC-PLL, QT1-PLL, H-PLL and DMAF-PLL are compared in [28]. Most of these strategies increase the complexity of the MAF-PLL to achieve a better dynamic response. However, this paper shows that it is possible to obtain a fast-dynamic response with a simple in-loop MAF-PLL by using an adequate low-order approximation of the MAF model and by refining the PI controller tuning method. An in-loop MAF-PLL is considered to be fast if it achieves settling times around two grid cycles when a phase jump is applied in the input voltage.

The first contribution of this paper consists of obtaining an adequate approximation for the MAF. The MAF is originally a discrete-time filter with a high order transfer function, and thus the complexity of the PLL design is high [11]. To simplify the analysis and tuning, the MAF-PLL is often designed in continuous-time and then implemented in discrete-time domain [16]. Since the continuous-time model of the MAF presents an exponential function, a series expansion of this term is typically made to obtain a rational expression. As will be detailed in this paper, this rational expression is used to widen the number of available control system design methods and analysis tools for the PLL [29], [30], as well to enable the derivation of a low-order transfer function for the MAF, which simplifies the control system analysis. In this way, authors of [23] did this expansion by using Taylor series and by truncating the series in the first-order term, resulting in a unitary gain of the MAF. Thus, the dynamics of the MAF is neglected in [23], resulting in a slow PLL (14.01 cycles). On the other hand, authors of [16] improved the MAF model of [23] by using a first-order Padé approximation in the continuous-time domain (3.68 cycles). However, as it will be shown in Section III of this work, the first-order Padé approximation also does not allow the design of a fast-dynamic response MAF-PLL, since this approximation order results in significant amplitude and phase errors near the crossover frequency. To solve this issue, this paper evaluates several orders of the Padé approximation for the MAF and demonstrates that the second-order approximation is enough to achieve an accurate model for the MAF which allows fast-dynamic response designs.

The second contribution of this paper consist of improving the PI controller design. This paper uses a PI controller as the *C(s)* function of Figure 1. Typically, this controller is tuned by the Symmetrical Optimum (SO) method, which consists of maximizing the phase margin of the control system, as can be seen in [16], [21], [23] and [25]. However, SO technique does not lead to the minimum achievable settling time when a phase angle step (jump) is applied at the PLL input. The reasons are explained by [31], which states that for control systems that cannot be reduced to the standard second-order system, the correlation between the frequency response and the transient response is more complex, and thus the transient response cannot be easily predictable from the frequency response. Moreover, for the PLL system under analysis the real zero is located near the complex dominant poles, and thus the transient response is substantially affected when compared to the response of the standard second-order system [32], [33]. Thus, for the PLL control system of this paper the phase margin represents more a robustness index than a transient response parameter to be chosen for achieving the desired performance. In this way, this paper presents a PI controller tuning method for a MAF-PLL which aims at minimizing the settling time, while the phase margin is observed only to ensure the control system stability.

Finally, by considering the MAF model with the second order Padé approximation together with the proposed PI controller tuning method, a fast-dynamic response in-loop MAF-PLL is achieved. Settling times around two grid cycles are obtained for phase jumps and for frequency step variations at the grid voltage.

This paper is organized as follows. Section II derives the PLL linear model that will be used for the controllers design. Section III presents the MAF model by using the Padé approximation. In Section IV, the continuous-time PI controllers are tuned for each MAF approximated by five different Padé orders. Simulations are made to evaluate the modeling error caused by the Padé approximation order. Finally, in the experimental setup of Section V, the designed PLLs are implemented in a Digital Signal Processor (DSP), validating the model and the design criterion proposed in this paper.

II. PLL MODELING

Figure 1 shows the single-phase PLL adopted in this paper, where $\bar{\omega}$ is the grid nominal frequency that has the function of keeping the output frequency near the grid frequency during the initialization of the PLL. This frequency is also known as the center frequency in the PLL theory [9]. As can be seen in Figure 1.a, the VCO block is responsible for generating the sinusoidal signals $\overline{v}_o$ (in phase with the input signal v_i) and v_o (in quadrature with the input signal v_i). This is done by integrating the frequency signal ω_o, resulting in the phase angle θ_o, which will be used to synthesize $\overline{v}_o$ and v_o. The transfer functions of the filter and of the PI controller are respectively given by *F(s)* and *C(s)*.

The input (v_i) and output (v_o) voltage signals are respectively given by (1) and (2), where A_1 is the peak of the grid voltage fundamental component, ω_1 is the grid fundamental frequency, h is the harmonic order of the grid voltage, ϕ_1 is the phase of the fundamental component of v_i, and ϕ_o is the phase of v_o.

$$v_i = A_1 \sin\left(\omega_1 t + \phi_1\right) + \sum_{h=2}^{\infty} A_h \sin\left(h\omega_1 t + \phi_h\right), \quad (1)$$

$$v_o = \cos\left(\omega_o t + \phi_o\right) = \cos(\theta_o). \quad (2)$$

If v_o follows v_i (i.e., if $\omega_o = \omega_1$) then the output of the PD block is composed of a constant term and of sinusoidal terms, according to (3), where the term *n* represents the sum of all harmonics generated by the multiplier [15], [16]. Moreover, if small values of ϕ_d are considered, then $\sin(\phi_d) \approx \phi_d$, which linearizes the PD block, as can be seen in (3) and in the PLL model of Figure 1.b.

$$v_{mult} = 0.5A_1 \sin\left(\phi_d\right) + n = 0.5A_1 \sin\left(\phi_1 - \phi_o\right) + n,$$

$$v_{mult} \approx 0.5A_1\left(\phi_1 - \phi_o\right) + n. \quad (3)$$

The controller of Figure 1 forces the difference between ϕ_o and ϕ_1 to be zero (i.e., $\phi_d \to 0$). Moreover, the signal *n* represents a disturbance to the linearized system, to be attenuated by $F(s)$, $C(s)$, and by the integrator of the VCO block. This signal also influences the behavior of θ_o in the linearized model of Figure 1.b and exists even when v_i is purely sinusoidal. For this case *n* presents only a component whose frequency is $2\omega_1$ with amplitude $A_1/2$. Thus, if *n* is not properly attenuated, harmonic distortion will appear in v_o. This issue is detailed in next Section, which analyses the MAF performance with respect to the attenuation of *n*. Since the controller of Figure 1.b affects the attenuation of *n*, and since the filter affects the PLL dynamic performance, Sections III and IV assume these two blocks as a single block to be designed.

III. MODELING THE MAF

This Section describes the MAF in the discrete and in the continuous-time domains.

A. MAF Description in Discrete-time

The calculation of the *N-th* order MAF output (v_f) is based on the arithmetic mean (or simply on the average value) of the last *N* stored samples of the signal v_{mult}, as it is described by [15], i.e.,

$$v_f(k) = (1/N) \cdot \sum_{j=1}^{N} v_{mult}(k - j + 1) = S(k)/N. \quad (4)$$

The parameter *N* is also known as the window size of the MAF. In (4) the variable *S(k)* is the sum of the last *N* stored samples and requires *N-1* sum operations to be calculated. A more efficient way to compute *S(k)* is by means of (5),

$$S(k) = S(k-1) + v_{mult}(k) - v_{mult}(k-N). \quad (5)$$

Equation (5) avoids *N-1* sum operations, since it employs the value of *S(k-1)* calculated in previous sampling time, and the current sample $v_{mult}(k)$ minus the oldest value $v_{mult}(k-N)$. By replacing (5) into (4), (6) is easily calculated by

$$v_f(k) = (1/N) \cdot \left[S(k-1) + v_{mult}(k) - v_{mult}(k-N)\right]. \quad (6)$$

Thus, the discrete-time transfer function of a *N-th* order MAF [11] is derived from (6) and given by

$$F_{MAF}(z) = \frac{v_f(z)}{v_{mult}(z)} = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}}. \quad (7)$$

Considering the sampling frequency equal to f_s, *N* is given by

$$N = f_s / f_n, \quad (8)$$

where f_n is the MAF base frequency. Ideally, the harmonics of v_{mult} which are multiple of f_n have infinite attenuation, as can be seen in Figure 3 (solid line curve). When v_i contains only odd harmonics, the MAF attenuates all the frequency components multiples of $2f_1$. Thus, substituting $f_n = 2f_1$ in (8) results $N = f_s/2f_1$. On the other hand, input signals v_i with DC or odd harmonics require $f_n = f_1$. If the grid frequency varies then attenuation of harmonics provided by the MAF will decrease. In this case, an adaptive MAF must be implemented by varying the switching frequency or by changing the window size, as it is done in [10].

Figure 2 shows the discrete-time nonlinear and linearized models of the PLL with the MAF and the PI controller, where the latter and the VCO integrator have been discretized by applying the bilinear (Tustin) transformation, where T_s is the sampling period. This paper adopts this discretization method because it preserves the stability when mapping from the continuous to the discrete-time [34].

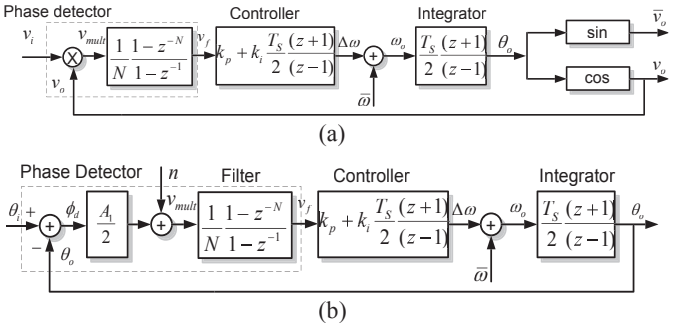

Fig. 2. Discrete-time single-phase PLL with the MAF. (a) Nonlinear model. (b) Linearized model.

B. Padé Approximation for the MAF in Continuous-time

The main objective of this Section is to obtain a reduced order MAF model in continuous-time by applying the Padé approximation. In this way, the continuous-time version of (4) is given by

$$v_f(t) = \frac{1}{T_n}\int_{t-T_n}^{t} v_{mult}(\tau)d\tau = \frac{1}{T_n}\left(\int_0^t v_{mult}(\tau)d\tau - \int_0^{t-T_n} v_{mult}(\tau)d\tau\right), \quad (9)$$

where T_n is obtained by rearranging (8), resulting in $T_n = N/f_s = 1/f_n$. Applying the Laplace transformation to (9), the MAF transfer function is

$$F_{MAF}(s) = \frac{v_f(s)}{v_{mult}(s)} = \frac{1}{T_n}\left[\frac{1}{s} - \frac{\exp(-sT_n)}{s}\right] = \frac{1-\exp(-sT_n)}{sT_n}. \quad (10)$$

Authors of [33] stated that for most of analytical tools used for evaluation and design of control systems, the plant plus controller are described by rational functions or by a finite set of differential equations with constant coefficients. For instance, tools such as the Routh-Hurwitz criterion are restricted to rational transfer functions [29]. The root-locus technique is also easily applied to systems with rational

transfer functions [29]. Linear–quadratic–Gaussian (LQG) regulator and pole placement do not work properly if time delays are present [30]. In this way, to not restrict the control system available tools and analysis, typically the pure delay of (10) is expressed by a rational function. This paper uses the Padé approximation of the pure delay presented in [35], considering that the numerator and denominator have the same order p, resulting in

$$\exp(-sT_n) \cong \frac{\frac{1}{12}\sum_{m=0}^{p}\frac{(2p-m)!}{m!(2-m)!}(-sT_n)^m}{\frac{1}{12}\sum_{m=0}^{p}\frac{(2p-m)!}{m!(2-m)!}(sT_n)^m} = \frac{P_p(sT_n)}{P_p(-sT_n)}. \quad (11)$$

Substituting (11) into (10), the MAF transfer function with the Padé approximation is

$$F_{MAF}(s) = \frac{\sum_{m=0}^{p}\frac{(2p-m)!}{m!(2-m)!}(sT_n)^m - \sum_{m=0}^{p}\frac{(2p-m)!}{m!(2-m)!}(-sT_n)^m}{sT_n\sum_{m=0}^{p}\frac{(2p-m)!}{m!(2-m)!}(sT_n)^m},$$

$$F_{MAF}(s) = \frac{P_p(-sT_n) - P_p(sT_n)}{sT_n \cdot P_p(-sT_n)}. \quad (12)$$

As the order of the Padé approximation p increases in (12), $F_{MAF}(s)$ tends to the full order discrete-time transfer function described by (7). This can be seen in Figure 3, where the Padé approximations from the 1st to the 3rd order are shown for a MAF with $N=100$, $f_n = 120\,\text{Hz}$ and $f_s = 12\,\text{kHz}$.

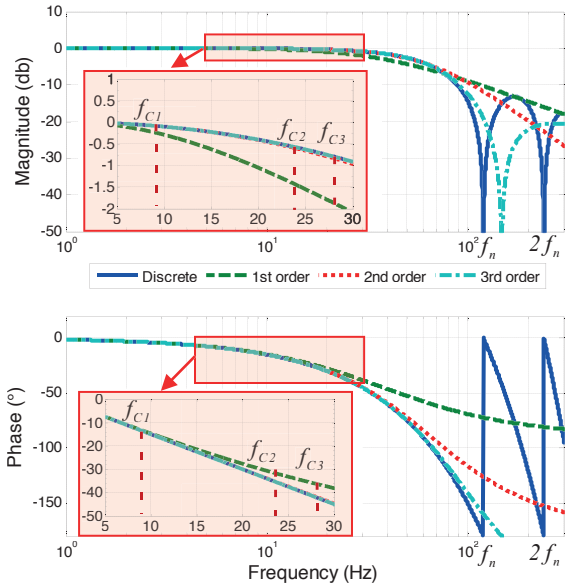

Fig.3. Bode Diagram of the discrete-time MAF for $N=100$, $f_n=120$ Hz, $f_s=12$ kHz and of the continuous-time MAF transfer functions using the 1st to 3rd order Padé approximations.

The zoomed views of the magnitude and phase plots in Figure 3 (shaded areas) show that, as the frequency increases from f_{C1} to f_{C3}, the first-order approximation of the continuous-time MAF model deviates from the original discrete-time MAF transfer function. Since the PLL crossover frequency typically lies in the shaded areas of Figure 3, this means that as the crossover frequency increases, the model mismatch of the first-order approximation also increases (see dashed line in Figure 3). Consequently, fast-dynamic response PLLs (i.e., with higher crossover frequencies) must not adopt the first-order approximation to model the MAF, as it will be confirmed in the results of next Section. It must also be noted in Figure 3 that, by increasing only one order of the Padé approximation to $p=2$, the amplitude and phase errors are significantly reduced (see magnitude and phase errors for f_{C2} and f_{C3}, dotted lines in Figure 3). For instance, for f_{C2} the magnitude and phase error for the first order approximation are respectively 147.96% and 11.05%, while for the second order approximation these errors decrease to respectively 4.19% and 0.33%.

As can be seen in Figure 3, the Padé approximation of the pure delay is a good choice for the frequency domain in a limited range of frequency. Moreover, the use of the Padé approximation allows to compare the proposed method with the existing literature MAF-PLL designs.

IV. TUNING OF THE PI CONTROLLER

This Section details the proposed tuning method of the PI controllers and the criteria to select the Padé approximation order for the single and three-phase MAF-PLLs.

A. Tuning Method Applying the Continuous-time Linear model

The PLL continuous-time linearized model is obtained by substituting (12) into the $F(s)$ function of Figure 1.b, and by considering the PI controller described by

$$C(s) = k_p + k_i/s. \quad (13)$$

The PLL design procedure of this paper aims the minimum possible settling time for an arbitrary order p of $F_{MAF}(s)$. Considering (12) and (13), the minimum order of the closed loop system to be designed in continuous-time is three, obtained for the 1st Padé approximation order (i.e., $p=1$). As p increases, the design complexity also increases, and it becomes harder to obtain algebraic expressions that relate the proportional and integral gains with the settling time. Therefore, the controller design in this paper will be done using a graphical procedure obtained by exhaustively simulating the linearized model of Figure 1.b for a unit step input. The procedure consists of first calculating the settling time by performing a gain sweep on k_p and k_i. Next, the optimal values of the proportional and integral gains that minimize the settling time are graphically evaluated, similarly as it is done by [22]. Additionally, computation and graphical analysis of the phase margin and the overshoot values are also performed. Though the presented controller tuning method may not require the time delay of (10) to be approximated by rational functions, the Padé approximation of (12) is applied in a way to extend the proposed model to any controller or any simulation software which cannot directly deal with exponential functions in control systems.

The tuning method will be shown for the second-order Padé approximation. In this way, for $f_1 = 60\,\text{Hz}$, $p=2$ and

$T_n = 1/120\,s$, Figure 4 shows the plot of the continuous domain settling time t_{SC} as a function of the gains k_p and k_i.

All settling times are calculated for the ±2% final value range. The minimum settling time is shown in Figure 4.a and emphasized in the 2D zoomed view of Figure 4.b by the '+' symbol. This point is achieved for $k_p = 312$ and $k_i = 16192$, resulting in $t_{SC} \cong 2.06$ cycles.

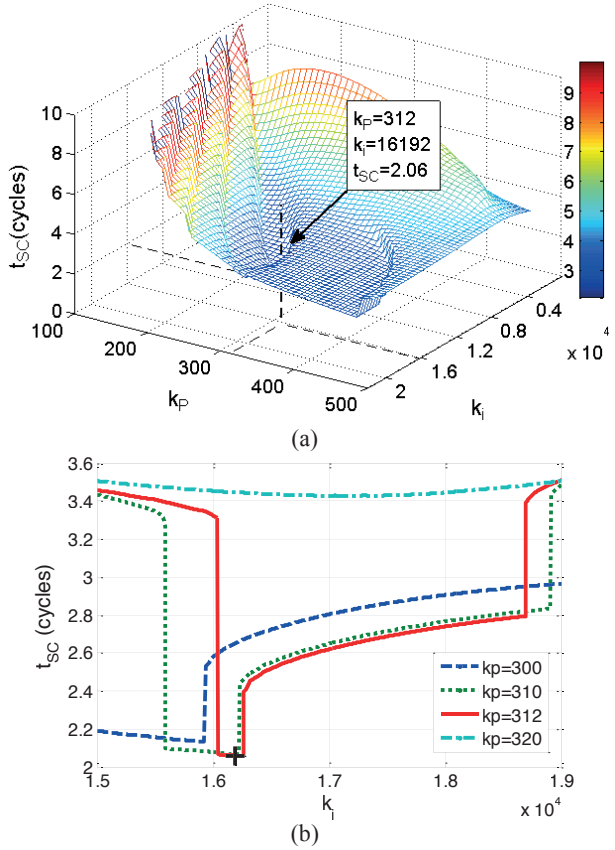

Fig. 4. Settling time for a unit step input in continuous-time and a 2nd order Padé approximation of the MAF, $f_1 = 60\,\text{Hz}$ and $T_n = 1/120\,s$. (a) 3D view. (b) 2D plot for four values of k_P.

Figure 5 shows the plot of the continuous-time domain overshoot and phase margin as a function of the gains k_p and k_i. The designed controller results in the overshoot of $M_P = 48.08\%$ in Figure 5.a and in the phase margin of 34.82° in Figure 5.b, both highlighted by the "+" symbol.

B. Selection of the Padé Approximation Order and Validation of the Tuning Method in the Linearized Discrete-time Model

Using the proposed tuning method of Section IV.A, the optimized gains k_p and k_i are now determined in continuous-time domain for different values of p. The PLL with the original full order discrete MAF of Figure 2.b is simulated using MATLAB® and it is compared to the continuous-time reduced order linearized PLL of Figure 1.b for *C(s)* and *F(s)* respectively given by (12) and (13). Comparison of settling times will define which is the minimum Padé approximation order that adequately represents the discrete-time MAF. Considering the PI controller designs based on Padé approximation from the 1st to the 5th order, the results are summarized in Table I, which shows:

- k_p and k_i gains, designed in the continuous-time linearized model, and obtained according to the minimum settling time criterion proposed in Section IV.A. For the first-order of the Padé approximation, the design for the Symmetrical Optimum (SO) method is also shown;

- the PLL settling time t_{SC}, simulated in MATLAB® for the continuous-time linearized model of Figure 1.b, with *F(s)* defined by (12);

- the PLL settling time t_{SD}, the gain margin G_m and the phase margin P_m, simulated in MATLAB® for the full order discrete-time linearized model of Figure 2.b.

Again, all settling times are referred to the ±2% final value range for a step response.

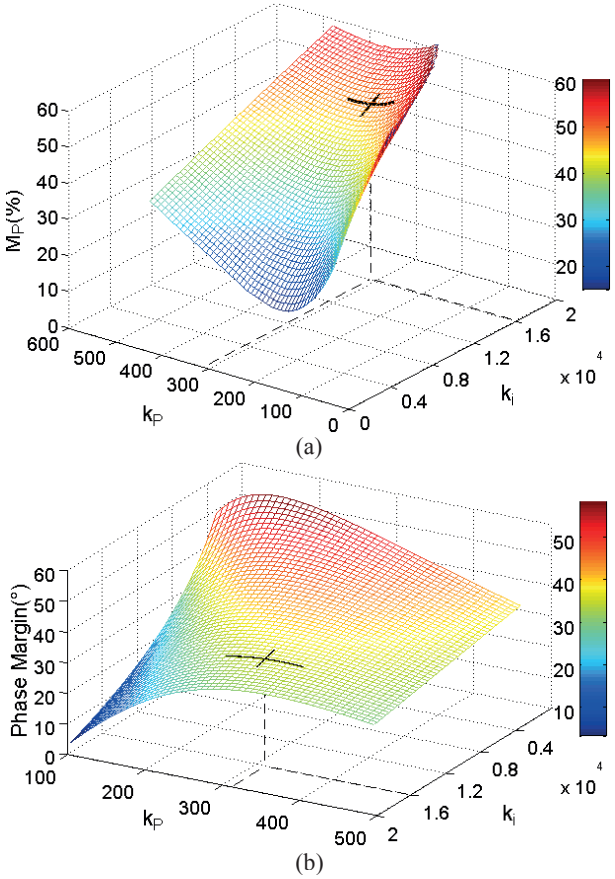

Fig. 5. Response for a unit step input in continuous-time and a 2nd order Padé approximation of the MAF, $f_1 = 60\,\text{Hz}$ and $T_n = 1/120\,s$. (a) Overshoot. (b) Phase Margin.

Table I shows that for the proposed tuning method the settling time of the first-order Padé approximation in the discrete-time model is 3.24 cycles of v_i while the value obtained for the linearized model of Figure 1.b is t_{SC}=1.99 cycles. This discrepancy confirms that the first-order approximation does not model adequately the MAF for fast-dynamic responses PLLs. As stated before, this is due to the errors of the 1st order Padé approximation at the crossover frequency region, when compared to the full order discrete-time MAF. The MAF continuous-time model mismatch for the first-order approximation can be seen in Figure 3, where the crossover frequency of the continuous-

time model using the proposed tuning method is $f_{C3} = 28.56\,\text{Hz}$.

The analysis of Table I also shows that, from the 2nd order on, the settling time of the continuous-time and discrete-time models are the same. Moreover, the gain and phase margins are enough to guarantee the control system stability. Table I also confirms that for the in loop MAF-PLL with a PI controller, MAF approximations of order higher than two do not result in significant improvements on the dynamic response. This result is compatible with [11], where the full order MAF discrete-time transfer function with N=100 is employed but settlings times around two grid cycles are achieved. That is, if settling times lower than two cycles are desired for a the proposed PLL topology, more complex control strategies, which are out of the scope of this paper, must be adopted.

For instance, Figure 3 shows that by using the proposed tuning method and the second-order approximation, the crossover frequency is $f_{C2} = 24.45\,\text{Hz}$ and the MAF modeling errors are very small. In summary, considering the simplicity of the transfer function, the 2nd order approximation is chosen in this paper for the PI controller design, since higher orders would only bring complexity to the control system design without improving the dynamic response.

TABLE I
Simulation of the Single-phase Discrete-time Linearized PLL for $f_1 = 60\,\text{Hz}$, $f_s = 12\,\text{kHz}$, $N = 100$

Padé Order	k_P	k_i	t_{SC} (cyc.)	t_{SD} (cyc.)	G_m (dB)	P_m (deg.)
1st-SO	200	8334	3.74	3.71	14.26	43.57
1st	380	19120	1.99	3.24	8.35	31.92
2nd	312	16192	2.06	2.06	10.01	35.02
3rd	312	16219	2.05	2.05	10.00	34.99
4th	312	16240	2.04	2.05	10.00	34.97
5th	312	16240	2.04	2.05	10.00	34.97

If the PI controller is tuned according to the SO method, the design proposed in [16] is based on (14) and (15), where A_1 is the amplitude of the fundamental component and b is a design constant which should be selected according to the required transient response and stability margin. Assuming 60 Hz as the grid nominal frequency, the grid fundamental component $A_1 = 1.0\,\text{V}$, $b = 2.4$ and $T_n = 1/120\,\text{s}$, then for the single phase model of Figure 1.b the controller gains are $k_P = 200$ and $k_i = 8333.34$.

$$k_p = 2\left(2 / A_1 b T_n\right), \tag{14}$$

$$k_i = 2\left(4 / A_1 b^3 T_n^{\,2}\right). \tag{15}$$

A slower dynamic PLL is achieved for the SO method and the 1st order approximation is enough to represent the MAF model. This can be noted in Figure 3 for the crossover frequency $f_{C1} = 9.44\,\text{Hz}$ obtained for the SO tuning method. As can be seen in the Table I, the settling times and the phase margin obtained in continuous-time domain (3.74 cycles and 45.25°) match with the results of the discrete-time model (3.71 cycles and 43.57°). In summary, to avoid unacceptable modeling and design errors, the first-order Padé approximation may be only used for slow-dynamic response MAF-PLLs.

The proposed tuning method may be applied for the most typical grid frequencies $f_1 = 50\,\text{Hz}$ and $f_1 = 60\,\text{Hz}$, as well for the most typical MAFs found in literature ($f_n = f_1$ and $f_n = 2f_1$). In this way, PI gains are obtained in continuous-time and are shown in Table II, where the parameters t_{SD}, G_m, G_m and f_C were obtained for a discrete-time implementation with $f_S = 12\,\text{kHz}$. As it is stated in [16], since typically the PLL bandwidth is much lower than its sampling frequency, the continuous-time design can provide an accuracy as good as that achievable in discrete-time domain. In any case, design guidelines for discrete-time analysis and tuning are shown in [10], [11] and [12]. In [12] an existing pair of discrete controller gains can be easily readjusted for other operation conditions, including new sampling frequencies values.

TABLE II
Controller Gains for Single Phase Discrete-time Linearized PLL

f_1	f_n	Padé Order	k_P	k_i	t_{SD} (cyc.)	G_m (dB)	P_m (deg.)	f_c (Hz)
50 Hz	50 Hz	1st	159	3300	6.47	8.23	31.75	11.93
		2nd	130	2800	4.10	9.91	34.88	10.18
	100 Hz	1st	319	13300	3.23	8.27	31.78	23.93
		2nd	260	11290	2.05	9.97	34.88	20.38
60 Hz	60 Hz	1st	191	4780	6.46	8.23	31.68	14.33
		2nd	156	4064	4.09	9.91	34.76	12.23
	120 Hz	1st	380	19120	3.24	8.35	31.92	28.56
		2nd	312	16192	2.06	10.01	35.02	24.45

Despite they must not be used for fast-dynamic responses MAF-PLLs, the gains for the first order Padé approximations are also shown in Table II. They are only presented because they will be used for the experiments in Section V.

The extension of the proposed tuning method to the three-phase case is shown in next Section.

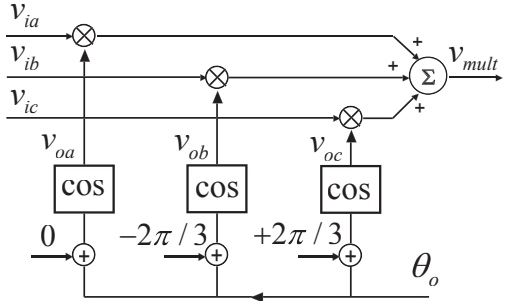

Fig. 6. Three-phase multiplier

C. Extension to Three-phase PLL

The previous single-phase results may be extended to three-phase PLLs if some modifications are made in the control system of Figures 1 and 2. The first one consists of generating the equally displaced three-phase VCO signals

$v_{o\_a}, v_{o\_b}, v_{o\_c}$ according to Figure 6 [24]. The multiplier output v_{mult} is obtained by means of the dot product of the input signals $v_{i\_a}, v_{i\_b}, v_{i\_c}$ and the VCO voltages $v_{o\_a}, v_{o\_b}, v_{o\_c}$.

Since the three-phase dot product gain is 3/2 [24] and the single-phase multiplier gain of Figure 1.b is 1/2, the controllers gains derived for the single-phase PLL in Table I must be divided by 3 to keep the loop gain unchanged. It must also be clarified that for both single and three-phase PLLs, the amplitude of the input signal A_1 is considered unitary, and this can be achieved by normalizing the input signals by their nominal fundamental peak amplitude.

V. EXPERIMENTAL RESULTS

The PLL of Figure 2.a was implemented in the TMS320F28335 Texas DSP for the three-phase structure of Section IV-C. The PLL input signals (v_i) were generated in the DSP, and data were post processed in MATLAB®.

By using the tuning method proposed in this paper, the PI controllers (designed for the first and second-order Padé approximation of the MAF) are tested, and then their performances are compared to the PI controller adjusted by the SO for the following cases:

- Case A: $f_1 = 60\,\text{Hz}$, $f_n = 120\,\text{Hz}$ and $f_s = 12\,\text{kHz}$ ($N = 100$);
- Case B: $f_1 = 50\,\text{Hz}$, $f_n = 100\,\text{Hz}$ and $f_s = 10\,\text{kHz}$ ($N = 100$);
- Case C: $f_1 = 50\,\text{Hz}$, $f_n = 50\,\text{Hz}$ and $f_s = 10\,\text{kHz}$ ($N = 200$).

In all cases a phase jump of 40° and a frequency jump of 5 Hz are applied for the three input voltages. The PI controllers gains of Table II are divided by three for the three-phase PLL, as stated in Section IV-C.

Figures 7, 8 and 9 show the results for the Proposed Tuning (PT) method based on the first and second-order Padé approximations for the MAF, and for the Symmetrical Optimum (SO) technique considering the first order Padé approximation. Table III summarizes the experimental results for the phase jump case, for different fundamental frequencies and different MAF window sizes. These results confirm again that the behavior of the system designed for the 1st order Padé approximation is significantly different from that achieved for the discrete-time MAF if the minimum settling time criterion is adopted (fast-dynamic response PLL), since the mean of the errors of Table III is 64.92% for t_s and 33.84% for M_p. Furthermore, it is possible to note that by increasing the Padé approximation to the second-order, the designed and experimental values of the settling times are almost equal, and the mean of the errors between the continuous and discrete-time models are reduced to 1.38% for t_s and 0.43% for M_p.

On the other hand, if the PLL is designed according to SO method for the 1st order Padé approximation, the mean of the errors for the settling time and overshoot are 0.95% and 2.57%, respectively. These results confirm that for a slow-dynamic response MAF-PLL, the 1st order Padé approximation represents a feasible model for the MAF.

In summary, the results obtained in Table III demonstrate that the second-order linear approximation of the MAF is adequate to model the non-linear PLL with the full order MAF and the PI Controller of Figure 2.a for different window sizes and fundamental frequencies, and fast-dynamic response.

The frequency jump test for the three-phase case resulted null frequency and phase errors. The mean f_0 settling times for *N=100* are equal to 2.21 cycles (SO), 1.39 cycles (1st order PT) and 1.58 cycles (2nd order PT). The mean f_0 overshoots for *N=100* are equal to 2.75 % (SO), 4.38% (1st order PT) and 3.94% (2nd order PT).

Figure 10 compares the continuous-time linearized PLL (simulation of Figure 1b) with the discrete-time nonlinear PLL (experimental results, Figure 2.a) for the 40° phase jump of Case A. The PI controllers are tuned using the Proposed Tuning Method and the 2nd order Padé approximation for the MAF. Results show good agreement between the continuous-time linear model and the real PLL.

V. CONCLUSION

This work has analyzed the modeling and the design of PLLs which use Moving Average Filters inside the Phase Detector and PI controllers in the Loop Filter block. This paper has shown that it is possible to obtain a fast-dynamic response stable MAF-PLL if the MAF is modelled by using a second-order Padé approximation, and if the controller gains are selected in a way to minimize the settling time instead of maximizing the phase margin. Simulation and experimental results of single and three-phase cases have shown that the proposed model and tuning method allow achieving settling times of approximately two grid cycles for phase jumps when $f_n = 2f_1$, with null frequency and phase errors, validating the proposed approach.

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TABLE III
Experimental and Designed Results of t_s and M_p, for 40° Phase Jump

PLL design			Case A (60Hz, N=100)			Case B (50Hz, N=100)			Case C (50Hz, N=200)		
			2nd order, PT	1st order, PT	1st order, SO	2nd order, PT	1st order, PT	1st order, SO	2nd order, PT	1st order, PT	1st order, SO
Designed (continuous-time)	t_{SC}	(ms)	34.25	33.17	61.33	41.00	39.60	73.60	82.40	79.40	147.20
		(cycles)	2.06	1.99	3.68	2.05	1.98	3.68	4.12	3.97	7.36
	M_p	(%)	48.08	39.88	33.84	48.39	39.91	33.78	48.14	39.78	33.83
Experimental (discrete-time)	t_{SD}	(ms)	34.67	54.67	61.87	41.54	65.36	74.29	83.71	130.92	148.73
		(cycles)	2.08	3.28	3.71	2.08	3.29	3.71	4.18	6.55	7.44
		Error (%)*	1.23	64.82	0.88	1.32	65.05	0.94	1.59	64.88	1.04
	M_p	(%)	48.38	53.51	34.72	48.51	53.57	34.67	47.94	52.95	34.67
		Error (%)*	0.62	34.18	2.60	0.25	34.23	2.63	0.41	33.11	2.48

*Error (%) = 100 x |(experimental result - designed value) / designed value|

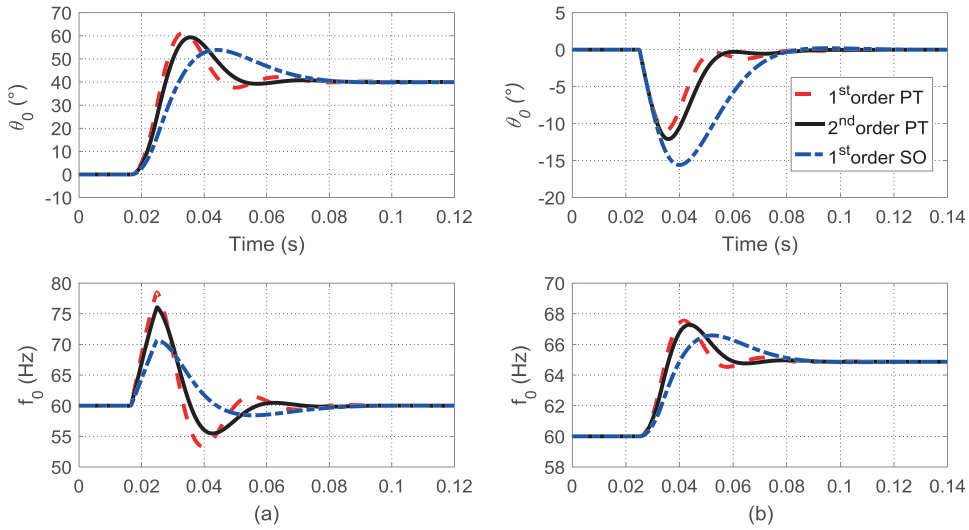

Fig. 7. Experimental results for Case A $\left(f_1 = 60\text{Hz}, f_n = 120\text{Hz}, N = 100\right)$. Output phase angle θ_o (top) and estimated frequency f_o (bottom). (a) 40° phase jump. (b) 5Hz frequency jump.

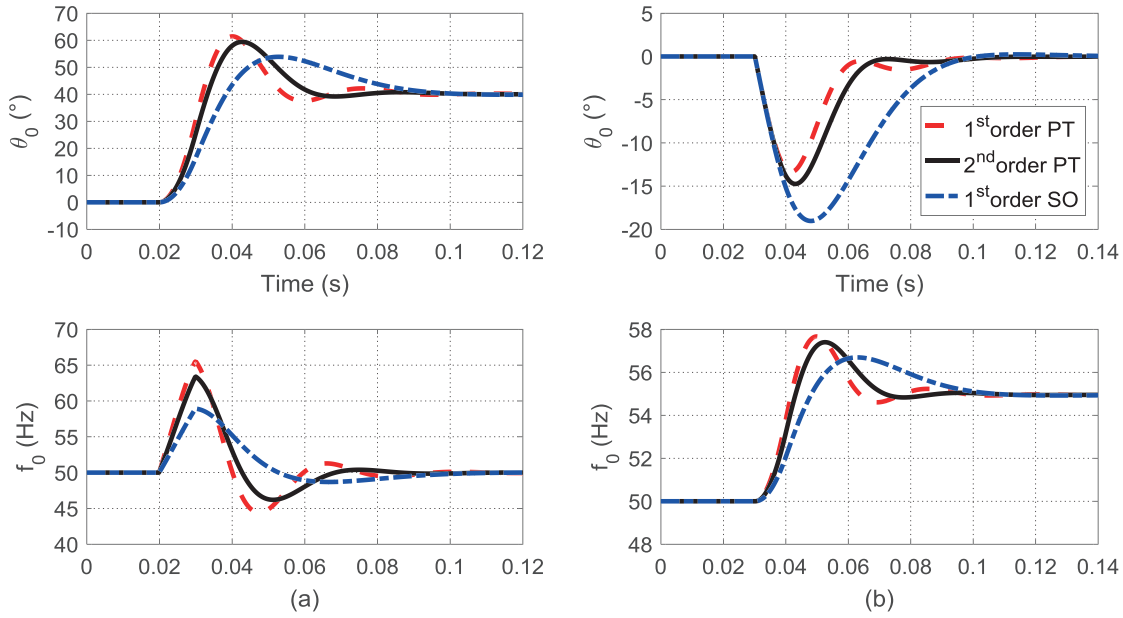

Fig. 8. Experimental results for Case B $\left(f_1 = 50\text{Hz}, f_n = 100\text{Hz}, N = 100\right)$. Output phase angle θ_o (top) and estimated frequency f_o (bottom). (a) 40° phase jump. (b) 5Hz frequency jump.

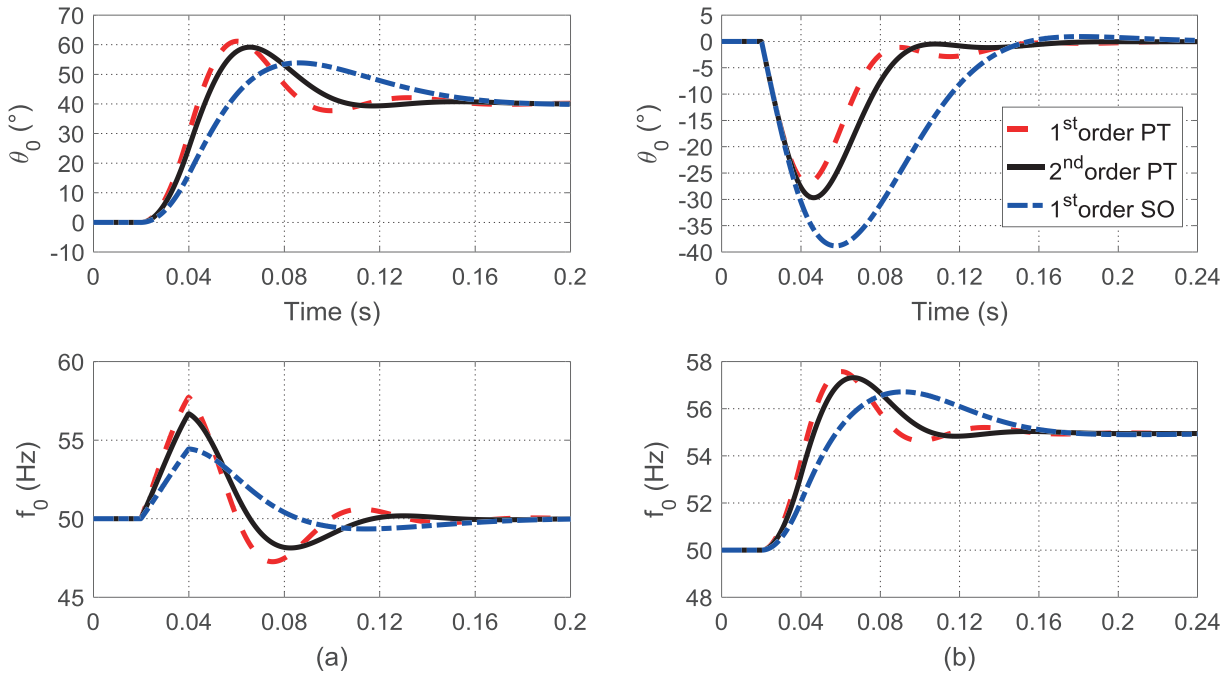

Fig. 9. Experimental results for Case C $\left(f_1 = 50\text{Hz}, f_n = 50\text{Hz}, N = 200\right)$. Output phase angle θ_o (top) and estimated frequency f_o (bottom). (a) 40° phase jump. (b) 5Hz frequency jump.

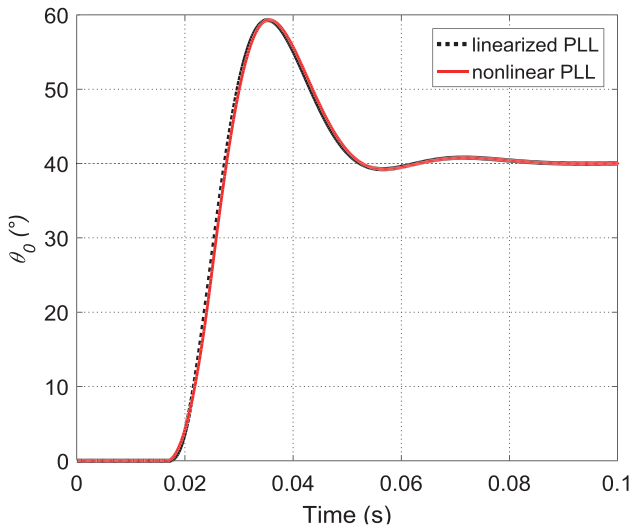

Fig. 10. Output phase angle θ_o for case A and a 40° phase jump. Simulation of continuous-time linear PLL (dotted line) and experimental results for nonlinear model (solid line).

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BIOGRAPHIES

Fernando Ortiz Martinz received the B.S. degree in electrical engineering from the State University of Campinas, São Paulo, Brazil, in 2003, and the M.S. and Ph.D. degrees from the Polytechnic School of the University of São Paulo (EPUSP), São Paulo, Brazil, in 2007 and 2013, respectively. His interests include modeling, control, and synchronization in power electronics, power quality, and grid-connected power converters. Mr. Martinz is a member of the Brazilian Power Electronics Society (SOBRAEP).

Rayra Destro received the B.S. degree in electrical engineering from the Polytechnic School of the University of São Paulo, Brazil, in 2015. Currently, she is pursuing the M.S. degree at the Polytechnic School of the University of São Paulo. Her interests include synchronization systems and industrial automation.

Naji Rajai Nasri Ama received the B.S. (2000) and the M.S. (2003) degrees in electrical engineering from the University of Technology, Baghdad, Iraq, Ph.D. (2012) and Post-Doctorate (2014) in Electrical Engineering from the Polytechnic School of the University of São Paulo (EPUSP), São Paulo, Brazil. Currently, he is an Associate Professor at Dom Bosco Catholic University (UCDB) and a postgraduate professor at the Federal University of Mato Grosso do Sul (UFMS). His research interests include grid synchronization methods, power electronics, digital signal processing, control systems, and grid-connected power converters.

Kelly Caroline Mingorancia de Carvalho received the B.S. and M.S. degrees in electrical engineering from the Polytechnic School of the University of São Paulo, São Paulo, Brazil, in 2012 and 2015 respectively. Currently, she is pursuing the Ph.D. degree in electrical engineering at the Polytechnic School of the University of São Paulo. Her current research interests include power quality, active power filters, modular multilevel converters and disturbances detection in power systems.

Wilson Komatsu born in São Paulo, Brazil, in 1963. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Polytechnic School of the University of São Paulo (EPUSP), São Paulo, in 1986, 1992, and 2000, respectively. He is Associate Professor of power electronics at EPUSP. His research areas are control and modeling of static converters and their application to electrical power systems and electrical power quality. Dr. Komatsu is a member of the Institute of Electrical and Electronics Engineers (IEEE) and of the Brazilian Power Electronics Society (SOBRAEP).

Lourenço Matakas Junior received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Polytechnic School of the University of São Paulo, São Paulo (EPUSP), Sao Paulo, in 1984, 1989, and 1998. He is an Associate Professor at EPUSP. His research focus on topologies, control and application of static converters connected to the grid, phase-locked loops, and pulse width modulation strategies. He is a member of the Brazilian Power Electronics Society (SOBRAEP) and IEEE.