PASSIVE VOLTAGE BALANCING IN MODULAR MULTILEVEL CONVERTER DURING PRECHARGE: ANALYSIS AND DESIGN

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***Abstract* – The modular multilevel converter is composed of many equal submodules connected in series, each having to ideally withstand the same voltage and current stresses. The resulting configuration when each SM capacitor feeds its own auxiliary power supply is unstable during at least part of the converter precharge process. SM capacitor voltages can diverge until a protection trips in. The system can be stabilized by adding a balancing resistor in parallel to each SM capacitor. In this work, models for the dc-side precharge of the modular multilevel converter are proposed and its dynamics are analyzed in depth. The worst case parameter combination is found by running the models for all possible combinations within certain discrete ranges. A conservative estimation of the balancing resistor value is proposed by analysis of the results.**

***Keywords* – Modular Multilevel Converter, Nonlinear Dynamics, Passive, Precharge, Stability, Voltage Balancing.**

I. INTRODUCTION

The modular multilevel converter (MMC) has been originally proposed for usage as high voltage direct current (HVDC) stations and has become the prevailing solution for these type of systems [1],[2]. Its modular design facilitates the manufacturing process and also provides scalability, easing the design of stations with different specifications. The MMC is also successfully employed in medium voltage applications, including energy storage systems, medium voltage drives, wind power and static compensation [3]–[6].

A typical MMC can be seen in Figure 1(a). It is built of series of submodules (SMs), commonly half-bridge (HB) or full-bridge (FB) converters. A series connection of several SMs constitutes an arm and two arms form a phase-leg. Each arm is connected to the circuit through an arm inductor L_a, whose main purpose is to limit circulating currents, and the converter is connected to the ac port through filter inductors L_f. The internal circuit of a half-bridge SM is also shown. Beside its main parts, the switching cell (S_1 and S_2) and the energy storage element C_i, in practice, there is need for other auxiliary circuits such as sensors, communication devices, gate drivers and an auxiliary power supply (APS) to power them.

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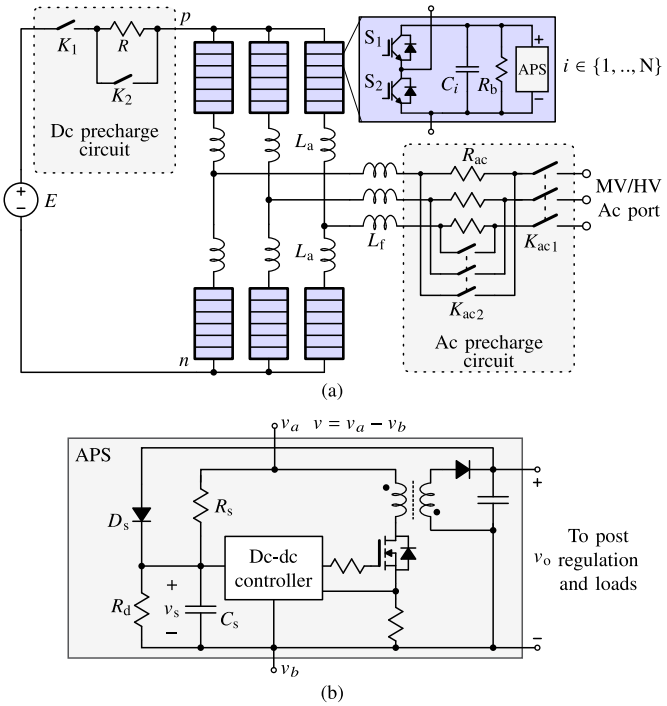


Fig. 1. (a) MMC converter and its ac and DC precharge circuits (adapted from [7]). (b) Simplified circuit of an APS based on a flyback converter.

The APSs can be fed either externally by a high-voltage isolated source or by their own SM capacitor [8],[9]. The cost and complexity of the APS is high when externally fed, since its insulation has to withstand medium/high voltages. It has to insulate the much lower SM capacitor voltage only when fed by the SM capacitor. However, test routines that can detect failures in the communication and control systems can only be executed after the main power connections are already made.

Independently of the type of APS, the MMC can only be connected to the grid, dc or ac, after the precharge of its capacitors to a certain voltage level that prevents inrush currents that could lead to damage. Different precharge schemes have been proposed by researchers, where some use an external low voltage source to charge the SMs one by one or in pairs, some precharge all SMs simultaneously by using series current limiting resistors and circuit breakers, either on the alternate current (AC) or direct current (DC) port, as shown in Figure 1 (a) [1], [10]–[12]. This work analyzes a solution of the last kind. First, the switch K_1 (Figure 1(a)) is closed, starting the precharge. Once the capacitor voltages is close enough to E, so that the parasitic resistances of the MMC and the DC side are sufficient to limit the current flow, K_2 is closed, bypassing the current limiting resistor R. A

balancing resistance R_b is connected in parallel with each SM capacitor to stabilize the operating point, since the constant power characteristic of the APSs introduce instability into the system [13]. This solution still has limitations involving the computation of the R_b value for a practical case [14]. These limitations are addressed in this work.

The precharge operation can be divided into three stages:

Uncontrolled and inactive – Starts with K_1 closing. Even though the switches S_1 and S_2 are kept off during this stage, current flows though the parallel diode of switch S_1 of each SM, charging the capacitors. Their voltage rise quickly to a magnitude around E/N, with E being the DC bus voltage and N the number of SMs per phase. The actual values depend mainly on the capacitance differences. The one with smallest capacitance ends with the highest voltage and the biggest capacitance ends with the lowest voltage. Such differences slowly decrease over time due to the balancing action of R_b. The APSs start turning on after a certain delay, which is dependent on their design and the tolerance of their components. As each APS turns on, all the capacitor voltages are disturbed due to the new configuration of currents in the circuit.

Uncontrolled and active – Starts when all APSs are on. Considering that each APS consumes a constant power, the resulting circuit configuration is known to be unstable [13]. A sufficiently low value of R_b, however, can counteract this effect and make the system stable [14].

Controlled – The capacitor voltages will be typically around half of the nominal value at the end of the preceding stage. This last stage is responsible for bringing the voltages to their nominal operating values by appropriately switching S_1 and S_2.

The aim of this work is to present an in-depth analysis of the stability of the *uncontrolled and active* stage of the precharge process and to provide a guideline for choosing R_b. The analysis is developed for one phase based on the system non-linear dynamics and is an extension of [7]. The paper is structured as follows. Section II presents models for the APS, which were absent in [7], and for the MMC phase-leg circuit during precharge. Section III presents an extension of the analysis introduced in [7] of the nonlinear dynamics of a MMC system with two SMs with the aim of providing insight about the system dynamics and stability. Section IV extends the proof of stability of the system operating point in the previous section for a system with N SMs. Section V shows simulation results, which, compared to [7], the variables are now normalized and equations for the design of R and R_b are now given. Section VI is totally new and provides a guideline for choosing R_b based on the simulation results of a high number of different cases that accounts for capacitance tolerances. Section VII presents new experimental results and the conluding remarks are presented in section VIII.

II. PRECHARGE STAGE MODEL

A. APS Model

The APS's purpose is to convert the submodule capacitor voltage (typically between 100's and 1000's of volts) to low voltages used to feed the internal circuits of the SM. A wide input operational voltage range is desirable, since it allows the control and communication circuits to be operational under abnormal conditions and early on during startup. Figure 1 (b) shows the simplified circuit of an APS based on a flyback converter, which is widely used in applications up to 1000 V due its simplicity and low cost. Operation at higher voltages is possible, but it requires series connection of semiconductors [15]. Only one output is shown in Figure 1 (b), but other windings could be added to the transformer to directly provide other voltage levels to feed the SM circuitry.

Independently of the topology used for the APS dc-dc converter, its own controller, usually composed of a integrated circuit and a few passives, needs a small amount of energy to start sending commands to the MOSFET before the APS as a whole starts working and can power itself. The APS startup circuit composed of R_s and C_s is responsible for providing that energy. Once there is sufficient voltage across C_i, C_s charges until v_s reaches the controller threshold voltage V_{th} and the dc-dc controller starts operation. The diode D_s turns on and the dc-dc controller is powered by the own output of the APS as soon as the output voltage v_o is higher than v_s. Resistor R_d is used here to approximately model any additional load that may be connected in parallel to C_s, including the dc-dc controller standby current. The behavior of this circuit is described by

$$\frac{\mathrm{d}v_s}{\mathrm{d}t} = \begin{cases} \dfrac{Fv - v_s}{\tau} & \text{if } v_s < V_{th} \\ 0 & \text{otherwise,} \end{cases} \tag{1}$$

where v is the APS input voltage, $F = R_d/(R_s + R_d)$ and $\tau = FC_sR_s$. This model neglects that v_s rises to v_o (ignoring the voltage drop across D_s) once the dc-dc converter has started. Since the variable of interest in this case is the APS startup time T_{st}, this is no major concern. Most of T_{st} is due to the charge of C_s. Thus, T_{st} can be approximated by the time it takes for v_s to reach V_{th}. Assuming that a voltage step of amplitude E/N is applied to the input of the APS, the startup time is found by solving (1) with zero initial condition and finding the instant at which $v_s = V_{th}$, which is

$$T_{st} = \tau \ln\left(\frac{1}{1 - \hat{V}_{th}}\right), \tag{2}$$

where $\hat{V}_{th} = V_{th}N/(EF)$. This and τ are the two parameters used to characterize the APS startup. Both can be calculated directly if one knows the APS circuit or can be estimated through curve fitting of experimental data.

The power P the APS consumes is expected to be ideally constant once it started operation since the consumption of its loads, the micro-controller and the auxiliary circuits, are mostly independent of time and capacitor voltage. Figure 2 shows the power consumed by the ten APSs used in this work when the capacitor voltage is varied. The APSs consume 10.9 W on average for 64 V $< v <$ 90 V that is the maximum expected range for the precharge voltage, whose nominal value is close to $E/N = 80\ V$. The minimum value is 10.72 W, 1.62% lower than average, and the maximum is 11.06 W, 1.5% higher than average.

Power consumption increases for $v >$ 90 V due to variations in the APS efficiency and the power dissipated in R_s, which increases quadratically with v. The output voltages of the APS

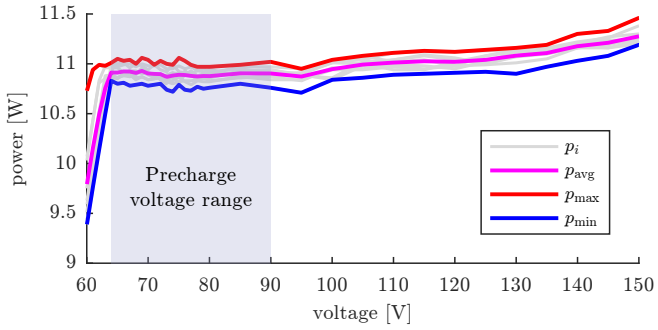


Fig. 2. Power consumption p_i, for $i \in \{1,..,10\}$, of the APSs used in this work as a function of SM capacitor voltage v. Average, maximum and minimum values are also shown.

fall when $v < 64$ V, making some of the SM circuits enter standby mode, rapidly decreasing consumption. In the range of interest, however, the APS consumes an almost constant power and can be approximately modeled by a power drain P.

B. Phase Leg Model

In order to understand the dynamics of the capacitor voltages v_i, and to find stability conditions for the operating point of the system, a model of the phase-leg of the MMC during the precharge process is derived. This is a model of the circuit in Figure 3 by neglecting the effect of L_a and corresponds to the stage 2 (uncontrolled and active) of the precharge. An adequate value for the balancing resistance R_b can be chosen by understanding the stability conditions. A phenomenological model is chosen, since the topology and the parameter values are known. In the case some value is unknown, it may be obtained through data fitting. Analysis of the resulting non-linear system is facilitated by choosing a state space representation.

The equivalent circuit of the MMC during the second stage of the precharge can be seen in Fig. 3. In this circuit, it can be obtained from Fig. 1 (a), when the circuit breaker switch K_1 is closed, K_2 is open, S_1 and S_2 for every SM are blocked, so the current flows through the anti-parallel diode of S_1. The circuit breaker switch K_{ac1} is open. The APSs in this stage are modeled as constant power drains.

The dynamics of L_a can be neglected if it is relatively small ($L_a \to 0$). On the dc side loop:

$$E - Ri_R - \sum_{k=1}^{N} v_k - 2L_a \frac{di_R}{dt} = 0. \tag{3}$$

So, if $L_a \to 0$, i_L can be approximated as

$$i_R \approx \frac{E - \sum_{k=1}^{N} v_k}{R}. \tag{4}$$

Taking these assumptions and applying the Kirchhoff's laws to the circuit, the state space model equations is derived as

$$\frac{dv_i}{dt} = \frac{1}{C}\left(\frac{E - \sum_{k=1}^{N} v_k}{R} - \frac{v_i}{R_b} - \frac{P}{v_i}\right). \tag{5}$$

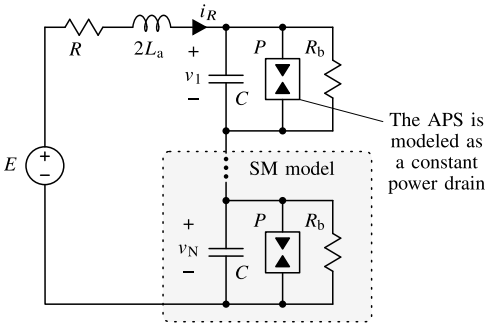


Fig. 3. Equivalent phase circuit during the *Uncontrolled and active* precharge stage.

with i $\in \{1,2,\ldots,N\}$. The voltages v_i are denoted by $\boldsymbol{v} = [v_1\, v_2 \ldots v_N]^T$.

III. STABILITY ANALYSIS OF TWO-SM SYSTEMS

In this section a two-dimensional case is analyzed, that is, (5) with two SM ($N = 2$). By doing that, one may gain insight on the system dynamics and some results can be extended for the N-dimensional case. This also allow one to use the phase plane tool to better understand the system dynamics. The system equilibrium points are calculated and conditions for stability of the operating point are derived, in which v_i are balanced. The system is represented by

$$\begin{bmatrix} \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{C}\left(\frac{E-(v_1+v_2)}{R} - \frac{P_1}{v_1} - \frac{v_1}{R_b}\right) \\ \frac{1}{C}\left(\frac{E-(v_1+v_2)}{R} - \frac{P_2}{v_2} - \frac{v_2}{R_b}\right) \end{bmatrix}. \tag{6}$$

A. Equilibrium Points

The system has four equilibrium points, computed as the solution for $\frac{dv_1}{dt} = 0$ and $\frac{dv_2}{dt} = 0$, given by

$$\boldsymbol{v}_{e1} = \left(\frac{ER_b + \sqrt{\alpha_{12}}}{2(R+2R_b)}, \frac{ER_b + \sqrt{\alpha_{12}}}{2(R+2R_b)}\right), \tag{7}$$

$$\boldsymbol{v}_{e2} = \left(\frac{ER_b - \sqrt{\alpha_{12}}}{2(R+2R_b)}, \frac{ER_b - \sqrt{\alpha_{12}}}{2(R+2R_b)}\right), \tag{8}$$

$$\boldsymbol{v}_{e3} = \left(\frac{ER_b + \sqrt{\alpha_{34}}}{2(R+R_b)}, \frac{ER_b - \sqrt{\alpha_{34}}}{2(R+R_b)}\right), \tag{9}$$

$$\boldsymbol{v}_{e4} = \left(\frac{ER_b - \sqrt{\alpha_{34}}}{2(R+R_b)}, \frac{ER_b + \sqrt{\alpha_{34}}}{2(R+R_b)}\right), \tag{10}$$

with

$$\alpha_{12} = E^2R_b^2 - 4PRR_b(R+2R_b), \tag{11}$$

$$\alpha_{34} = E^2R_b^2 - 4PR_b(R+R_b)^2. \tag{12}$$

The equilibrium points $\boldsymbol{v}_{e1}$ and $\boldsymbol{v}_{e2}$ are such that $v_1 = v_2$. As in $\boldsymbol{v}_{e1}$, the voltages are closer to E/N, $\boldsymbol{v}_{e1}$ is the operating point.

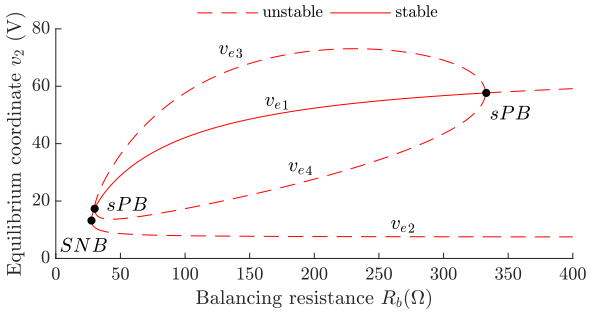
The equilibrium must fulfil the existence conditions $\alpha_{12} \geq 0$, for $\boldsymbol{v}_{e1}$ and $\boldsymbol{v}_{e2}$, and $\alpha_{34} \geq 0$, for $\boldsymbol{v}_{e3}$ and $\boldsymbol{v}_{e4}$. If $\alpha_{12} > 0$, $\boldsymbol{v}_{e1}$ and $\boldsymbol{v}_{e2}$ exist with independent coordinates. They collide if $\alpha_{12} = 0$ and they cease to exist if $\alpha_{12} < 0$. This characterize a saddle node bifurcation [16]. $\boldsymbol{v}_{e3}$ and $\boldsymbol{v}_{e4}$ exist in distinct coordinates if $\alpha_{34} > 0$. If $\alpha_{34} = 0$, they collide together with

$\boldsymbol{v}_{\mathbf{e}1}$ at

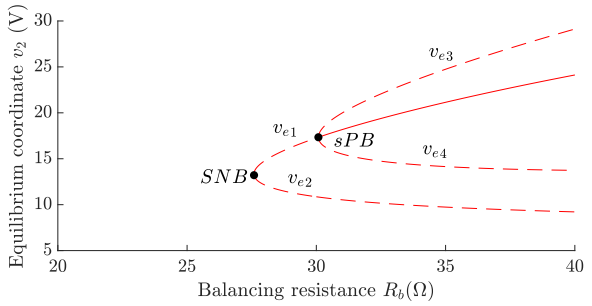
$$\boldsymbol{v} = \left(\frac{ER_\mathrm{b}}{2(R+R_\mathrm{b})}, \frac{ER_\mathrm{b}}{2(R+R_\mathrm{b})} \right), \tag{13}$$

and if $\alpha_{34} < 0$, $\boldsymbol{v}_{\mathbf{e}3}$ and $\boldsymbol{v}_{\mathbf{e}4}$ cease to exist, while $\boldsymbol{v}_{\mathbf{e}1}$ remains. This characterizes a pitchfork bifurcation [16]. The bifurcation kind allows one to infer about the equilibrium points stability. In this case, the existence of $\boldsymbol{v}_{\mathbf{e}4}$ and $\boldsymbol{v}_{\mathbf{e}3}$ is associated with the stability of $\boldsymbol{v}_{\mathbf{e}1}$.

The bifurcations are depicted in Figure 4. This diagram shows the geometric position (here the v_2 coordinate) of the equilibrium points in dependence with a varying parameter. In this case, R_b was chosen as the varying parameter. The saddle node bifurcation (SNB) occurs when $\alpha_{12} = 0$ and a subcritical pitchfork bifurcation (sPB) occurs when $\alpha_{34} = 0$. The stability of each the equilibrium point was calculated by linearizing the system around it for each R_b value, and then calculating the system Jacobian eigenvalues. It can be seen that the operating point $\boldsymbol{v}_{\boldsymbol{e}1}$ is locally stable for a certain R_b range. Its stability is studied in detail in the next section.



(a)



(b)

Fig. 4. Bifurcation diagram of (6) for R_b as the varying parameter in the range $[0,400]\Omega$ (for $E = 150$V, $R = 100\Omega$ and $P = 10$W). Full bifurcation diagram (a) and zoom around the saddle-node bifurcation (b).

B. Operating Equilibrium Point Stability

The equilibrium point $\boldsymbol{v}_{\mathbf{e}1}$ is stable if $det(\boldsymbol{A}|_{\boldsymbol{v}=\boldsymbol{v}\mathbf{e}_1}) > 0$ and $tr(\boldsymbol{A}|_{\boldsymbol{v}=\boldsymbol{v}\mathbf{e}_1}) < 0$ are verified, in which $\boldsymbol{A}$ is the Jacobian matrix of (6) in respect to $\boldsymbol{v}$, namely

$$\boldsymbol{A} = \begin{bmatrix} \frac{1}{C}\left(\frac{P}{v_1^2} - \frac{1}{R} - \frac{1}{R_\mathrm{b}}\right) & -\frac{1}{RC} \\ -\frac{1}{RC} & \frac{1}{C}\left(\frac{P}{v_2^2} - \frac{1}{R} - \frac{1}{R_\mathrm{b}}\right) \end{bmatrix}. \tag{14}$$

Defining V_b as the balanced voltage at the operating point, $\boldsymbol{v}_1 = (V_\mathrm{b}, V_\mathrm{b})$. Also, the expressions $det(\boldsymbol{A}|_{\boldsymbol{v}=\boldsymbol{v}_{\mathbf{e}1}}) > 0$ and $tr(\boldsymbol{A}|_{\boldsymbol{v}=\boldsymbol{v}_{\mathbf{e}1}}) < 0$, can be expressed as

$$\frac{V_\mathrm{b}^2}{R_\mathrm{b}} > P, \tag{15}$$

$$\frac{V_\mathrm{b}^2}{R_\mathrm{b}} > P - \frac{V_\mathrm{b}^2}{R}. \tag{16}$$

Since (15) is more restrictive than (16), it follows that (15) is the stability condition of $\boldsymbol{v}_{\mathbf{e}1}$. It means that the power consumed in R_b must be greater than P, consumed by an APS.

IV. STABILITY CONDITION FOR N-SM SYSTEMS

In this section, the results obtained in the previous one regarding the local stability of the operating point are generalized. Also, from these results it is shown how to choose appropriate values for R and R_b.

A system with N SM as shown in Section II.b is described by

$$\frac{\mathrm{d}v_i}{\mathrm{d}t} = \frac{1}{C}\left(\frac{E - \sum_{k=1}^{N} v_k}{R} - \frac{v_i}{R_\mathrm{b}} - \frac{P}{v_i} \right). \tag{17}$$

The analytic calculation of all its equilibrium points is a complex process and many times not feasible for high values of N, because it involves solving a system of N nonlinear equations. However, with a little knowledge about the physical behaviour of the system, it is possible to calculate the most important equilibrium point, the operating point, and infer about its stability.

At the operating point, the capacitor voltages must be balanced. That means it is on the line $v_1 = v_2 = \cdots = v_N$. This invariant straight line in fact satisfies $\frac{d\boldsymbol{v}_i}{dt} = \boldsymbol{0}$, so there is an equilibrium point $\boldsymbol{v}_{\boldsymbol{e}1} = (V_b, V_b, \ldots, V_b)$ on it, with V_b being the balanced voltage at the operating point. For the system to work as desired, this point must also be stable.

As in the previous case, the Jacobian $\boldsymbol{A}$ can be computed. It is the symmetric matrix[1]

$$\boldsymbol{A} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1N} \\ a_{21} & a_{22} & \cdots & a_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ a_{N1} & a_{N2} & \cdots & a_{NN} \end{bmatrix}, \tag{18}$$

whose elements are defined by

$$a_{ij} = \begin{cases} \frac{1}{C}\left(-\frac{1}{R} + \frac{P}{v_i^2} - \frac{1}{R_\mathrm{b}}\right) & , \text{if } i = j \\ -\frac{1}{RC} & , \text{if } i \neq j \end{cases} \tag{19}$$

The eigenvalues of such a matrix can be calculated, knowing that a matrix $\boldsymbol{M}$ in such a form

$$m_{ij} = \begin{cases} D & , \text{if } i = j \\ O & , \text{if } i \neq j \end{cases} \tag{20}$$

[1]A matrix $\boldsymbol{A}$ is symmetric if $\boldsymbol{A} = \boldsymbol{A}^T$.

has the following eigenvalues[2]

$$\lambda_1 = \lambda_2 = \cdots = \lambda_{N-1} = D - O \tag{21}$$

$$\lambda_N = D + (N-1)O. \tag{22}$$

That way the eigenvalues of $\boldsymbol{A}|_{\boldsymbol{v}=\boldsymbol{v_{e1}}}$ are

$$\lambda_1 = \lambda_2 = \cdots = \lambda_{N-1} = \frac{1}{C}\left(\frac{P}{V_\mathrm{b}^2} - \frac{1}{R_\mathrm{b}}\right) \tag{23}$$

$$\lambda_N = \frac{1}{C}\left(-\frac{N}{R} + \frac{P}{V_\mathrm{b}^2} - \frac{1}{R_\mathrm{b}}\right). \tag{24}$$

From these, the following stability conditions are obtained:

$$\frac{V_\mathrm{b}^2}{R_\mathrm{b}} > P, \tag{25}$$

$$\frac{V_\mathrm{b}^2}{R_\mathrm{b}} > P - \frac{NV_\mathrm{b}^2}{R}. \tag{26}$$

As (25) is more restrictive than (26) for choosing the maximum value of R_b, (25) is enough to guarantee $\boldsymbol{v_{e1}}$ local stability. Note that it is the same as (15) from the two-dimensional case.

Based on (25), the appropriate R_b value can be calculated. First, defining the parameter γ as

$$\gamma = \frac{1}{P}\frac{V_\mathrm{b}^2}{R_\mathrm{b}}, \tag{27}$$

so the operating point $\boldsymbol{v_{eo}}$ is stable for $\gamma > 1$. Then, V_b is computed from (27) as a function of γ, by solving

$$E - Ri_{LR} - NV_\mathrm{b} = 0 \tag{28}$$

$$NV_\mathrm{b} i_{La} = (1+\gamma)PN, \tag{29}$$

where (28) is the Kirchhoff voltage law applied to the dc loop and (29) is the power consumed in the N SM when the system is at $\boldsymbol{v_{eo}}$, considering that the APS power consumption is P and the consumption in R_b is γP . Both (28) - (29) are calculated at the equilibrium point $\boldsymbol{v_{e1}}$. The solution corresponding to the operating point, closer to E/N, is

$$V_\mathrm{b} = \frac{E + \sqrt{E^2 - 4R(1+\gamma)PN}}{2N}. \tag{30}$$

Whenever $E^2 - 4R(1+\gamma)PN > 0$. Once V_b and γ have been chosen, R_b and R are found with

$$R_\mathrm{b} = \frac{V_\mathrm{b}^2}{\gamma P}, \tag{31}$$

$$R = \frac{EV_\mathrm{b} - NV_\mathrm{b}^2}{P(1+\gamma)}. \tag{32}$$

These values of R and R_b assure that $\boldsymbol{v_{e1}}$ is locally stable, as long as the V_b existence condition is satisfied.

It is indispensable to remark, though, that choosing the barely sufficient value of $\gamma > 1$ for $\boldsymbol{v_{eo}}$ to be local stable is not necessarily enough for the system to operate as desired. The initial conditions of the system, when it reaches this precharge stage, must be inside the attraction domain of $\boldsymbol{v_{e1}}$. How to choose an appropriate value of γ is investigated in the following section.

For the analysis carried out in the next sections, (5) is considered in a normalized form given by

$$\frac{\mathrm{d}\hat{v}_i}{\mathrm{d}\hat{t}} = \frac{\hat{R}_\mathrm{b}}{\hat{R}}\left(N - \sum_{k=1}^{N} v_k\right) - \frac{\hat{R}_\mathrm{b}}{\hat{v}_i} - \hat{v}_i, \tag{33}$$

for i $\in \{1, 2, \ldots, N\}$. System (33) is obtained by applying the standard change of variables (state and time) and parameters defined in Table I to the original system (5). Note that E/N is chosen for the voltage base, i.e., the ideal precharge value.

TABLE I
Normalized variables and parameters.

Variables and time			Parameters		
Original	Norm.	Base	Original	Norm.	Base
v	$\hat{v}$	E/N	V_b	$\hat{V}_\mathrm{b}$	E/N
v_s	$\hat{v}_s$	FE/N	V_th	$\hat{V}_\mathrm{th}$	FE/N
t	$\hat{t}$	$R_\mathrm{b}C$	τ	$\hat{\tau}$	$R_\mathrm{b}C$
			λ	$\hat{\lambda}$	$1/(R_\mathrm{b}C)$
			P	1	P
			R, R_b	$\hat{R}$, $\hat{R}_\mathrm{b}$	$E^2/(PN^2)$

V. NUMERICAL RESULTS

In this section, two simulated study cases are considered when: (i) a locally stable operating point is at $\boldsymbol{v_{e1}}$, and (ii) an unstable equilibrium point is at $\boldsymbol{v_{e1}}$. Phase portraits and corresponding time responses are shown in order to evaluate the dynamic behavior of the study system. The influence of the variation of γ or R_b in their attraction regions is also investigated.

A. Stable operating equilibrium point case

This case, referred here as case (i), was simulated for the normalized parameter values $\hat{R} = 7,81 \times 10^{-3}$ and $\hat{R}_\mathrm{b} = 894 \times 10^{-3}$. These correspond to parameters in a prototype available in our laboratory (see Table III), and corresponding $V_\mathrm{b} = 0.991$ and $\gamma = 1.1$. The resulting phase portrait can be seen in Figure 5(a), where four equilibrium points can be observed. Their corresponding eigenvalues and eigenvectors are listed in Table II. The operating point, $\boldsymbol{v_{e1}}$, is a stable node, since both of its eigenvalues are real negative. The equilibrium point $\boldsymbol{v_{e2}}$ is an unstable node since its eigenvalues are real positive. Since $\boldsymbol{v_{e2}}$ is close to the origin, in this case it has little influence in the system dynamics, because with low voltages like that, the APSs are still turned off. $\boldsymbol{v_{e3}}$ and $\boldsymbol{v_{e4}}$ are saddle points (unstable), because both have a positive and a negative eigenvalue each.

The saddle points $\boldsymbol{v_{e3}}$ and $\boldsymbol{v_{e4}}$ have stable asymptotes, lines drawn in green. These are associated with the negative eigenvalue and are tangent to the corresponding eigenvector of the saddle points, shown in Table II. A trajectory starting over these lines will reach them. Any other will diverge from them. These asymptotes, although very difficult to

[2]These eigenvalues were calculated for several N values with the aid of a symbolic computation tool.

reach in a practical case, delimit the attraction domain of $\boldsymbol{v}_{\mathbf{e}1}$, represented by the green shaded region in Fig. 5(a). Any trajectory with initial conditions inside this domain will reach $\boldsymbol{v}_{\mathbf{e}1}$ in finite time. That means the capacitor voltages will balance. Any trajectory starting outside it, will go towards the unstable asymptotes of $\boldsymbol{v}_{\mathbf{e}1}$ and $\boldsymbol{v}_{\mathbf{e}4}$, associated with the positive eigenvalue and are tangent to its corresponding eigenvector. In practice, that means the capacitor voltages diverge, until they reach a upper or lower voltage threshold that cause the whole system to turn off for safety reasons.

An example of convergent and divergent trajectory can be seen respectively in Fig. 5(b) and Fig. 5(c). The convergent trajectory starts inside $\boldsymbol{v}_{\mathbf{e}1}$ attraction domain and reaches $\boldsymbol{v}_{\mathbf{e}1}$. It has a fast and a slow dynamic. The fast is associated with $\boldsymbol{v}_{\mathbf{e}1}$ eigenvalue with highest value, λ_1 and corresponding eigenvector $\mathbf{w}_1$, whose direction is in this case associated with the total voltages in the capacitors. The slow one is associated with the eigenvalue with lowest value, λ_2 and $\mathbf{w}_2$, whose direction is associated with the balancing between v_1 and v_2. One can see in the time response—from 0 until 0.2 s, that the sum of the capacitor voltages rapidly reach values close to 1. Then, it takes about 200 s to balance v_1 and v_2.

The divergent trajectory time response is represented in Fig. 5 (c). The initial conditions start outside the attraction domain of $\boldsymbol{v}_{\mathbf{e}1}$. The capacitor voltages rise together fast in the first instants and then diverge until $\boldsymbol{v}_{\mathbf{e}2}$ reaches close to zero and the simulation stops. These dynamics, fast and slow, are associated with the eigenvalues and eigenvectors of $\boldsymbol{v}_{\mathbf{e}3}$ and $\boldsymbol{v}_{\mathbf{e}4}$ in an analogous way as the trajectory depicted in Fig. 5(b) and the eigenvalues and eigenvectors of $\boldsymbol{v}_{\mathbf{e}1}$.

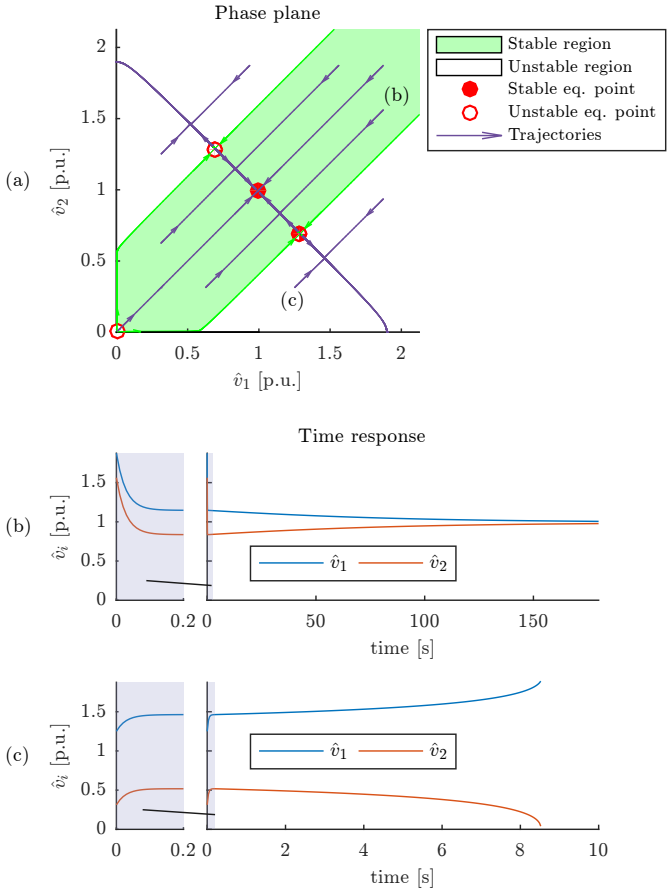


Fig. 5. Phase portrait of system (6) with stable $\boldsymbol{v}_{\mathbf{e}1}$ (for $\gamma = 1.1$, $\hat{R} = 7{,}81 \times 10^{-3}$ and $\hat{R}_\mathrm{b} = 894 \times 10^{-3}$.) (a) and corresponding converging and diverging time responses, respectively (b) and (c). Adapted from [7]

.

B. *Unstable operating equilibrium point case*

The normalized parameters values are $\hat{R} = 7.81 \times 10^{-3}$ and $\hat{R}_\mathrm{b} = 1.095$ for the unstable operating point case, refered here as case (ii). The normalized resistance $\hat{R}$ is the same used in the previous case and $\hat{R}_\mathrm{b}$ corresponds to a $V_\mathrm{b} = 0.991$ and $\gamma = 0.9$. The phase portrait of system (6) can be seen in Fig. 6(a). Only $\boldsymbol{v}_{\mathbf{e}1}$ and $\boldsymbol{v}_{\mathbf{e}2}$ exist in this case. By looking their eigenvalues in Table II, it can be seen that $\boldsymbol{v}_{\mathbf{e}1}$ is a saddle point (unstable).

The equilibrium point $\boldsymbol{v}_{\mathbf{e}1}$ as a stable asymptote. In this case, the trajectory will reach $\boldsymbol{v}_{\mathbf{e}1}$ if the initial conditions start at it. The time response corresponding to this case is in Fig. 6(b). This, however, is not feasible in a practical case, where there are uncertainties in the initial conditions, system parameters or even disturbances that would take the system away from its operating point. A closer to a real case time response is depicted in Figure 6(c). The voltages rise up together, then start to diverge, and the simulation stops when

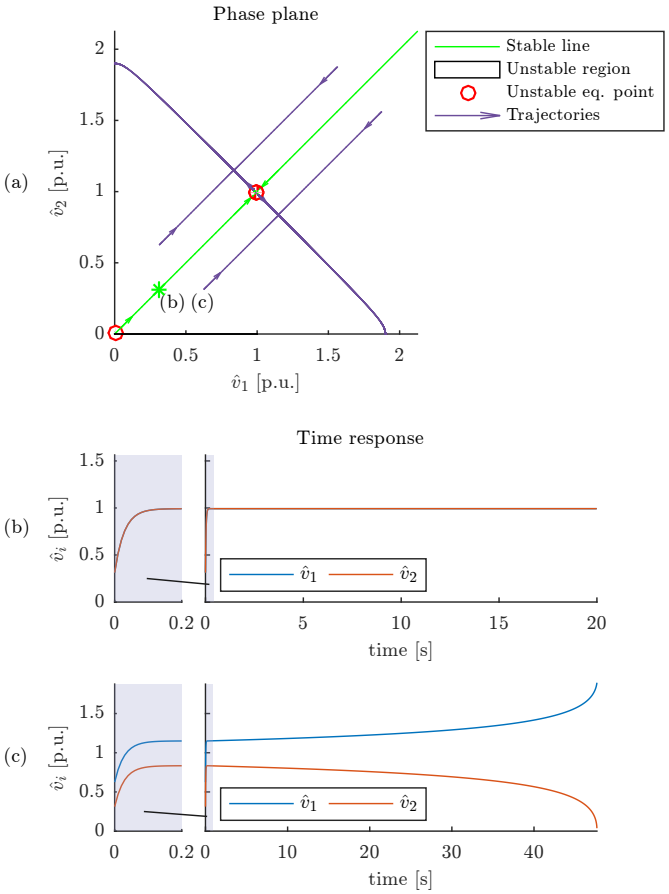


Fig. 6. Phase portrait of system (6) with stable $\boldsymbol{v}_{\mathbf{e}1}$ (for $\gamma = 1.1$, $\hat{R} = 7.81 \times 10^{-3}$ and $\hat{R}_\mathrm{b} = 1.095$) (a) and corresponding converging and diverging time responses, respectively (b) and (c). Adapted from [7]

.

TABLE II
Normalized equilibrium points coordinates and associated normalized eigenvalues and eigenvectors from linearized system at these points, for both stable and unstable operation point simulated cases.

Case	Normalized Equilibrium Point	$(\hat{v}_1, \hat{v}_2)$	$\hat{\lambda}_1$	$\hat{\lambda}_2$	$\hat{\mathbf{w}}_1$	$\hat{\mathbf{w}}_2$
(i)	$\hat{\boldsymbol{v}}_{\mathbf{e}1}$	$(0.991, 0.991)$	-228	-0.0909	$[1\ 1]^T$	$[-1\ 1]^T$
	$\hat{\boldsymbol{v}}_{\mathbf{e}2}$	$(0.00392, 0.00392)$	579	581	$[1\ 1]^T$	$[-1\ 1]^T$
	$\hat{\boldsymbol{v}}_{\mathbf{e}3}$	$(1.28, 0.693)$	-228	0.200	$[1.00\ 1]^T$	$[-0.994\ 1]^T$
	$\hat{\boldsymbol{v}}_{\mathbf{e}4}$	$(0.693, 1.28)$	-228	0.200	$[0.994\ 1]^T$	$[-1.00\ 1]^T$
(ii)	$\hat{\boldsymbol{v}}_{\mathbf{e}1}$	$(0.992, 0.992)$	-280	0.111	$[1\ 1]^T$	$[-1\ 1]^T$
	$\hat{\boldsymbol{v}}_{\mathbf{e}2}$	$(0.00392, 0.00392)$	70900	71100	$[1\ 1]^T$	$[-1\ 1]^T$

v_2 collapses to 0.

C. Attraction domain of the operating equilibrium point

Figure 7 depicts the location of the stable asymptotes of the saddle points $\boldsymbol{v}_{\boldsymbol{e}2}$ and $\boldsymbol{v}_{\boldsymbol{e}3}$ for several γ values(and its corresponding $\hat{R}_\mathrm{b}$), for $\hat{R} = 7.81 \times 10^{-3}$, the same as the previous cases. For $\gamma > 1$, they define the limits of the attraction domain of $\boldsymbol{v}_{\boldsymbol{e}1}$. The equilibrium points $\boldsymbol{v}_{\boldsymbol{e}2}$ and $\boldsymbol{v}_{\boldsymbol{e}3}$ move away from each other, increasing the attraction domain area, as γ increases. However, the greater the γ is, the less their distance increases for a same increment in γ.

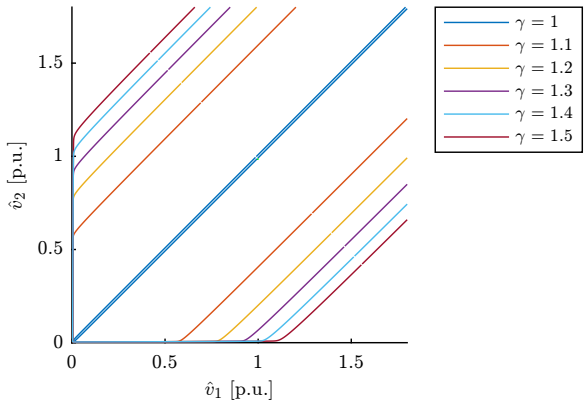


Fig. 7. Stable asymptotes of $\boldsymbol{v}_{\mathbf{e}2}$ and $\boldsymbol{v}_{\mathbf{e}3}$ as a function of γ, for $\hat{R} = 7.81 \times 10^{-3}$. Adapted from [7].

VI. GUIDELINES FOR CHOOSING γ

The parametric combination that leads to the worst initial condition for $N = 3$ and higher values of N are analyzed in this section. It also discusses how to choose an appropriate value for γ in order to ensure a successful precharge, i.e., that all voltages converge to the desired equilibrium point.

A. Inclusion of Stage 1 Model

The spread of initial conditions, which define whether the capacitor voltages will converge or not, is mainly a consequence of variations in the parameters of the SMs. If all SMs are completely equal, all voltages will be always equal and all APSs turn on at the same time. Capacitors have the widest tolerances among the main components that form a SM. Thus, the tolerance of C and C_s, the SM and the APS capacitors, as the the main parameter, are chosen for a certain MMC design—that means, for a certain combination of N, $\hat{V}_\mathrm{b}$, $\hat{V}_\mathrm{th}$ and $\hat{\tau}$, that defines how large γ has to be to ensure the convergence of the capacitor voltages.

From now on, it is assumed that each capacitance has a different value, represented by $C_i = (1+\delta_i)C$ and $C_{\mathrm{s}i} = (1+\delta_{\mathrm{s}i})C_\mathrm{s}$. The effect of having different capacitors C_i is clear, i.e., the resulting v_i voltages are inversely proportional to C_i if the same current flows through all capacitors. Different voltages v_i in association with varied $C_{\mathrm{s}i}$ values result in different startup times. The rate of change $\mathrm{d}v_i/\mathrm{d}t$ is higher, in absolute values, for the SMs whose APS are already on. This may lead to a high dispersion in v_i depending on the capacitance configuration as shown later. The normalized model (5) is augmented with the dynamics of the startup circuit (1), also normalized, in order to capture these phenomena. Thus,

$$\begin{aligned}
\frac{\mathrm{d}\hat{v}_i}{\mathrm{d}\hat{t}} &= \frac{1}{1+\delta_i}\left[\frac{\hat{V}_\mathrm{b}{}^2(1+\gamma)}{\gamma N\left(\hat{V}_\mathrm{b}-\hat{V}_\mathrm{b}{}^2\right)}\left(N-\sum_{k=1}^{N}\hat{v}_k\right)-\frac{\gamma\hat{v}_i}{\hat{V}_\mathrm{b}{}^2}-\frac{s_i}{\hat{v}_i}\right] \\
\frac{\mathrm{d}\hat{v}_{\mathrm{s}i}}{\mathrm{d}\hat{t}} &= (1-s_i)\frac{\hat{v}_i-\hat{v}_{\mathrm{s}i}}{(1+\delta_{\mathrm{s}i})\hat{\tau}} \\
s_i &= \begin{cases} 0 & \text{if } \hat{v}_{\mathrm{s}i} < \hat{V}_\mathrm{th} \\ 1 & \text{otherwise.} \end{cases}
\end{aligned} \tag{34}$$

The resistances $\hat{R}$ and $\hat{R}_\mathrm{b}$ in equation (5) have been rewritten in terms of the normalized desired balanced voltage $\hat{V}_\mathrm{b}$ and γ with the help of (31) and (32) and the normalization described in Table I. The capacitance relative variations δ_i and $\delta_{\mathrm{s}i}$ have also been included. The auxiliary variable s_i indicates when the i-th APS is on ($s_i = 1$) or off ($s_i = 0$). The parameters present in (34) are N, $\hat{V}_\mathrm{b}$, $\hat{\tau}$, $\hat{V}_\mathrm{th}$ and the relative capacitance variations δ_i and $\delta_{\mathrm{s}i}$. Now it is possible to verify whether a certain γ would result in balanced capacitor voltages by plugging in values for the other parameters in (34) and solving it numerically.

A binary search algorithm has been implemented in order to find which minimum value of γ would be enough to insure the convergence of v_i for a certain parametric combination. The algorithm works similarly to the bisection method, but instead of testing a function for its sign, it tests if the solution of (34) has reached balance or not [17]. An absolute tolerance of 0.001 for γ is used as stopping criterion. The model is solved for the interval $0 \le \hat{t} \le T_\mathrm{s} = 40$. The precharge is considered successful when $\max(|\hat{v}_i(T_\mathrm{s}) - \mathrm{avg}(\hat{v}_i(T_\mathrm{s}))|) <$

$0.001 \cdot \text{avg}(\hat{v}_i(T_s))$ and no $\hat{v}_i$ falls bellow 0.45 at any instant of time.

B. Minimum γ for $N \in \{3,..,6\}$

A discrete range for each parameter of (34) was defined, since different MMC designs are possible. This covers most of the reasonable implementations whose APSs can modeled as presented in this work. The used values were,

$$\begin{aligned} \hat{\boldsymbol{\tau}} &= \begin{bmatrix} 0.556 & 0.927 & 1.928 & 1.669 & 2.04 \end{bmatrix} \\ \hat{\boldsymbol{V}}_{\mathbf{th}} &= \begin{bmatrix} 0.07 & 0.211 & 0.352 & 0.493 & 0.634 \end{bmatrix} \\ \hat{\boldsymbol{V}}_{\mathbf{b}} &= \begin{bmatrix} 0.94 & 0.957 & 0.975 & 0.9925 \end{bmatrix} \\ \boldsymbol{N} &= \begin{bmatrix} 3 & 4 & 5 & 6 \end{bmatrix}. \end{aligned} \tag{35}$$

There is a certain capacitance combination that leads to the worst case or the highest γ_m (minimum value of γ that ensures balancing) for each parametric combination. A discrete range for values for the capacitance variations is assumed and all non-repeated combinations are tested to find this point. The discrete values are $\delta_i \in \{-\Delta, -\Delta + \frac{2\Delta}{N_m - 1}, .., \Delta\}$ and $\delta_{si} \in \{-\Delta, -\Delta + \frac{2\Delta}{N_s - 1}, .., \Delta\}$, where N_m is the number of values tested for C_i, N_s is the number of values tested for C_{si} and Δ is the capacitance tolerance. A capacitor combination vector is defined as

$$\boldsymbol{c}_n = \begin{bmatrix} 1+\delta_1 & \cdots & 1+\delta_N \mid 1+\delta_{s1} & \cdots & 1+\delta_{sN} \end{bmatrix}. \tag{36}$$

This combination is assumed to be repeated if another combination $\boldsymbol{c}_p$ has been already tested, which can be obtained by permutations on the columns of $\boldsymbol{c}_n$ that preserves the distance between the u-th and the $(u+N)$-th elements, for $u \in \{1,..,N\}$, or, in other words, that only changes the position of the SMs, but maintain their internal composition δ_i and δ_{si}. The number of possible compositions for a SM is $N_m N_s$ that constitute the set S. Thus, the number of different capacitor combinations for N submodules is given by the number of multi-subsets (a subset with repeated elements) with N elements that can be obtained from S. This number is given by the binomial coefficient

$$N_{\text{comb}} = \binom{N_m N_s + N - 1}{N}, \tag{37}$$

[18]. For $N_m = 4$ and $N_s = 2$, the values used in this work, there are 120 non-repeated capacitor combination vectors for $N = 3$, 330 for $N = 4$, 792 for $N = 5$ and 1716 for $N = 6$. Testing all combinations for higher values of N becomes impractical due the long computation time. The goal of testing for these small values of N, which are unrealistic for real applications, is to find whether there is a trend for the worst capacitance vector. The simulations were performed for $\Delta = 0.2$. Considering the values used for the other parameters, 295800 cases were tested in total.

The simulations results showed that γ_m has little sensitivity to $\hat{V}_b$ within the adopted range. The maximum absolute change in γ_m caused by a variation in $\hat{V}_b$ among all cases tested was from 1.748 ($\hat{V}_b = 0.9925$) to 1.787 ($\hat{V}_b = 0.94$), an increase of 2.2% for the case $N = 6$, $\hat{\tau} = 2.04$ and $\hat{V}_{th} = 0.63$. For every combination of N, $\hat{\tau}$ and $\hat{V}_{th}$ tested, the same worst capacitance vector was found for all values of $\hat{V}_b$.

Figure 8 summarizes the simulation results. The second row of graphics shows how γ_m varies with $\hat{\tau}$ and $\hat{V}_{th}$ for the different values of N. The highest γ_m that results from the worst combination of $\boldsymbol{c}$ and $\hat{V}_b$ is shown for each pair $(\hat{\tau}_x, \hat{V}_{thy})$. The colored matrices show that the minimum γ_m values happen for elements close to the anti-diagonal of the matrices and that the way γ_m varies with $\hat{\tau}$ and $\hat{V}_{th}$ is very similar for all tested N, although the values of γ_m scale up as N increases. The highest γ_m always occurs for the minimum values of both $\hat{\tau}$ and $\hat{V}_{th}$ for the elements below the anti-diagonal. This combination is defined as the worst fast case (WFC), to which there is an associated γ_{mf}. For the elements above the anti-diagonal, the highest γ_m, called γ_{ms} in allusion to the worst slow case (WSC), always happens for the maximum values of both $\hat{\tau}$ and $\hat{V}_{th}$.

The first row of graphics in Figure 8 shows how the worst capacitance combination changes with $\hat{\tau}$ and $\hat{V}_{th}$. All WFCs are associated to the same structure of capacitance combination, described by

$$\boldsymbol{c}_{wf} = \begin{bmatrix} 1+\Delta & 1-\Delta & \cdots & 1-\Delta \mid 1-\Delta & 1+\Delta & \cdots & 1+\Delta \end{bmatrix}. \tag{38}$$

In words, the WFCs are associated with a configuration of SMs where one has the highest possible C and the lowest C_s, and all other SMs have the opposite configuration. On the other hand, all WSCs are associated with the following configuration,

$$\boldsymbol{c}_{ws} = \begin{bmatrix} 1-\Delta & 1+\Delta & \cdots & 1+\Delta \mid 1-\Delta & 1+\Delta & \cdots & 1+\Delta \end{bmatrix}. \tag{39}$$

Which means that there is one SM with minimum values for C and C_s, and all others have maximum values for both capacitances.

The relative distance d_{Cxy}, given by

$$d_{Cxy} = \frac{2}{\pi} \text{atan}\left(\frac{\left\| \hat{\boldsymbol{c}}_{wxy} - \hat{\boldsymbol{c}}_{wf} \right\|}{\left\| \hat{\boldsymbol{c}}_{wxy} - \hat{\boldsymbol{c}}_{ws} \right\|} \right), \tag{40}$$

where $\hat{\boldsymbol{c}} = \boldsymbol{c}/\|\boldsymbol{c}\|$, is used as a measure of how close the worst capacitance combination $\boldsymbol{c}_{wxy}$ is to $\boldsymbol{c}_{wf}$ or $\boldsymbol{c}_{ws}$. d_{Cxy} is 0 for $\boldsymbol{c}_{wxy} = \boldsymbol{c}_{wf}$, and goes towards 1 when $\boldsymbol{c}_{wxy}$ approaches $\boldsymbol{c}_{ws}$. The first row of Figure 8 shows that most tested cases are associated with $\boldsymbol{c}_{wf}$, but the worst capacitance combination quickly and smoothly changes to $\boldsymbol{c}_{ws}$ as the WSC is approximated. Both $\boldsymbol{c}_{wf}$ and $\boldsymbol{c}_{ws}$ have the same configuration for the C_{si} values, as all worst capacitance combinations found for the other cases. Only the configuration of C_i have changed among them.

Figure 9 shows the time responses of the WFC (a) and the WSC (b) for $N = 3$. The systems enter stage 2 (all APSs on) at 0.074 s in (a), and at 2.57 s in (b). As expected for the fast case, v_1, the capacitor voltage of the SM with bigger C, is smaller. If all three SMs had the same value for C_s, the APSs of SMs 2 and 3 would turn on first due the higher v_i, and that would help balance the voltages, since v_2 and v_3 would start decreasing, making v_1 increase. However, as C_{s1} is smaller than C_{s2} and C_{s3}, all APSs start operation at approximately the same time, making the system enter stage 2 with heavily

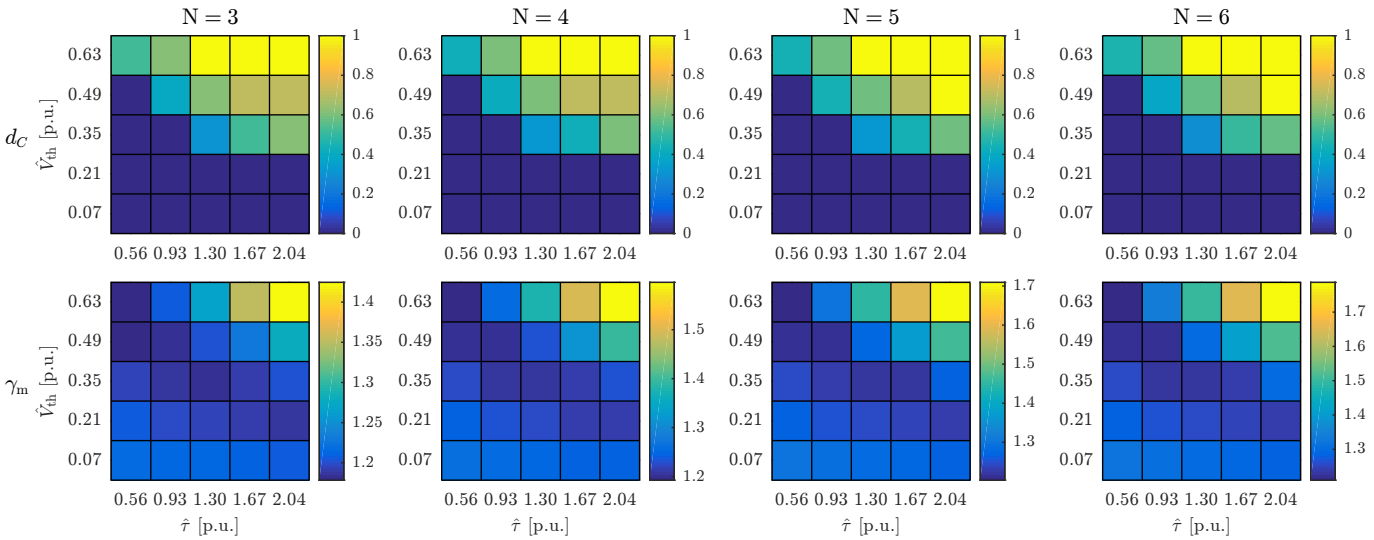


Fig. 8. The first row of graphics shows how the worst capacitor combination varies with the normalized threshold voltage $\hat{V}_{\text{th}}$ and precharge time constant $\hat{\tau}$ for $N \in \{3,..,6\}$. d_C measures how close the worst capacitance vector $\boldsymbol{c}_{\text{w}xy}$ is to $\boldsymbol{c}_{\text{wf}}$ ($d_{\text{C}} = 0$) or to $\boldsymbol{c}_{\text{ws}}$ ($d_{\text{C}} = 1$). The second row shows how γ_{m} varies for the same cases.

unbalanced voltages. For the slow case, the smaller C_1 and $C_{\text{s}1}$ cause the APS of SM 1 to turn on much earlier due to the higher voltage at its inputs and lower time constant τ. Voltage v_1 falls until the others APSs start operation after the turn on, which takes much longer due the higher C_{s}. The voltage conditions have reversed by the time APSs 2 and 3 turn on: v_1 is much smaller than v_2 and v_3, a state similar to the WFC when stage 2 begins.

The worst combinations of $\hat{\tau}$ and $\hat{V}_{\text{th}}$ (WFC and WSC) have also been tested for lower capacitance tolerances $\Delta \in \{0.5, 0.1, 0.15\}$. All tested cases resulted in the same worst capacitor combinations $\boldsymbol{c}_{\text{wf}}$ or $\boldsymbol{c}_{\text{ws}}$. However, as expected, lower γ_{mf} and γ_{ms}.

C. Extrapolation forHigher N

Since it becomes impractical to simulate all capacitor combinations for N higher than a few dozens, only the WFC and WSC previously found to be the worst cases for $N \in \{3,..,6\}$ are considered in this section. Although the simulation results are suggestive, it is important to emphasize that this work does not prove that $\boldsymbol{c}_{\text{wf}}$ and $\boldsymbol{c}_{\text{ws}}$ in association with $(\hat{\tau}_1, \hat{V}_{\text{th}1})$ and $(\hat{\tau}_5, \hat{V}_{\text{th}5})$, respectively, will also be the worst cases for any other N different from the values tested.

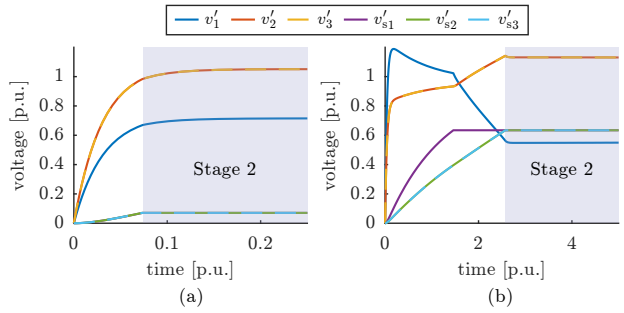


Fig. 9. Time responses of the (a) worst fast case and the (b) worst slow case for $N = 3$. The voltages converge at $\hat{t} = 40$, but only the first instants are shown.

The vectors $\boldsymbol{c}_{\text{wf}}$ and $\boldsymbol{c}_{\text{ws}}$ have an important characteristic in common. They describe configurations where only one SM is different from all the others. This can be used to simplify (34), since now it is necessary to model only two different dynamics, one being related to the distinct SM and the other associated with the remaining $N-1$ submodules. As two states are needed to model one SM, four state variables are necessary to model the system, given by

$$\begin{aligned}
\frac{\mathrm{d}\hat{v}_i}{\mathrm{d}\hat{t}} &= \frac{1}{1+\delta_i}\left[\frac{\hat{V}_{\text{b}}{}^2(1+\gamma)}{\gamma N\left(\hat{V}_{\text{b}}-\hat{V}_{\text{b}}{}^2\right)}(N-\hat{v}_1-(N-1)\hat{v}_2)-\frac{\gamma\hat{v}_i}{\hat{V}_{\text{b}}{}^2}-\frac{s_i}{\hat{v}_i}\right]\\
\frac{\mathrm{d}\hat{v}_{\text{s}i}}{\mathrm{d}\hat{t}} &= (1-s_i)\frac{\hat{v}_i-\hat{v}_{\text{s}i}}{(1+\delta_{\text{s}i})\hat{\tau}}\\
s_i &= \begin{cases} 0 & \text{if } \hat{v}_{\text{s}i} < \hat{V}_{\text{th}} \\ 1 & \text{otherwise,} \end{cases}
\end{aligned} \tag{41}$$

where now $i \in \{1,2\}$. For the WFC, the normalized capacitances are given by $\delta_1 = 1+\Delta$, $\delta_2 = 1-\Delta$, $\delta_{\text{s}1} = 1-\Delta$ and $\delta_{\text{s}2} = 1+\Delta$. For the WSC, they are $\delta_1 = 1-\Delta$, $\delta_2 = 1+\Delta$, $\delta_{\text{s}1} = 1-\Delta$ and $\delta_{\text{s}2} = 1+\Delta$.

The same binary search algorithm described previously has been used to find γ_{mf} and γ_{ms}. The results are shown in Figure 10. Each curve in the graph shows how γ_{mf} or γ_{ms} varies with the number of SMs N for a certain capacitance variation $\Delta \in \{0.05, 0.01, .., 0.2\}$. For each case, the same range for the desired equilibrium voltage $\hat{V}_{\text{b}} \in \{0.94, 0.9575, .., 0.9925\}$ was tested and the highest resulting γ_{m} was chosen. As already seen on the tests with smaller number of SMs, γ_{m} increases with N, with a higher sensitivity to this parameter for $N \leq 100$. The capacitance variation Δ, as expected, also significantly impacts γ_{m}, which increases for higher values of Δ.

In practice, most of the real cases are expected to have a combination of $\hat{\tau}$ and $\hat{V}_{\text{th}}$ that lies between the values defined

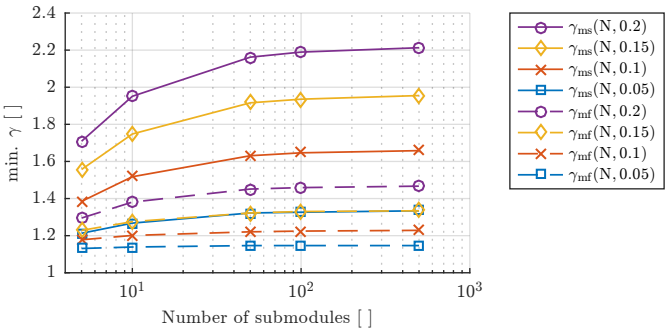


Fig. 10. Minimum γ needed to ensure voltage balancing for the worst fast case (γ_{mf}) and for the worst slow case (γ_{ms}), as functions of the number of SMs N and capacitance variation Δ.

for the WFC and the WSC, resulting in a γ_m located between γ_{mf} e γ_{ms}. Since the way γ_m varies between its extremes for variations in $\hat{\tau}$ and $\hat{V}_{th}$ is unknown, the solution is to use a value higher than the worst case, which is always γ_{ms} for a certain N and Δ. This results in a sub-optimal solution in terms of dissipated power, but is the best approximation attained so far.

Once a suitable γ has been found with the help of Figure 10 and a value for $\hat{V}_b$ has been chosen within the range defined by the maximum and minimum values shown in (35), R and R_b can be calculated with (31) and (32). Then, one must check if $\hat{\tau}$, whose base value used for normalization depends on R_b, is really within the range defined by the maximum and minimum values of $\hat{\boldsymbol{\tau}}$ in (35).

Depending on the power dissipated in R_b, it could impact the efficiency and thermal design of the whole system, especially in smaller power ratings. However, it would be possible to switch on the resistor through an appropriate electronic circuit at the beginning of the precharge and off at the end, eliminating any power loss due to the balancing resistor after the precharge.

VII. EXPERIMENTAL RESULTS

A MMC prototype with 10 SMs per phase was used to verify the passive balancing method explored in this work. Due to limitations in the hardware, only the single-phase configuration has been tested. The main converter parameters are shown in Table III, while a picture of the prototype can be seen in Figure 11. The tolerances of C and C_s are

TABLE III
Parameters of the MMC prototype .

N [ ]	E [V]	C [mF]	P [W]	τ [s]	V_{th} [V]	F [ ]
10	800	2.82	10.9	1.63	16	0.35

20%, according to the datasheets. For this value of Δ, from Figure 10, $\gamma = 1.96$ is needed to ensure that all capacitor voltages converge to V_b, whose chosen value was 76 V ($\hat{V}_b = 0.95$). The values of R_b and R were found with (31) and (32), resulting in $R_b = 270.4\ \Omega$ and $R = 94.2\ \Omega$. Due to limitations in the hardware, the values $R_b = 375\ \Omega$ and $R = 100\ \Omega$ have been used instead, resulting in $\hat{V}_b = 0.957$ and $\gamma = 1.43$. Figure 10 shows that the maximum Δ that could be compensated with this value of γ is close to 10%. However, the γ_{ms} values

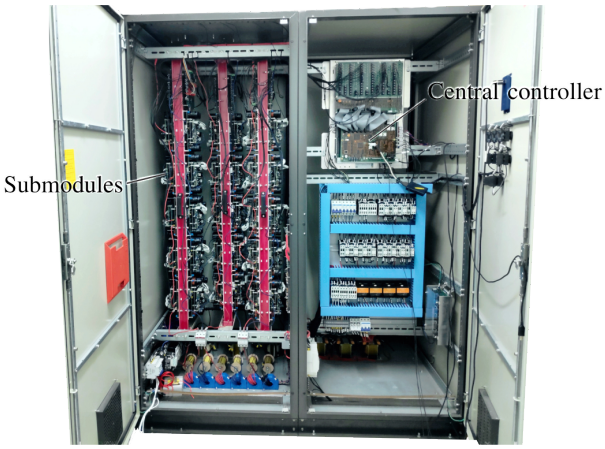


Fig. 11. Picture of the prototype used to obtain the experimental results [7].

presented in Figure 10 are exact only for the worst slow case (WSC), which is characterized by the capacitor combination $\boldsymbol{c}_{ws}$, $\hat{\tau} = 2.04$ and $\hat{V}_{th} = 0.634$. Once the value used for R_b is known, the actual $\hat{\tau}$ can be calculated with Table I, which gives $\hat{\tau} = 1.85$. The normalized threshold voltage is $\hat{V}_{th} = V_{th}N/(EF) = 0.57$. Since these values are smaller than the ones from the WSC, the actual minimum γ needed is expected to be smaller than the value given by Figure 10. To find the exact value, all capacitor combinations have been tested for the prototype parameters with the algorithm described in section VI for $\Delta \in \{0.05, 0.1, 0.15, 0.2\}$. Since only one combination of parameters was tested, the total number of simulations, 77792, is still feasible. The results show that the worst capacitance combination is $\boldsymbol{c}_{ws}$ for all values of tested Δ, but the minimum γ are 1.22, 1.39, 1.57 and 1.72, respectively. Comparing this result with the value used, $\gamma = 1.43$, it can be inferred that the combination of resistors used would be enough to ensure voltage balancing for the worst capacitance combination $\boldsymbol{c}_{ws}$ for some Δ between 10% and 15%.

The Figure 12 shows the capacitor voltages during the precharge phase of the converter for two values of R_b. In Figure 12 (a), $R_b = 500\ \Omega$, resulting in $\hat{V}_b = 0.963$ and $\gamma = 1.09$, while Figure 12 (b) shows the results for the already mentioned value $R_b = 375\ \Omega$, which has associated $\hat{V}_b = 0.957$ and $\gamma = 1.43$. Each voltage shown was obtained from the own SM acquisition system. Since it is not working before the correspondent APS starts operation, the capacitor voltage is unknown and is shown as zero. The dispersion in the SM parameters, specially C and C_s, results in the system entering stage 2 with diverse capacitor voltages and APSs turning on at different instants.

The second stage initial conditions for the case with $\gamma = 1.09$ lie outside the domain of attraction of the desired equilibrium point, leading the capacitor voltages to unbalance. One of the voltages falls until it finds another equilibrium due the power consumption decrease for $v < 64$ V shown in Figure 2. Even though the micro-controller is still working, other systems of the SM are not supplied with a proper voltage and the system will enter a protection state once it tries to start switching.

The second case shown in Figure 12(b) has a sufficiently large $\gamma = 1.43$ to ensure the convergence of the voltages

after it enters stage 2. The final voltages spread within the range $[73.5, 77.4]$ V, $[-3.2\%, +2.0\%]$ in respect to the average 75.89 V, which is less than 1% away from the predicted V_b. Standard deviation in steady state is $\sigma_\mathrm{ss} = 1.7\%$. This unbalance is probably caused by the dispersion in the values of P and R_b and uncertainties in the measurements. The chances of the capacitors used in the prototype having the exact worst configuration with values on the limits of the stated tolerances is very low. That is why the precharge is successful even though the used γ is smaller than the minimum estimated.

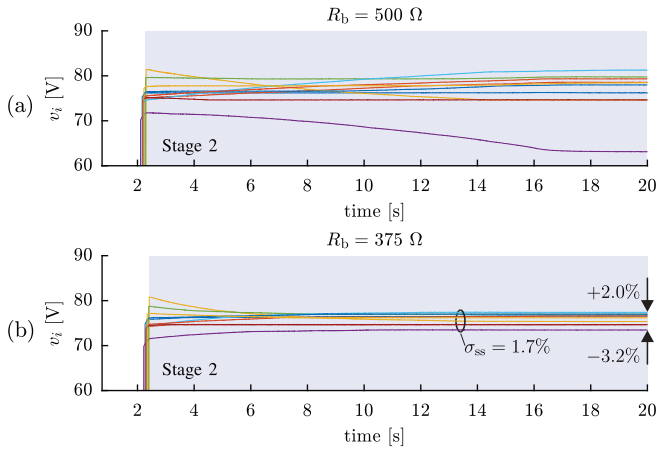


Fig. 12. Capacitor voltages during precharge for (a) $R_\mathrm{b} = 500\ \Omega$ ($\hat{V}_\mathrm{b} = 0.963$, $\gamma = 1.09$) and (b) $R_\mathrm{b} = 375\ \Omega$ ($\hat{V}_\mathrm{b} = 0.96$, $\gamma = 1.43$).

VIII. CONCLUSIONS

The natural instability of the MMC precharge procedure has been analyzed in this work. An in-depth case study with two SMs, although not realistic, allowed the nonlinear dynamics of the system to be understood and suggests a strategy for the choice of the balancing resistor R_b for a higher number of SMs. The resistance R_b defines how large the attraction domain of the desired equilibrium point is, or, in other words, how balanced the capacitor voltages must be when the system initiates the second precharge stage in order to ensure that they will converge and balance. These initial condition unbalances are mainly affected by the tolerance of the SM capacitor and of the APS startup circuit capacitor.

A normalized precharge model for a MMC converter has been proposed. Only four parameters, besides the capacitance tolerance, are used: the number of SMs, the desired final precharge voltage and the APS related parameters, the threshold voltage and startup circuit time constant. This model is solved numerically inside an algorithm that finds the minimum γ (relationship between the power dissipated in the balancing resistor and the power consumed by the APS) that ensures voltage convergence for a certain combination of parameters. Running this algorithm for all possible capacitor combinations for low values of N showed that there are two worst cases that lead to higher values of γ. The worst fast case is related to a low $\hat{V}_\mathrm{th}$, low $\hat{\tau}$ and a certain capacitance combination $\boldsymbol{c}_\mathrm{wf}$, while the worst slow case are related to a high $\hat{V}_\mathrm{th}$, high $\hat{\tau}$ and capacitance combination $\boldsymbol{c}_\mathrm{ws}$. Both combinations have only one SM different from all others. These two cases are assumed to be the worst cases also for higher values of N, reducing an unfeasible number of algorithm runs to only two per converter parameter combination. This allows one to estimate a minimum necessary γ as a function of only the number of SMs and the capacitance tolerance Δ. However, this number is conservative. Firstly, because it assumes the worst combination of $\hat{V}_\mathrm{th}$ and $\hat{\tau}$, which may not be the case for the design in hand, but was a necessary assumption to make the analysis feasible. Secondly, because it does not take into account the most plausible capacitor combination, but assumes it to be the worst.

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REFERENCES

[1] A. Lesnicar, R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range", *in Proc. IEEE Bologna Power Tech*, vol. 3, p. 6 pp., Jun. 2003, doi:10.1109/PTC.2003.1304403.

[2] H. J. Knaak, "Modular multilevel converters and HVDC/FACTS: A success story", *in Proc. 14th European Conf. Power Electronics and Applications*, pp. 1–6, Aug. 2011, URL: `https://ieeexplore.ieee.org/abstract/document/6020674`.

[3] A. Lachichi, "Modular multilevel converters with integrated batteries energy storage", *in 2014 International Conference on Renewable Energy Research and Application (ICRERA)*, pp. 828–832, Oct. 2014, doi:10.1109/ICRERA.2014.7016501.

[4] A. G. Siemens, Nuremberg, Germany, "Sinamics Perfect Harmony GH150", [Online], 2019, URL: `https://assets.new.siemens.com/siemens/assets/public.1564669468.18aa6fa6-7bfa-450a-8328-2cfe787e8844.gh150acbrochurejune2019.pdf`.

[5] J. Lyu, X. Cai, M. Molinas, "Optimal Design of Controller Parameters for Improving the Stability of MMC-HVDC for Wind Farm Integration", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 40–53, Mar. 2018, doi:10.1109/JESTPE.2017.2759096.

[6] T. Geyer, G. Darivianakis, W. van der Merwe, "Model predictive control of a STATCOM based on a modular multilevel converter in delta configuration", *in Proc. 17th European Conf. Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1–10, Sep. 2015, doi:10.1109/EPE.2015.7309148.

[7] L. H. Schmidt, G. J. de Sousa, M. L. Heldwein, D. J. Pagano, "Passive Capacitor Voltage Balancing in Modular Multilevel Converter During its Precharge: Analysis and Design", *in 2019 IEEE 15th Brazilian Power Electronics Conference*

and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), pp. 1–6, IEEE, 2019, doi:10.1109/COBEP/SPEC44138.2019.9065701.

[8] D. Cottet, F. Agostini, T. Gradinger, R. Velthuis, B. Wunsch, D. Baumann, W. Gerig, A. Rüetschi, D. Dzung, H. Vefling, *et al.*, "Integration technologies for a medium voltage modular multi-level converter with hot swap capability", *in Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4502–4509, Sep. 2015, doi:10.1109/ECCE.2015.7310295.

[9] G. Lambert, F. Seidel, L. V. Fiorio, Y. R. de Novaes, "Insulated Modular Auxiliary Power Source Concept With Multiple Outputs", *Eletrônica de Potência*, vol. 24, no. 2, pp. 139–146, Jun. 2019, doi:10.18618/REP.2019.2.0043.

[10] K. Tian, B. Wu, S. Du, D. Xu, Z. Cheng, N. R. Zargari, "A Simple and Cost-effective Precharge Method for Modular Multilevel Converter by Using a Low-Voltage DC source", *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5321–5329, Sep. 2015, doi:10.1109/TPEL.2015.2484222.

[11] L. Zhang, J. Qin, X. Wu, S. Debnath, M. Saeedifard, "A Generalized Precharging Strategy for Soft Startup Process of the Modular Multilevel Converter-Based HVDC Systems", *IEEE Transactions on Industry Applications*, vol. 53, no. 6, pp. 5645–5657, Nov. 2017, doi:10.1109/TIA.2017.2736958.

[12] B. Li, D. Xu, Y. Zhang, R. Yang, G. Wang, W. Wang, D. Xu, "Closed-Loop Precharge Control of Modular Multilevel Converters During Start-Up Processes", *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 524–531, Feb. 2015, doi:10.1109/TPEL.2014.2334055.

[13] L. Luo, Y. Zhang, L. Jia, N. Yang, "A Novel Method Based on Self-Power Supply Control for Balancing Capacitor Static Voltage in MMC", *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1038–1049, Feb. 2018, doi:10.1109/TPEL.2017.2679130.

[14] J. Li, B. Zhao, Q. Song, Y. Huang, W. Liu, "Minimum Voltage Tracking Balance Control Based on Switched Resistor for Modular Cascaded Converter in MVDC Distribution Grid", *IEEE Transactions on Industrial Electronics*, vol. 63, no. 9, pp. 5437–5441, Sep. 2016, doi:10.1109/TIE.2016.2586755.

[15] Y. Han, W. Chen, X. Chen, X. Ma, Y. Sha, X. Yang, X. Li, "A 4000V input auxiliary power supply with series connected SiC MOSFETs for MMC-based HVDC system", *in Proc. IEEE 8th Int. Power Electronics and Motion Control Conf. (IPEMC-ECCE Asia)*, pp. 279–284, May 2016, doi:10.1109/IPEMC.2016.7512299.

[16] S. H. Strogatz, *Nonlinear dynamics and chaos*, Westview Press, 2nd Edition, Cambridge, 2000.

[17] J. D. F. Richard L. Burden, *Numerical Analysis*, BROOKS COLE PUB CO, 9th ed., Boston, USA, 2011.

[18] T. Cleveland, *Number Theory*, EDTECH, 1st. ed., Waltham Abbey, United Kingdom, 2018.

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