HIGH-VOLTAGE GAIN DC-DC CONVERTER FOR PHOTOVOLTAIC APPLICATIONS IN DC NANOGRIDS

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Abstract – **Photovoltaic (PV) systems used in DC Nanogrids present prominent advantages associated with low maintenance need and operation costs. Owing to the low output voltage of the PV module, highly efficient high-voltage gain DC-DC converters are required for connection with the DC nanogrid. This work presents a novel DC-DC converter topology with current source characteristic for PV applications and current injection in DC nanogrids. The introduced converter uses coupled inductors and switched capacitors to achieve high voltage gain with low component count and without using extreme duty ratios. Besides, the main switch is turned on with nearly zero current, thus contributing to minimized switching losses. The qualitative and quantitative analyzes of the circuit are presented in detail and a prototype rated at 200 W is developed and evaluated in the laboratory. Experimental results demonstrate efficient renewable energy conversion, where the maximum efficiency is 96.8%.**

Keywords – **DC Nanogrids, Grid connected, High Step-up DC–DC converter, High voltage gain, Photovoltaic (PV).**

I. INTRODUCTION

The continuous evolution of semiconductor technology has allowed the improved use of DC distribution systems [1]–[7], with consequent increase of efficiency due to the lack of ac-DC converters typically required to provide power factor correction [5].

By definition, a DC nanogrid is a DC distribution system where one or more DC energy sources, e.g., photovoltaic modules, fuel cells, DC generators, among others, provide power to a DC bus in low power plants [8], [9].

A DC nanogrid can operate in standalone mode or connected to a local power grid. It is also possible to distribute energy through an ac bus, i.e., ac nanogrid, or using a hybrid approach [10]–[14].

Since most renewable energy sources operate with DC quantities, as well as energy storage devices (ESDs) and often electronic loads, DC nanogrids become more efficient, due to less energy conversion stages [5], with prominent advantages over their ac counterparts [15]–[18].

The use of photovoltaic (PV) systems in DC nanogrids is quite attractive due to the low maintenance and operating [9]. In this context, DC buses rated at 380 V are widely employed in several applications [19]–[21]. Since the PV modules typically provide low voltages rated between 20 V and 50 V, the series connection of PV modules is employed to obtain higher voltages, which allows the use of basic DC-DC converters in the interconnection between PV modules and the DC bus [22]. In such conditions, partial or total shading can compromise the operation at the maximum power point (MPP) [23]. Therefore, the use of high-voltage gain DC-DC converters is an alternative, since it allows the individual tracking of the MPP in each module, thus optimizing the extraction of power and bringing system modularity.

Several high-voltage gain DC-DC converter topologies have been proposed so far in the literature [8], [9], [24]–[32] Among the existing approaches the extend conversion range, cascaded converters, voltage multipliers, multilevel converters, interleaved converters, switched capacitors and coupled inductors can be highlighted [33]–[35]. The use of coupled inductors has drawn significant attention, since it allows obtaining a high static gain while using few components in the power circuit. However, if the turns ratio is high, the voltage across the output diode will also be. In addition, resonance between the leakage inductance and the intrinsic capacitance of the output diode may cause overvoltage on the active switch, thus leading to the need of clamping circuits [36], [37].

A circuit composed of a diode and a capacitor was employed in [36] to provide the active clamping of the voltage across the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), as the energy associated with the leakage inductance can be absorbed. A family of high-voltage gain converters based on coupled inductors and distinct configurations for the clamping capacitor was introduced in [37]. Besides, the leakage inductance is used to control the falling rate of the current through the output diode, thus minimizing reverse recovery issues. The use of clamping capacitors associated with distinct positions in a coupled-inductor-based boost converter was also analyzed in [38], as the voltage stresses on the capacitors are minimized without changing the operating principle of the converter.

Most high-voltage gain converters described in the literature have an output with voltage source characteristic.

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Therefore, an eventual voltage disturbance in the DC bus can cause current peaks in the output of the converter and reduce the life of the capacitors [39]. In addition, devices connected to the same bus operating at different frequencies may cause beat frequency oscillations [39]. In this context, DC-DC converters with current source characteristic at the output has the output current limited by output inductor, allowing the converter to be connected to a voltage bus without generating current peaks and oscillations that can cause instability.

This work proposed a non-isolated DC-DC conversion for high-voltage step-up for PV system applications and current injection in DC nanogrids. The main advantages lie in low component count and use of the leakage inductance associated with the coupled inductors to provide nearly zero current switching (ZCS), leading to minimized switching losses. The stores energy is then recovered, thus avoiding high voltage spikes on the switch and increasing the converter efficiency.

II. CONVERTER ANALYSIS

A. Circuit Description

The proposed converter is shown in Figure 1. The coupled inductances $\boldsymbol{L_P}$ e $\boldsymbol{L_S}$ are replaced by the simplified model of a transformer in Figure 3.a, which allows analyzing the influence of the leakage inductances. The number of turns of the primary and secondary windings in the ideal transformer are given by $\boldsymbol{N_1}$ and $\boldsymbol{N_2}$, respectively. The magnetizing inductance of the transformer corresponds to $\boldsymbol{L_m}$, while the leakage inductances are $\boldsymbol{L_{KP}}$ and $\boldsymbol{L_{KS}}$. The circuit composed of capacitor C_3 and diode D_2 clamp the voltage across the main switch S_1, thus absorbing the energy stored in L_{KP} and allowing the use of switches with lower rated voltages and consequently reduced conduction losses. The switched capacitors C_1 and C_2 provide higher voltage gain to the converter and damp the resonance associated with the leakage inductances and the intrinsic capacitances of diodes D_1 and D_2. The swichting frequency of S_1 is f_S. The output side of the converter have current source characteristic provided by L_o in series with the output stage represented by a constant voltage V_o. The converter operates in continuous conduction mode (CCM) since the current through the magnetizing inductance L_M does not become null over the switching period. The main theoretical waveforms are presented in Figure 2, while the operation modes are detailed in Figure 3.

B. Operation Stages

In order to perform the qualitative analysis, capacitances C_1, C_2, and C_3 are considered large enough so that their respective voltages are constant with negligible ripple. All semiconductors are considered to be ideal and the converter operates in CCM according to Figure 3.

Mode 1 $(\boldsymbol{t_0 - t_1})$: Switch S_1 is turned on under nearly ZCS condition. The current through D_1 decreases as limited by L_{KS}, being the diode reverse biased at t_1 with zero current. Inductors L_m and L_{KP} store the energy supplied by V_{IN}. Diodes D_2 and D_3 remain reverse biased. Capacitors C_1, C_2, and C_3 provide energy to L_o and V_o. This mode finishes when the current through D_1 becomes null.

Mode 2 $(\boldsymbol{t_1 - t_2})$: Diodes D_1 and D_2 are reverse biased at t_1, while both S_1 and D_3 are on. Due to the magnetic coupling, the magnetizing inductance is responsible for charging C_2, whose voltage depends on the turns ratio between N_1 and N_2. Inductances L_m, L_{KP}, L_{KS}, and L_o store energy. Capacitors C_1, C_2, and C_3 provide energy to the DC bus of the nanogrid. This mode finishes when S_1 is turned off.

Mode 3 $(\boldsymbol{t_2 - t_3})$: Switch S_1 is turned off at t_2, while the polarity of the voltage across the inductors is inverted. Diode D_1 is reverse biased. Diode D_2 is forward biased and the energy stored in L_{KP} is transferred to C_3, as the voltage across the switch is clamped with reduced voltage spikes. The current through D_3 decreases according to a rate defined by L_{KS}, as the diode is turned off under ZCS condition and this mode finishes.

Mode 4$(\boldsymbol{t_3 - t_4})$: Both S_1 and D_3 are off at t_3. Diode D_1 is forward biased as the current through it is limited by L_{KS}. Diode D_2 is still forward biased, thus allowing C_3 to be completely charged. Besides, the voltage across C_1 is proportional to the sum of the voltages across the primary and secondary windings. Inductor L_o provides energy to the output stage. This mode finishes when D_2 is reverse biased.

Mode 5 $(\boldsymbol{t_4 - t_5})$: Only diode D_1 remains forward biased. Capacitor C_1 is still charged, while C_2, C_3, and L_o provide energy to the output stage. This mode finishes when S_1 is turned on.

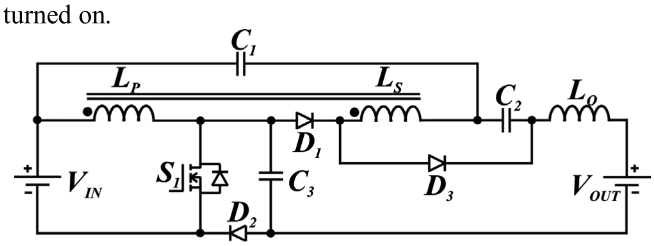


Fig. 1. Proposed coupled inductor based converter.

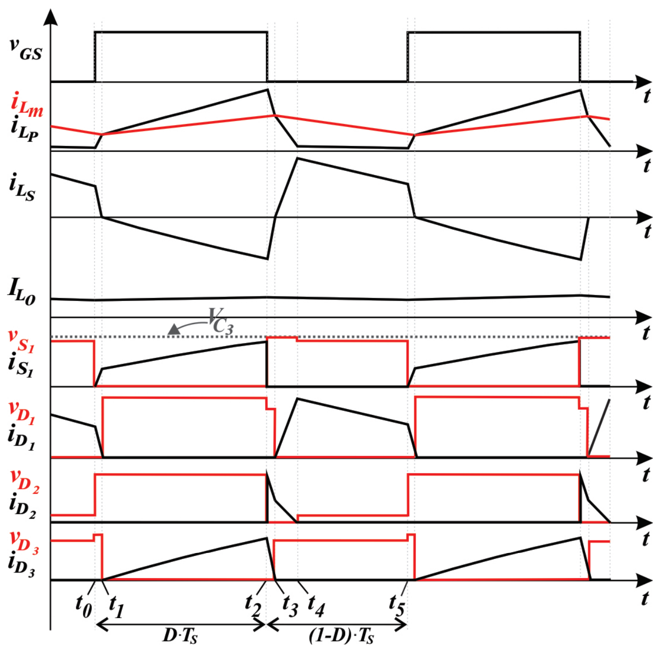


Fig. 2. Main theoretical waveforms of the proposed DC-DC converter.

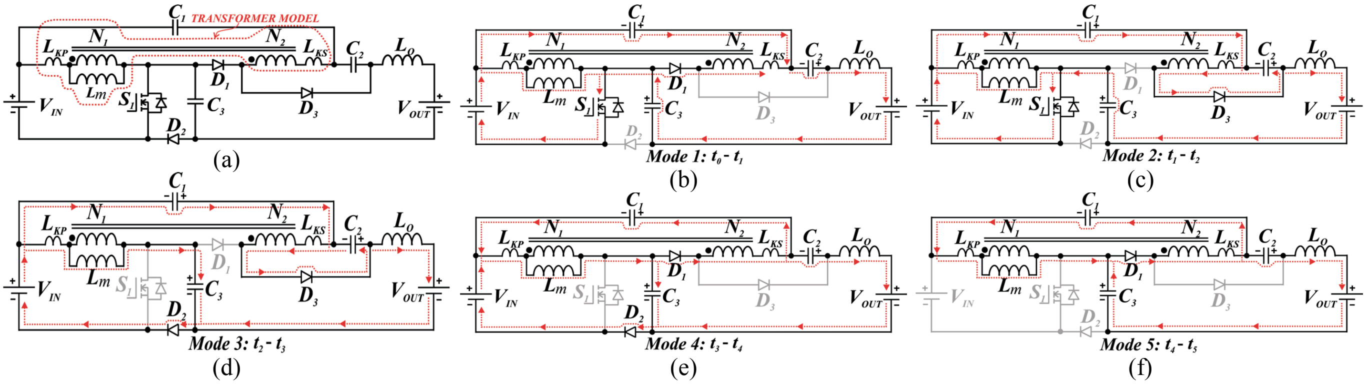


Fig. 3. (a) Circuit employing an ideal transformer model representing the coupled inductors. Operation modes of the proposed DC-DC converter: (b) Mode 1 ($\boldsymbol{t_0 - t_1}$); (c) Mode 2 ($\boldsymbol{t_1 - t_2}$); (d) Mode 3 ($\boldsymbol{t_2 - t_3}$); (e) Mode 4 ($\boldsymbol{t_3 - t_4}$); (f) Mode 5 ($\boldsymbol{t_4 - t_5}$).

C. Static Gain

In order to determine the static gain, switch S_1 is assumed to be on during $D \cdot T_s$ and off during $(1\text{-}D) \cdot T_s$, where D is the duty cycle and T_s is the switching period. The turns ratio of the coupled inductors given by $\boldsymbol{n}$ is:

$$n = \frac{N_1}{N_2} \tag{1}$$

where:
N_1 – number of turns of the primary winding;
N_2 – number of turns of the secondary winding.

Some authors only consider the influence of the primary leakage inductance L_{KP}, while neglecting the secondary leakage inductance L_{KS} [26], [40], [41]. It is worth mentioning that L_{KS} is responsible for limiting the di/dt of the current through the active switch, being an important parameter for the circuit analysis. However, in order to simplify the calculatings, the secondary leakage inductance L_{KS} influence on static gain can be disconsidering. The coupling fator k can be defined [9]:

$$k = \frac{L_m}{L_m + L_{KP} + {L_{KS}}/{n^2}} \quad . \tag{2}$$

During the time interval defined by $D \cdot T_s$, the voltage across the magnetizing inductance is:

$$v_{L_m} = \frac{L_m}{L_m + L_{KP}} \cdot V_{IN} = k \cdot V_{IN} \tag{3}$$

where V_{IN} is the average input voltage.

The current through the secondary winding is much lower than that through the primary winding. Thus, the influence of L_{KS} on the charging process of capacitors C_1 and C_2 can be neglected. Then, the voltage across C_2 is:

$$V_{C_2} = k \cdot n \cdot V_{IN} \quad . \tag{4}$$

During the time interval defined by $(1\text{-}D) \cdot T_s$, the voltage across the magnetizing inductance is:

$$V_{L_m} = k \cdot \left(V_{C_3} - V_{IN} \right). \tag{5}$$

Besides, the voltage across secondary winding L_s is equivalent to the reflected voltage V_{Lm}, i.e.:

$$V_{L_S} = k \cdot n \cdot \left(V_{C_3} - V_{IN} \right). \tag{6}$$

The average voltage across L_m is null during T_s, resulting in:

$$\int_0^T v_{L_m}(t)dt = \int_0^{DT} v_{L_m}(t)dt + \int_{DT}^{T} v_{L_m}(t)dt = 0 \, . \tag{7}$$

Substituting (3) and (5) in (7) it is possible to determine the average voltage across C_3 as:

$$. \; V_{C_3} = \frac{1}{1-D} \cdot k \cdot V_{IN} \tag{8}$$

When switch S_1 is ed off, capacitor C_1 is charged with the sum of the voltages across the primary and secondary windings, i.e.:

$$V_{C_1} = k \cdot \left(V_{C_3} - V_{IN} \right) + \left(k \cdot n \cdot \left(V_{C_3} - V_{IN} \right) \right). \tag{9}$$

Substituting (8) in (9), it is possible to determine V_{C1} $\boldsymbol{V_{C_1}}$:

$$V_{C_1} = \frac{V_{IN} \cdot D}{1-D} \cdot (1+n) \cdot k \tag{10}$$

The average output voltage V_{OUT} corresponds to the sum of the voltages across C_1, C_2, and C_3:

$$V_{OUT} = \left(\frac{V_{IN} \cdot D \cdot (1+n) \cdot k}{1-D} + V_{IN} \cdot n \cdot k + \frac{k \cdot V_{IN}}{1-D} \right). \tag{11}$$

Rearranging (11), the static gain M can be obtained in the form:

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{1 + (D+n) \cdot k}{1-D} \, . \tag{12}$$

Considering the ideal model in Figure 1.a, the static gain can be determined for k=1 as:

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{1+D+n}{1-D} \, . \tag{13}$$

The voltage clamping on S_1 is provided by C_3. Thus, for k=1 the voltage across S_1 can be determined substituting (13) in (8):

$$v_{S_1} = V_{C_3} = \frac{V_{IN}}{1-D} = \frac{V_{OUT}}{1+D+n} \, . \tag{14}$$

Figure 4.a presents a gain curve of the boost converter and the gain static curves of proposed converter for different coupling factor values.

The equations (15), (16), (17) and (18) calculate the minimum value of the capacitors and the output inductor of the converter. The converter switches were chosen according to the voltage and current efforts.

$$C_1 = \frac{I_O \cdot (1-D)}{f_s \cdot \Delta V_C \cdot V_{IN} \cdot D \cdot (1+n)} \tag{15}$$

$$C_2 = \frac{I_O}{f_s \cdot \Delta V_C \cdot n \cdot V_{IN}} \tag{16}$$

$$C_3 = \frac{I_O \cdot (1-D)}{f_s \cdot \Delta V_C \cdot V_{IN}} \tag{17}$$

$$L_O = \frac{V_{IN} \cdot D^2}{(1-D) f_s \cdot \Delta I_{Lo}} \tag{18}$$

where:

$\boldsymbol{\Delta V_C}$ – Maximum percentage voltage ripple in the capacitors;

$\boldsymbol{\Delta L_O}$ – Maximum percentage current ripple in the inductor L_O.

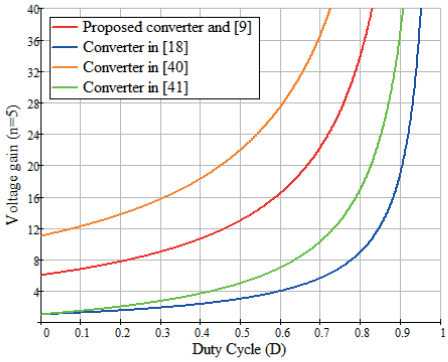


Fig. 4. Ideal static gain curves of the proposed converter and of the converters presented in table II.

TABLE I
Prototype Components Specifications

Parameter	Specifications
S_1	IRFB4310 (International Rectifier)
$D_1 = D_3$	IDT02S60C (Infineon)
D_2	STPS3150 (STMicroelectronics)
$C_1 = C_2$	2μF/400V (MKP-379 Vishay)
C_3	4 x (10μF/100V) Multilayer Ceramic – MLCC – SMD/X7R/12105C106KAT2A AVX/Kyocera
L_O	5 mH -NEE – MTT140EE3007 Magmattec
L_P / L_S	Core: MTT140EE4012 Magmattec $N_1\!:\!N_2 = \mathbf{11\!:\!55}/L_p = \mathbf{52\mu H}/L_s = \mathbf{1.4\,mH}$ $L_{KP} = \mathbf{657nH}/k = 0.987$

D. Comparison Among the Proposed Converter and Other Similar DC-DC Topologies

Table II presents a comparison of the proposed converter with the topologies presented in [9], [18], [40], [41]. Some criteria were considered to select the converters in table II: drive complexity, number of components, photovoltaic applications, high voltage gain and high efficiency. The converter introduced in [9] has current source characteristic at the output. However, it uses an extra diode and capacitor, what may lead to reduced efficiency. The converter proposed in [18] employs few components, but three active switches are necessary, with consequent increase of complexity associated with the drive circuitry. Besides, the output presents voltage source characteristic. A DC-DC interface converter for DC microgrids is described in [40], whose output behaves as a voltage source. Besides, an auxiliary clamping circuit is requited to limit the maximum voltage across the switch, while complexity is increased as a consequence. The high-voltage gain DC-DC converter proposed in [41] presents high efficiency, but the output has voltage source characteristic. Two active switches are also employed in the power stage, resulting in increased cost and reduced robustness. The converter proposed in this manuscript has few components, only one switch which reduces the complexity of activation and output with a current source characteristic which helps in reducing problems associated with the beat frequency [39].

The photovoltaic modules have parasitic capacitances distributed throughout the panel, intrinsic to the manufacture. In the presence of voltage at the terminals of the panel, the load stored by these capacitances can flow through the common point of the system, generating a leakage current that will circulate between the panel and the network. Without galvanic isolation or a common mode filter, the leakage current can be large enough to activate the inverter protection system, removing it from the grid, for example [43], [44]. These currents can cause electromagnetic interference, harmonics in the electrical network and losses in the circuit. In this converter, the L_O output inductor can be bypassed to form a common mode filter without changing the converter's operating modes. However, to simplify the operation analysis of the converter, the prototype was developed disregarding the common mode configuration of the inductor.

TABLE II
Comparison Among the Converters Presented in [9], [18], [40], and [41] and the Proposed Topology

Parameter	Topologies				
	Converter in [9]	Converter in [18]	Converter in [40]	Converter in [41]	Proposed converter
Diodes	4	2	4	2	3
Switch	1	3	2	2	1
Capacitor	4	1	5	3	3
Coupled Inductor	1	0	1	0	1
Inductor	1	2	0	3	1
Voltage Gain	$\frac{1+D+n}{1-D}$	$\frac{1+D1}{1-D1-D2}$	$\frac{1+2n}{1-D}$	$\frac{3D+1}{1-D}$	$\frac{1+D+n}{1-D}$
Voltage stress of main switch	$\frac{V_{OUT}}{1+D+n}$	$\frac{V_{OUT}+V_{IN}}{2}$	$\frac{V_{OUT}}{1+2n}$	$\frac{V_{OUT}}{1+3D}$	$\frac{V_{OUT}}{1+D+n}$
Output characteristic	current source	voltage source	voltage source	voltage source	current source
Total number of components	11	8	12	10	9

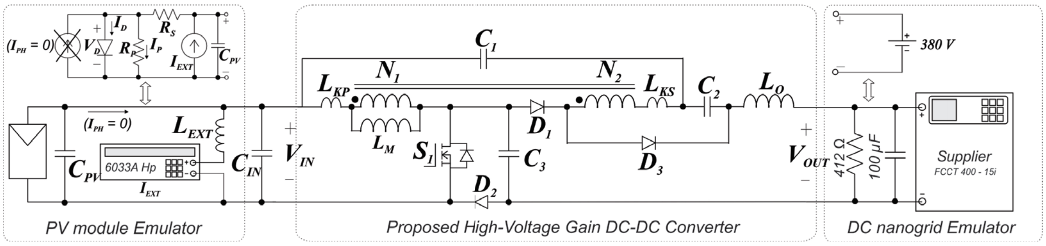


Fig. 5. Laboratory setup using the method proposed in [42], where an external current source is connected to the input to emulated the photogenerated currente. A voltage source is used at the output to emulate DC bus of the nanogrid.

III. EXPERIMENTAL VALIDANTION

In order to validate the theoretical assumptions and evaluate the performance of the proposed converter, a 200-W prototype was implemented in the laboratory, being connected to PV module KD210GX-LPU by Kyocera under the manufacturer's standard test conditions. Table I summarizes the components used in the prototype, while Figure 5 presents the experimental setup employed in the tests. The method proposed in [42] was adopted to evaluate the converter in the laboratory, where a PV module emulator is required.

The detailed setup is represented in Figure 5. A programmable source model 6033A by HP is configured to operate as a current source. A voltage source model FCCT400 – 15i by Supplier was adjusted to provide a DC voltage of 380 V aiming to emulate the DC nanogrid. This power supply not absorb power. Thus, a 412 Ω interface resistor is added to the output terminals to guarantee the power flux direction of converter to load. The converter was designed with an input voltage of 26 V while operating at 50 kHz. The output voltage and output current are shown Figure 6.a. The voltages across C_1, C_2, and C_3, and the voltage clamping as provided by C_3 can be seen in Figures 6.b and 6.c, respectively. Figure 6.d shows the voltage and current waveforms in the active switch, while the detailed view in Figure 6.e denotes low switching losses during turn on. As expected, the maximum voltage across S_1 is about 60 V. The currents through the primary inductance (I_{Lp}), secondary inductance (I_{Ls}), and magnetizing inductance (I_{Lm}) are represented in Figure 6.f. The commutation of diodes D_1, D_2, and D_3 is shown in Figures 6.g, 6.i, and 6.k, respectively. The detailed views presented in Figures 6.h, 6.j, and 6.l clearly evidence that such diodes are turned off under ZCS condition, thus contributing to the minimization of switching losses. The efficiency curve of the converter as a function of the output power for V_{IN} = 26 V is presented in Figure 7, being measured with power analyzer PA4000 by Tektronix. Since the converter designed for PV applications, EURO (European Efficiency) and the CEC (California Energy Commission) standards were adopted [8], [9], resulting in:

$$\eta_{EURO} = (0.03 \cdot 95.4) + (0.06 \cdot 96.08) + (0.13 \cdot 96.57) + (0.1 \cdot 96.65) + (0.48 \cdot 96.8) + (0.2 \cdot 95.4) = 96.38\% \qquad (19)$$

$$\eta_{CEC} = (0.04 \cdot 96.08) + (0.05 \cdot 96.57) + (0.12 \cdot 96.65) + (0.21 \cdot 96.8) + (0.53 \cdot 96.3) + (0.05 \cdot 95.4) = 96{,}4\%\,. \qquad (20)$$

Analogously to the proposed converter, the topology in [9] has output current source characteristic and presents a maximum efficiency of 94.7%. Considering standards EURO and CEC, the efficiencies become 96.38% and 96.4%, respectively. Figure 8 shows the distribution of losses among the power stage components, being D_2 the major responsible for the existing losses due high current conduction. A picture of the laboratory prototype is represented in Figure 9, where capacitor C_3 is assembled at the bottom layer of the printed circuit board (PCB).

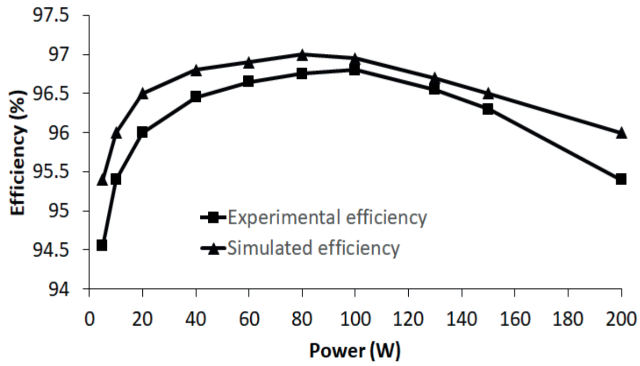


Fig. 7. Efficiency curve of proposed converter for V_{IN} = 26 V.

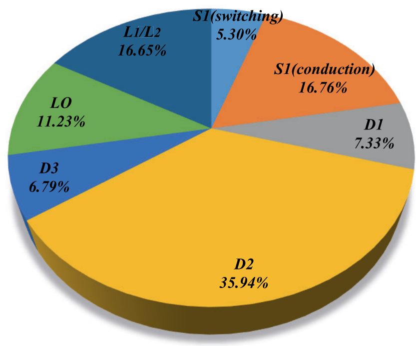


Fig. 8. Percent distribution of losses in the power stage components at the rated power condition.

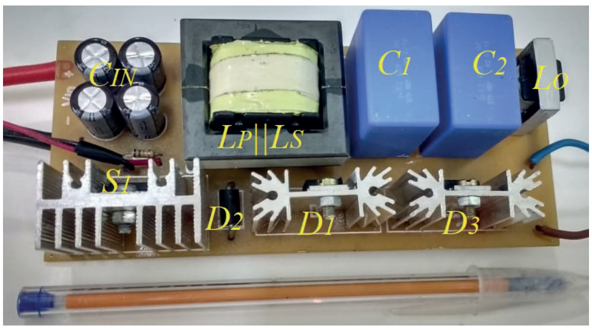
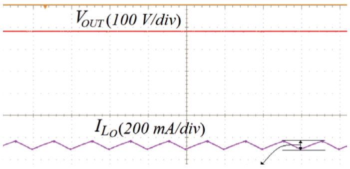
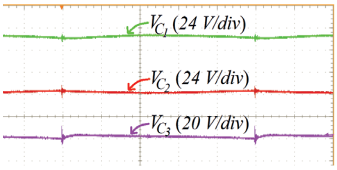
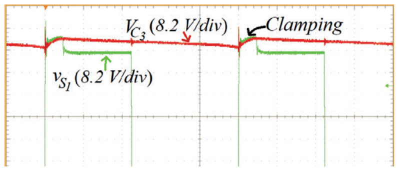


Fig. 9. Laboratory prototype.







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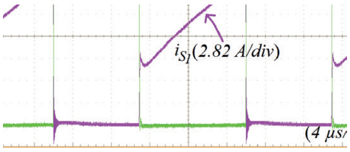

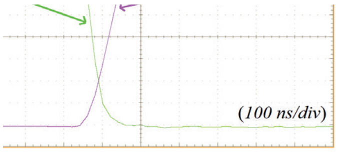

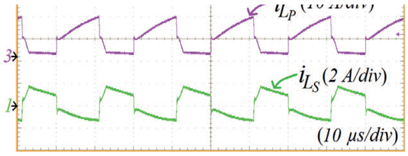

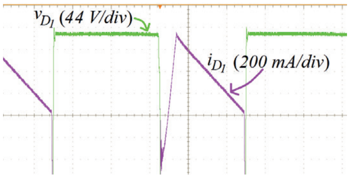

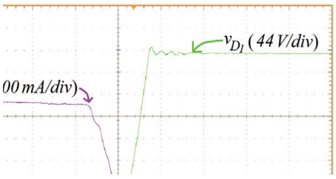

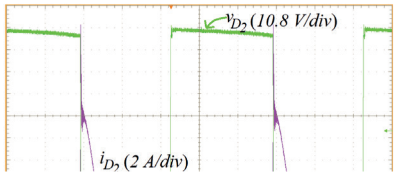

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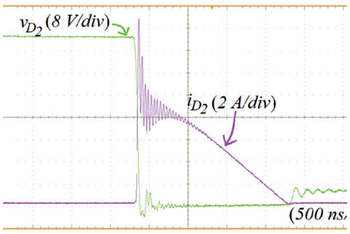

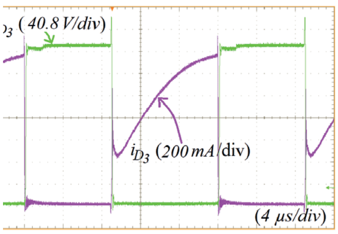

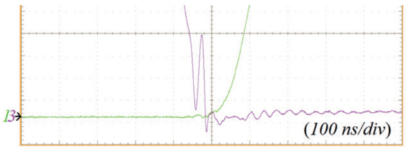

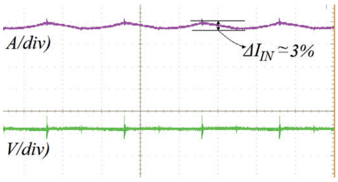

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