

# Asymmetrical ZVS-PWM Half-Bridge-Type Switched-Capacitor DC-DC Converter Isolated with peak voltage equal to $V_{in}/2$ switch

Angélica Paula Caús, Ivo Barbi Instituto Brasileiro de Eletrônica de Potência e Energias Renováveis - IBEPE - UFSC, Florianópolis - SC, Brasil  
e-mail: caus.angelica@gmail.com, ivobarbi@gmail.com

**Abstract** – This paper presents a new power converter topology generated by the integration of the asymmetrical ZVS-PWM dc-dc converter with a switched-capacitor ladder-type commutation cell. Circuit operation and theoretical analysis with emphasis on the soft-commutation process are included in the paper. The main advantage of the proposed converter with respect to the conventional asymmetrical half-bridge dc-dc converter is the reduction of the voltage stress across the power switches to the half of the input dc bus voltage, enabling the utilization of lower voltage rating components. Experiments conducted on a laboratory prototype with 1.4 kW power-rating, 800 V input voltage, 48 V output voltage and 100 kHz switching frequency are included to verify the theoretical analysis and the design methodology. The maximum efficiency of the experimental non-optimized prototype was 93.6%.

**Keywords** – Asymmetrical Dc-Dc Converter, Pulse-Width Modulation, Switched-Capacitor, Zero Voltage Switching, Isolated.

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## I. INTRODUCTION

In recent years, the increasing demand for power sources with high voltage and efficiency and low electromagnetic interference, together with light weight and reduced size, has led to the need for designers to develop new techniques or improve existing ones. Thus, dc-dc converters, which process high levels of power and energy, are currently one of the main subjects of focus in power electronics research. The asymmetrical half-bridge dc-dc converter, initially presented by P. Imbertson and N. Mohan [1] and studied in [2]–[11], presents high gain and high efficiency, soft switching in the power semiconductors, small number of components and is one of the most promising topologies in low-to-medium power applications. However, the voltage stresses on the switches are the same as the voltage in its power source, which hinders its implementation in applications that require high input voltages. For this reason, in applications where the input stage is as high as 750-1000 V, this converter is not always a suitable choice, since it would require the use of semiconductors with rated voltages of 1200 V.

Three-level isolated dc-dc converters [12]–[15] may solve this issue and are the most commonly used solutions for isolated dc-dc converter designs with these specifications.

However, they use a larger number of components in the power stage, in addition to the need, in many applications, to control the voltages across the input capacitors, as this equalization does not occur spontaneously. This control requires the use of voltage sensors and additional circuitry, contributing to the increase in equipment cost and complexity. In addition, these topologies are not suitable for asymmetric operation, as this type of operation does not allow the equalization of the voltages in the capacitors. Even for symmetrical topologies, the distribution of voltages across the capacitors is sensitive to the modulation employed or to the imperfections of the gate signals of the switches.

The series asymmetrical half-bridge converter with voltage autobalance is proposed to reduce the power semiconductors voltage stress to half of the input voltage [16]. Besides reducing the voltage across the switches, the proposed solution provides ZVS transition and natural voltage equalization across the input dividing voltage capacitors without control.

As a solution for the issue of high-voltage input, it is also possible to use commutation cells in a switched-capacitor, such as the ladder cell [17]. However, the switched capacitor converter does not allow control of the load voltage by adjustments of the duty cycle  $D$  and this is its main disadvantage in relation to conventional converters.

Isolated dc-dc converters combining switched capacitor circuits and conventional isolated dc-dc topologies were proposed, aiming to reduce power switches voltage ratings and allow operation with wide voltage conversion range. The integration of the switched capacitor ladder cell with LLC resonant converters has been proposed in recent papers [18], [19], with the purpose of reducing the voltage stress of the the power semiconductors preserving the other desirable characteristics of the LLC converter, which includes low switching losses and operation with high switching frequencies without sacrificing efficiency. The converter presented in [19] features ZVS on the input switches, zero current switching (ZCS) on the output diodes, a small variation in the static gain with load variation, and all the advantages of the ladder cell. However, in the two proposed topologies, the power transfer between the power source and the load is controlled by frequency modulation (FM).

With the aim of combining the features of the asymmetrical half-bridge converter and the ladder-type commutation cell, this paper presents the asymmetrical half-bridge switched capacitor converter, as an alternative solution to the issue of high-voltage input, which preserves all the attributes of the original asymmetrical half-bridge converter, such as the output current and soft commutation, with a natural reduction in voltage stress of the components of the power stage to half the voltage value of the power source. In the proposed

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converter, as will be shown below, the voltages across the input capacitors are naturally balanced, without the need of a control loop, as usually occurs in isolated dc-dc converters based on multi-level topologies. In addition, the control is performed by conventional PWM modulation, with constant frequency, which in many applications has advantages over the FM modulation of resonant converters.

## II. PROPOSED CONVERTER

The power stage of the proposed converter shown in Figure 1(a) is comprised of four power semiconductors  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$ , two fixed capacitors  $C_1$  and  $C_2$ , a floating capacitor  $C_5$ , a high frequency transformer  $T_1$ , an output rectifier stage made up of diodes  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$ , and an output filter comprised of  $L_O$  and  $C_O$ . The load is represented by the resistance  $R_O$ . The inductances  $L_m$  and  $L_c$  represent, respectively, the magnetizing inductance of the transformer and the commutation inductance, usually formed by the leakage inductance of the transformer in addition to an external inductance.

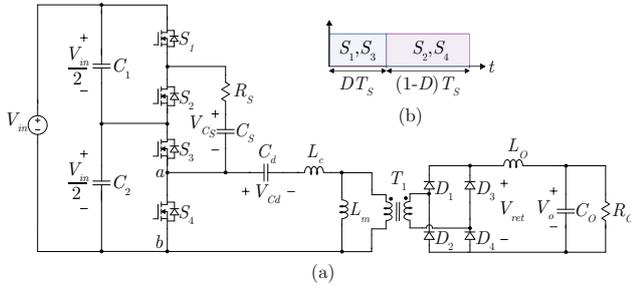


Fig. 1. (a) DC-DC hybrid half-bridge converter. (b) Gate signals.

The capacitor  $C_d$  is used to block the dc component of the voltage  $V_{ab}$ , generated due to the asymmetry of the converter, as occurs in the conventional asymmetrical half bridge converter. Figure 1(b) shows the gate signals of the ideal switches, without the dead time, which will be included later in Section 5, where the commutation analysis of the converter switches is made. The proposed converter operates with asymmetrical pulse-width modulation (PWM). The switches  $S_1$  and  $S_3$  are set to conduct during the time interval  $(0 - DT_S)$  and  $S_2$  and  $S_4$  are set to conduct during the complementary time interval  $(DT_S - T_S)$ .

The voltages across the capacitors  $C_1$ ,  $C_2$  and  $C_5$  and the switches  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$  are equal to half the voltage of the input source designated by  $V_{in}$ , this being the additional characteristic of this converter in relation to the conventional asymmetrical half-bridge converter.

## III. OPERATION PRINCIPLES OF THE PROPOSED CONVERTER

In order to simplify the description of the operation and the analysis of the proposed converter in the steady-state regime, the following simplifying hypotheses are adopted: 1) all power semiconductors, inductors and capacitors are considered ideal; 2) the voltages across the capacitors are considered constant during a period of operation; 3) the inductance of the output filter is considered sufficiently high

so that its current can be considered constant during a period of operation; 4) a single resistance, associated in series with the floating capacitor, represents all the conduction losses of the power semiconductors; 5) the dead time between switching signals is disregarded.

During a period of operation, the ideal converter has six operation stages which are described as follows. The topological stages are shown in Figure 2.

### A. First stage of operation ( $t_2-t_3$ )

The first stage of operation, which is shown in Figure 2(a), starts at the moment when the current in the inductance  $L_c$  reaches a value equal to the output current reflected to the primary side of the transformer ( $I'_o$ ), thus enabling the switches  $S_1$  and  $S_3$  to conduct. In this operation stage, the voltage source  $V_{in}$  supplies energy to the converter and the load.

### B. Second stage of operation ( $t_3-t_4$ )

The second stage of operation, which is shown in Figure 2(b), starts at the moment when  $S_1$  and  $S_3$  are gated off. The current in the commutation inductance ( $i_{Lc}$ ) does not reverse its direction instantly. Thus, the current is conducted through the intrinsic diodes of the switches  $S_2$  and  $S_4$ . All diodes of the output rectifier start to conduct and the voltage at its terminals becomes zero.

### C. Third stage of operation ( $t_4-t_5$ )

The third stage of operation, which is shown in Figure 2(c), starts at the moment when  $i_{Lc}$  reaches a null value, reversing its direction. Thus,  $i_{Lc}$  is conducted through the channels of  $S_2$  and  $S_4$ . All diodes of the output rectifier continue to conduct.

### D. Fourth stage of operation ( $t_5-t_6$ )

The fourth stage of operation, which is shown in Figure 2(d), starts at the moment when  $i_{Lc}$  reaches a value equal to  $-I'_o$ . In this time interval, the capacitor  $C_d$  supplies energy for the load.  $C_2$  and  $C_5$  are connected in parallel, allowing the discharge of  $C_5$ . This stage is concluded at the moment when the switches  $S_2$  and  $S_4$  are gated off and  $S_1$  and  $S_3$  are gated on.

### E. Fifth stage of operation ( $t_6-t_1$ )

The fifth stage of operation, which is shown in Figure 2(e), starts at the moment when the switches  $S_2$  and  $S_4$  are gated off. As occurs in the second stage of operation, the current in the commutation inductance is not reversed instantly. Thus, all diodes of the output rectifier start to conduct and the converter does not provide energy transfer for the load.

### F. Sixth stage of operation ( $t_1-t_2$ )

The sixth stage of operation, which is shown in Figure 2(f), starts at the moment when  $i_{Lc}$  reaches a null value, therefore reversing its direction and enabling the current, which up to this point is conducted by the intrinsic diodes of the switches  $S_1$  and  $S_3$ , to flow through the channel of the MOSFETs. However, the load voltage remains equal to zero since  $i_{Lc}$  is lower than the absolute value of  $-I'_o$ .

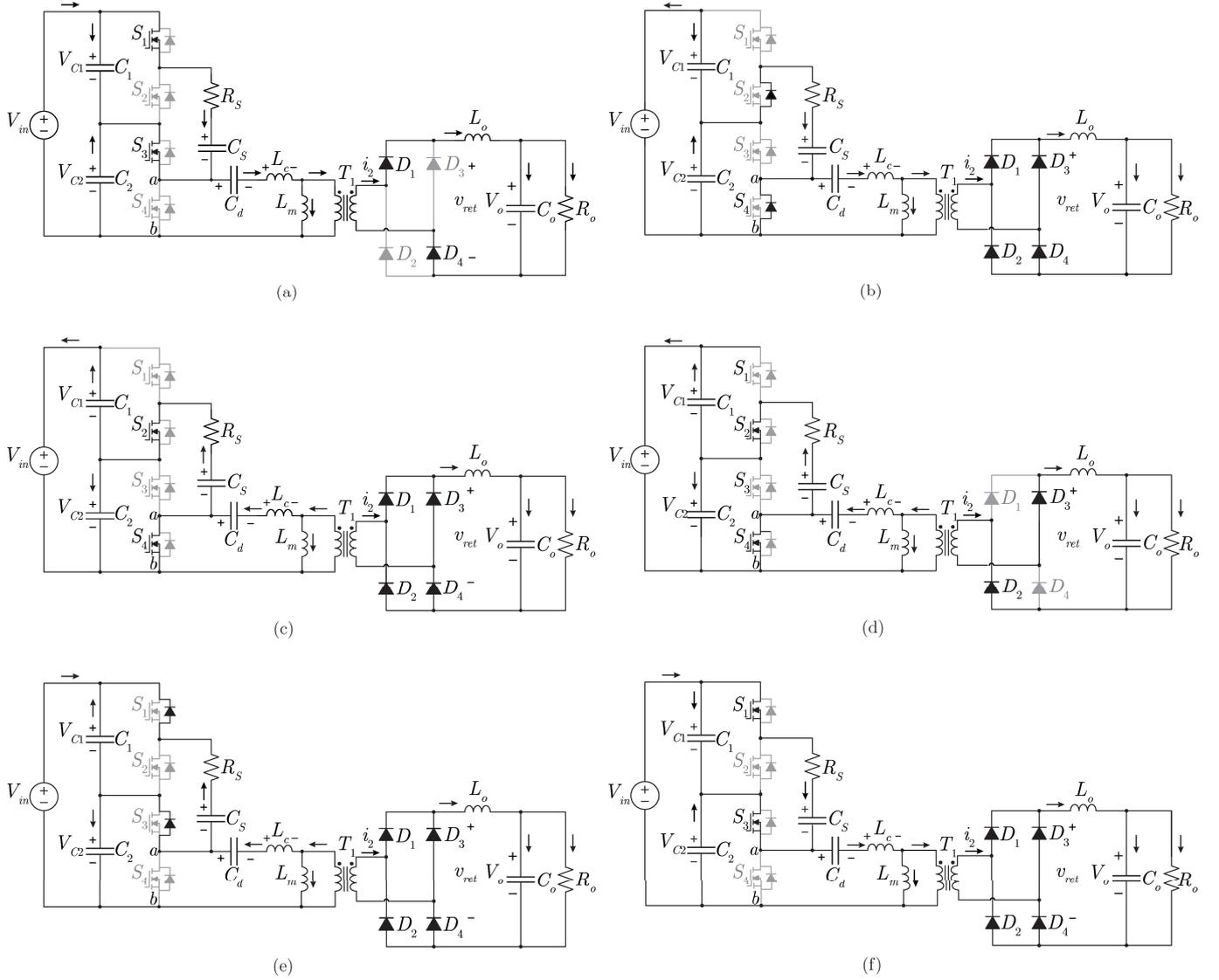


Fig. 2. Topological stages for the proposed converter: (a) First stage ( $t_2 - t_3$ ). (b) Second stage ( $t_3 - t_4$ ). (c) Third stage ( $t_4 - t_5$ ). (d) Fourth stage ( $t_5 - t_0$ ). (e) Fifth stage ( $t_0 - t_1$ ). (f) Sixth stage of operation ( $t_1 - t_2$ ).

#### IV. THEORETICAL ANALYSIS OF THE PROPOSED CONVERTER

The average value of the load voltage  $V_o$  can be determined by analyzing the waveform of the voltage at the terminals of the output rectifier  $v_{ret}$ . Its waveform is represented in Figure 3.

On analyzing the topological stages presented in Figure 2, the equations which define the voltages in the primary side of the transformer are determined. These are presented for the first and fourth stages of operation by expressions (1) and (2), respectively. For the other operating stages the voltage is null, as described in the previous section.

$$v_{ret}(t_1, t_2) = (1 - D) \cdot \frac{V_{in}}{2} \quad (1)$$

$$v_{ret}(t_3, t_4) = D \cdot \frac{V_{in}}{2} \quad (2)$$

In Figure 3 it can be noted that, for the time intervals

represented by  $t_a$  and  $t_b$ ,  $v_{ret}$  is null, which leads to a reduction in the static gain of the converter. Thus, in order to determine the static gain of the converter it is necessary to determine the time intervals and  $t_b$ .

On analyzing the waveforms of the voltage and the current on the commutation inductance ( $v_{Lc}$  and  $i_{Lc}$ ), in Figure 3, it can be observed that there is a voltage across  $L_c$  only during the time intervals represented by  $t_a$  and  $t_b$ . Thus, the duration of these time intervals can be defined through determining  $v_{Lc}$ .

Based on the analysis of the stages of operation, the values for  $v_{Lc}$  during the time intervals represented by  $t_a$  and  $t_b$  are defined by(3) and (4), respectively.

$$v_{Lc,t_a} = (1 - D) \cdot \frac{V_{in}}{2} \quad (3)$$

$$v_{Lc,t_b} = D \cdot \frac{V_{in}}{2} \quad (4)$$

As previously defined, at the moment that  $i_{Lc}$  reaches the output current value reflected to the primary side of the

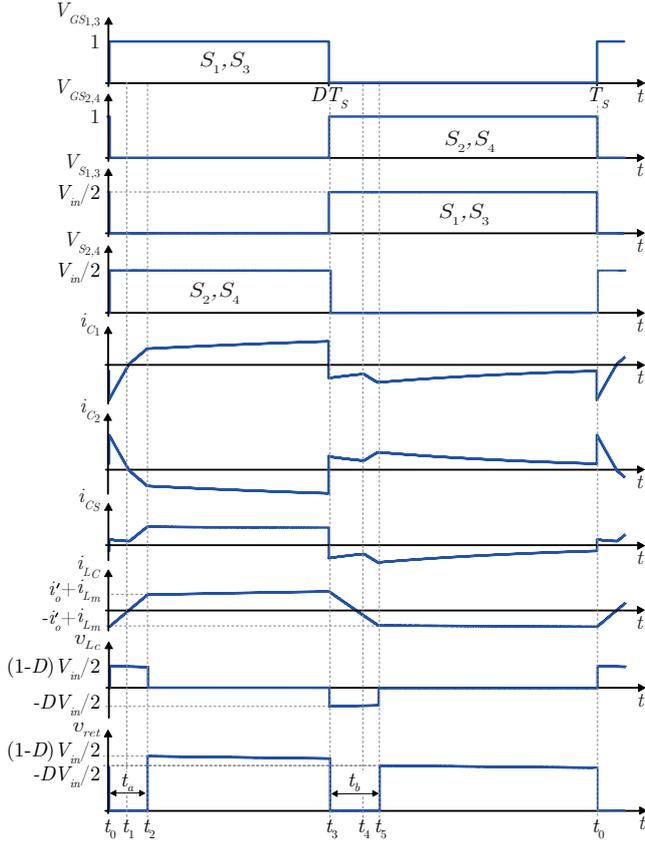


Fig. 3. Typical waveforms of the proposed converter.

transformer, the converter once again supplies energy to the load. Thus, the current in  $L_c$  at the moment when the third stage of operation is concluded is equal to  $-I'_o$ . Then:

$$t_a = \frac{4 \cdot L_c \cdot I'_o}{(1-D) \cdot V_{in}} \quad (5)$$

$$t_b = \frac{4 \cdot L_c \cdot I'_o}{D \cdot V_{in}}. \quad (6)$$

Having defined the values for  $t_a$  and  $t_b$ , the average value for the output voltage is obtained through the following equation

$$V_o = \frac{1}{T_s} \left[ \int_{t_a}^{D \cdot T_s} (1-D) \cdot \frac{V_{in}}{2n} + \int_{D \cdot T_s + t_b}^{T_s} D \cdot \frac{V_{in}}{2n} \right]. \quad (7)$$

Evaluating (8), the static gain is defined by

$$q = \frac{V_{in}}{V_o} = \frac{D \cdot (1-D)}{n} - \frac{4 \cdot f_s \cdot L_c \cdot I'_o}{n \cdot V_{in}} \quad (8)$$

where  $n$  is the transformer turns ratio.

Figure 5 shows the converter static gain for different values of  $D$  as function of the normalized load current reflected to the transformer primary side, given by

$$\bar{I}'_o = \frac{4 \cdot f_s \cdot L_c \cdot I'_o}{V_{in}}. \quad (9)$$

To determine the current stresses in the capacitors of the switched-capacitor stage, the non-idealities of the transformer are neglected. Thus, it is considered that the current through

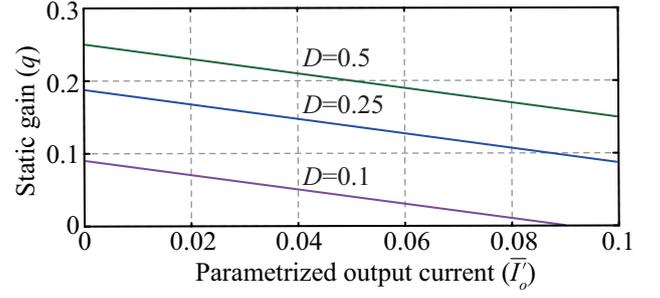


Fig. 4. Static gain of the proposed converter as a function of  $\bar{I}'_o$  for different values of the duty cycle  $D$ .

commutation inductance is instantly reversed and the proposed converter operates in only two stages.

To simplify the analysis of the switched capacitor stage formed by  $S_1 - S_4$ ,  $C_1$ ,  $C_2$ ,  $C_s$ ,  $R_s$ , and  $V_{in}$ , a current source with a current equal to  $\bar{I}'_o$  is connected at the terminals  $ab$ .

During the first stage of operation, shown in Figure 5, the instantaneous currents in the capacitors  $C_1$ ,  $C_2$  and  $C_s$  are given by (10), (11) and (12), respectively. The current in the capacitors are defined as shown in [20].

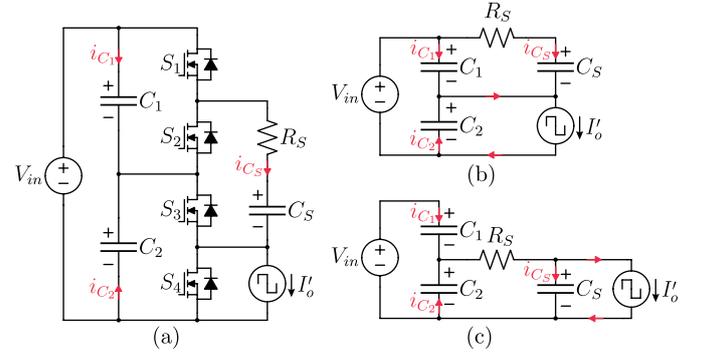


Fig. 5. (a) Simplified representation of the converter. (b) Equivalent circuit for the first stage of operation. (c) Equivalent circuit for the second stage of operation.

$$i_{C1} = \frac{D \cdot i_{Lc,p}}{12 \cdot f_s \cdot \tau} \cdot \frac{1}{\left(1 - e^{-\frac{D}{f_s \tau}}\right)} e^{-\frac{t}{\tau}} + \frac{i_{Lc,p}}{3} \quad (10)$$

$$i_{C2} = -\frac{D \cdot i_{Lc,p}}{12 \cdot f_s \cdot \tau} \cdot \frac{1}{\left(1 - e^{-\frac{D}{f_s \tau}}\right)} e^{-\frac{t}{\tau}} - \frac{i_{Lc,p}}{3} \quad (11)$$

$$i_{Cs} = \frac{D \cdot i_{Lc,p}}{6 \cdot f_s \cdot \tau} \cdot \frac{1}{\left(1 - e^{-\frac{D}{f_s \tau}}\right)} e^{-\frac{t}{\tau}} + \frac{i_{Lc,p}}{3} \quad (12)$$

During the second stage of operation, the above mentioned currents are given by (13), (14) and (15), respectively.

$$i_{C1} = -\frac{D \cdot i_{Lc,n}}{4 \cdot f_s \cdot \tau} \cdot \frac{1}{\left(1 - e^{-\frac{(1-D)}{f_s \tau}}\right)} e^{-\frac{t}{\tau}} \quad (13)$$

$$i_{C2} = \frac{D \cdot I'_o}{4 \cdot f_s \cdot \tau} \cdot \frac{1}{\left(1 - e^{-\frac{(1-D)}{f_s \tau}}\right)} e^{-\frac{t}{\tau}} \quad (14)$$

## V. COMMUTATION ANALYSIS

$$i_{C_S} = -\frac{D \cdot I'_o}{2 \cdot f_s \cdot \tau} \cdot \frac{1}{\left(1 - e^{-\frac{(1-D)}{f_s \cdot \tau}}\right)} e^{-\frac{t}{\tau}} \quad (15)$$

Assuming  $C_1 = C_2 = C_S = C$ . Thus, the time constant  $\tau$  is given by

$$\tau = \frac{4 \cdot C_S \cdot R_{dson}}{3}. \quad (16)$$

The resistance  $R_S$  is equal to twice the  $R_{dson}$  resistance of one of the switches, defined in the manufacturer's data sheet, for the junction temperature provided in the dimensioning of the converter's power stage.

Using (10)-(15) the effective values of the normalized currents in  $C_1$ ,  $C_2$  and  $C_S$  are found and represented Figure 6 as a function of the product  $f_s \tau$ , for  $D = 0.45$ .

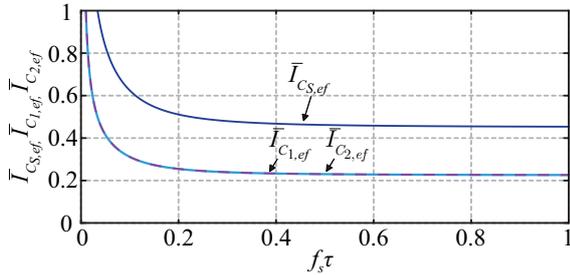


Fig. 6. Graphic representation of effective values of the currents in  $C_1$ ,  $C_2$  and  $C_S$ , normalized in relation to  $I'_o$  as a function of  $f_s \tau$ , for  $D = 0.45$ .

On analyzing the curves shown in Figure 6, it can be noted that the effective value of the current in  $C_S$  is higher than those in  $C_1$  and  $C_2$ , regardless of the value of  $f_s \tau$ . It can also be observed that for values of  $f_s \tau$  higher than 0.2, the effective values for the currents in the capacitors practically remain constant and close to their minimum values. However, for values of below 0.2, the effective values of the currents increase exponentially, contributing to the elevation of the conduction loss.

Inspection of the curves shown in Figure 6, reveals that the currents become independent of the frequency when  $f_s \tau \geq 0.2$ . Adopting  $f_s \tau = 0.4$ ,  $C_S$  is defined as presented in (17).

$$C_S > \frac{3}{10 \cdot R_{dson} \cdot f_s} \quad (17)$$

It is important that the capacitance value of the capacitor  $C_S$  meets the voltage ripple specification of the project. Thus,

$$C_S \geq \frac{2D \cdot \left( \frac{D \cdot i_{Lc,p}}{6 \cdot f_s \cdot \tau} \cdot \frac{1}{\left(1 - e^{-\frac{D}{f_s \cdot \tau}}\right)} e^{-\frac{t}{\tau}} + \frac{i_{Lc,p}}{3} \right)}{V_{in} \cdot f_s \cdot \Delta V_c} \quad (18)$$

Knowing the values of the currents in the capacitors for each stage of operation, the average and effective values of the currents in the switches can be obtained by means of the integral of the current waveform area in the switches shown in Figure 3.

The commutation of the power semiconductors in the Asymmetrical ZVS-PWM Half-Bridge-Type Switched-Capacitor DC-DC Converter is similar to that of the conventional half-bridge converter. The current that provides energy for charging and discharging the commutation capacitors and ensuring soft switching is formed by the sum of the current in the commutation inductance  $i_{Lc}$  with the current in the magnetizing inductance of the transformer  $i_{Lm}$ . If the magnetization inductance is low, the magnetization current has large ripple and peak value, significantly influencing the commutation process. Therefore, it should be included in the switching analysis. Since the amplitude of current in  $L_m$  is not sufficient to provide the complete charging and discharging of the commutation capacitors and ensure soft is, an external inductor switching included and associated in series with the leakage inductance to store the sufficient amount of energy to accomplish the soft switching.

Due to the asymmetry of the converter, the currents in inductor  $L_c$  at the instant  $S_2$  and  $S_4$  are turned off are different from the instant  $S_1$  and  $S_3$  are turned off. These currents are given by (19) and (20), respectively.

$$i_{Lc(2,4)} = I'_o + I'_o \cdot (1 - 2D) \cdot \left[ 1 - \frac{4 \cdot f_s \cdot L_c \cdot I'_o}{D \cdot (1 - D) \cdot V_{in}} \right] - \frac{D \cdot (1 - D) \cdot n \cdot V_{in}}{4 \cdot L_m \cdot f_s} \quad (19)$$

$$i_{Lc(1,3)} = I'_o + I'_o \cdot (1 - 2D) \cdot \left[ 1 - \frac{4 \cdot f_s \cdot L_c \cdot I'_o}{D \cdot (1 - D) \cdot V_{in}} \right] + \frac{D \cdot (1 - D) \cdot n \cdot V_{in}}{4 \cdot L_m \cdot f_s} \quad (20)$$

The ZVS range depends on the energy stored in the inductor  $L_c$  at the instant of the commutation, to charge and discharge the commutation capacitors associated in parallel with the switches. Thus, the ZVS is not achieved if the necessary energy is not stored in  $L_c$  before the beginning of the commutation. Consequently, the limit load range with ZVS is imposed by the smallest current in  $L_c$ , that occurs at the instant the switches  $S_2$  and  $S_4$  are turned off.

Due to similarity in the analysis of the two commutations, in this study only the analysis for the commutation of switches  $S_2$  and  $S_4$  is described, since it is the more critical of the two. Before the start of the commutation, the current  $i_{Lc}$  circulates through switches  $S_2$  and  $S_4$  and the corresponding topological stage is given in Figure 7, where  $V_{C_{S2}} = V_{C_{S4}} = 0$  and  $V_{C_{S1}} = V_{C_{S3}} = V_{in}/2$ .

### A. Linear stage ( $t_0 - t_{0a}$ )

At time  $t = t_0$  the semiconductors  $S_2$  and  $S_4$  are gated off and the linear stage of commutation begins. The capacitors  $C_{S2}$  and  $C_{S4}$  charge while  $C_{S1}$  and  $C_{S3}$  discharge with constant current and the respective voltages evolve linearly. This stage ends at time  $t = t_{0a}$  when the voltage  $V_{C_{S4}}$  becomes equal to  $V_{Cd}$ , that is the voltage across the capacitor  $C_d$ . This commutation stage is represented in Figure 7(b).

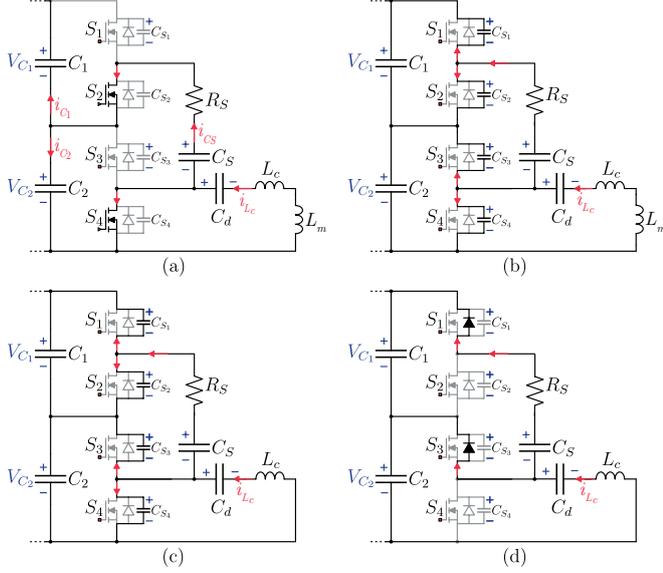


Fig. 7. Topological stages during commutation. (a) Before  $S_2$  and  $S_4$  turn off ( $t_0 - t_6$ ). (b) Linear stage ( $t_0 - t_{0a}$ ). (c) Resonant stage ( $t_{0a} - t_{0b}$ ). (d) End of commutation ( $t_{0b} - t_{0c}$ ).

### B. Resonant stage ( $t_{0a} - t_{0b}$ )

At time  $t = t_{0a}$  the resonant stage of commutation starts, represented by the topological stage shown in Figure 7(c). During this time interval the voltage across the inductance  $L_m$  is null and there is some resonance between the inductance  $L_c$  and the commutation capacitance. This stage of commutation ends when  $V_{CS2} = V_{CS4} = V_{in}/2$  and  $V_{CS1} = V_{CS3} = 0$ .

After time  $t = t_{0b}$  the diodes arranged in antiparallel with  $S_1$  and  $S_3$  start to conduct the current  $i_{Lc}$ . The corresponding topological stage is shown in Figure 7(d).

In the time  $t = t_{0c}$  the semiconductors are enabled to conduct before the current  $i_{Lc}$  is reversed, so that ZVS is achieved. The dead time  $t_{d2}$  must be longer than the commutation time  $t_{c2}$ . In Figure 8 the main waveforms for turn off of  $S_2$  and  $S_4$  are shown.

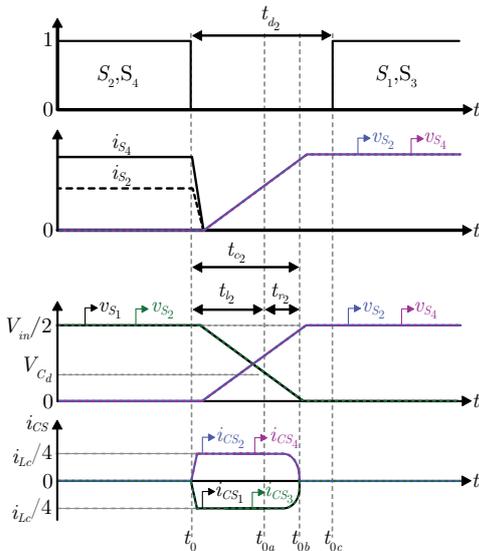


Fig. 8. Typical waveforms for the commutation initiated at time  $t = t_6$ .

### C. Duration of commutation

As follows from Figure 8, the current  $i_{Lc}$  is divided equally between the commutation capacitors, during the dead time interval. Therefore, the time duration of the linear charging and discharging of the capacitors is given by

$$t_{l2} = 2 \cdot C_c \cdot \frac{(1-D) \cdot V_{in}}{I_{Lc}}. \quad (21)$$

The duration of the resonant time interval is determined through the analysis of the state plane shown in Figure 9. To define it, it is necessary to know the equations that describe the voltage and current in the switching capacitors, which are obtained through the analysis of the equivalent circuits shown in Figure 8.

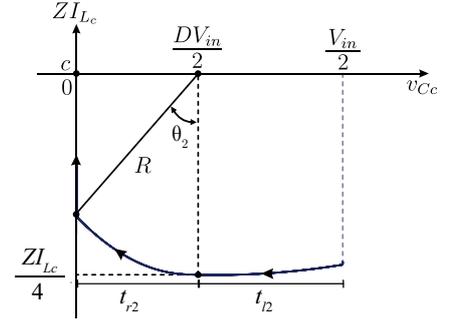


Fig. 9. State plane trajectory for the resonant stage of soft commutation.

The duration of the resonant transition is defined by multiplying the angle  $\theta_2$  by the inverse of the angular resonance frequency  $\omega$ . Thus:

$$t_{r2} = \frac{1}{\omega} \cdot \left[ \frac{\pi}{2} - \cos^{-1} \left( \frac{D \cdot V_{in}}{2 \sqrt{\left(\frac{D \cdot V_{in}}{2}\right)^2 + \left(Z \cdot \frac{I_{Lc}}{4}\right)^2}} \right) \right], \quad (22)$$

where,

$$Z = \sqrt{\frac{L_c}{4C_c}} \quad (23)$$

and

$$\omega = \frac{1}{\sqrt{\frac{L_c \cdot C_c}{2}}}. \quad (24)$$

The duration of the commutation is the sum of the time intervals  $t_{l2}$  and  $t_{r2}$  and is given by

$$t_{c2} = t_{l2} + t_{r2}. \quad (25)$$

As previously mentioned, the dead time  $t_{d2}$  must be longer than the time  $t_{c2}$ . Thus,

$$t_{d2} > t_{c2}. \quad (26)$$

## VI. EXPERIMENTAL RESULTS

In order to validate the theoretical analysis of the proposed topology, an experimental prototype was designed and built, as shown in Figure 10, and its specifications are given in Table I.

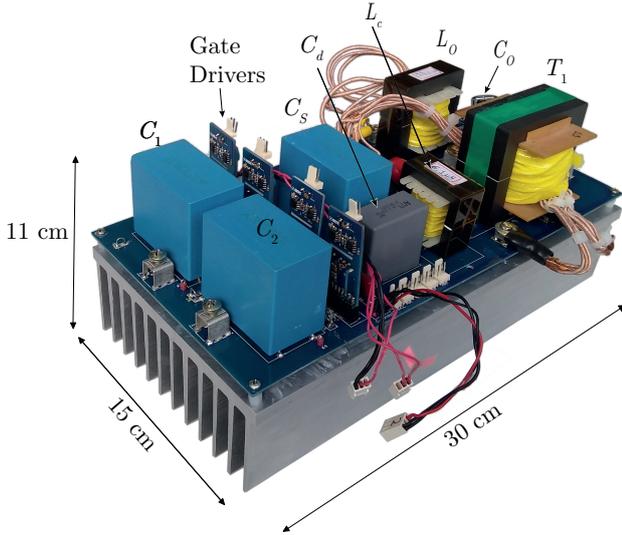


Fig. 10. Experimental prototype of the ZVS-PWM-SC asymmetrical half-bridge dc-dc converter.

**TABLE I**  
Converter specifications.

Specifications	Symbol	Value
Output power	$P_o$	1.4 kW
Input voltage	$V_{in}$	800 V
Output voltage	$V_o$	48 V
Switching frequency	$f_S$	100 kHz

The gate signals of the switches, with a dead time of 300 ns between them, generated by a DPS TMS320F28069, are shown in Figure 11.

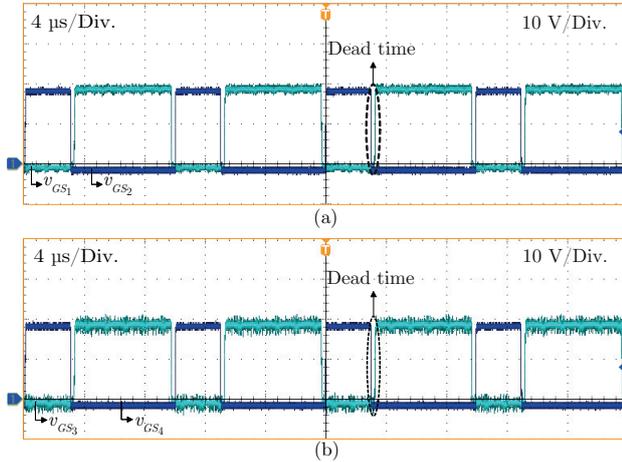


Fig. 11. (a) Gate signals of  $S_1$  and  $S_2$ . (b) Gate signals of  $S_3$  and  $S_4$ .

In the experimental prototype a voltage clamping circuit was included, comprised of a fast diode ( $D_g$ ), a resistor ( $R_g$ ) and a capacitor ( $C_g$ ), as shown in Figure 12. This clamping circuit is employed to limit the peaks in the voltages across the diodes  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$  of the output rectifier, caused by the reverse recovery currents during the commutations.

The voltage clamping circuit allows part of the energy stored in the commutation inductor  $L_c$  to be transferred to the output filter capacitor  $C_o$ , which contributes to increasing the efficiency of the converter.

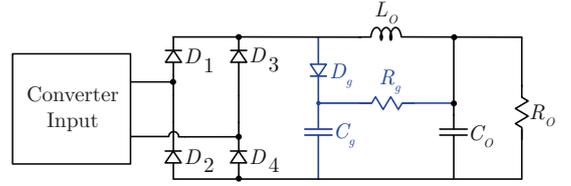


Fig. 12. Voltage clamping circuit to limit the voltage across diodes  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$ , included in the experimental prototype.

The components employed in the clamping circuit, along with the other components used in the prototype, are given in Table II. The semiconductor used was a (SiC) MOSFET, with a rated drain-source voltage of 650 V.

**TABLE II**  
Parameters of experimental prototype.

Component	Value
Input capacitor ( $C_1 - C_2$ )	25 $\mu$ F
Floating capacitor ( $C_s$ )	25 $\mu$ F
DC blocking capacitor ( $C_d$ )	4.7 $\mu$ F
Output capacitor ( $C_o$ )	1000 $\mu$ F
Clamp capacitor ( $C_g$ )	4.5 $\mu$ F
Total commutation inductance ( $L_c$ )	9.62 $\mu$ H
Output inductor ( $L_o$ )	25.2 $\mu$ H
Clamp resistor ( $R_g$ )	2.2 k $\Omega$
Diode clamp ( $D_g$ )	MUR4100
Secondary side diodes ( $D_1 - D_4$ )	MBR40250TG
Main switches ( $S_1 - S_4$ )	SCT3120AL / 650 V
$R_{dson}$ for $T_j [100^\circ\text{C}]$ e $V_{GS} = 18$ V	150 m $\Omega$
$f_S \tau$	0.4
Transformer turns ratio ( $n$ )	2.25
Magnetizing inductance ( $L_m$ )	183 $\mu$ H
Leakage inductance ( $L_k$ )	1.62 $\mu$ H
Dead time ( $t_d$ )	30 ns

Figure 13 shows the experimental waveforms of the currents in the primary and secondary windings of the high frequency transformer of the converter, operating with a power of 1.4 kW and rated input and output voltages.

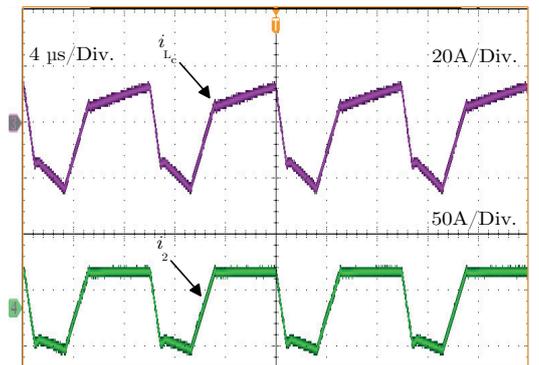


Fig. 13. Current waveforms in the transformer primary and secondary windings.

Figure 14 shows the experimental waveforms of voltages across the switches  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$ . It can be observed that the voltages across them are equal to 400 V, that is, half the value of the input voltage, which is 800 V. The main attribute of this converter in relation to the conventional asymmetrical half-bridge converter, which is the reduction in the voltage stresses on the components of the power stage, is then verified

experimentally. It is also verified that the equalization of the voltages across the capacitors occurs naturally, without any action of control. However, there is a difference of about 3.7% between the voltage across the switches  $S_1$  and  $S_2$  and about 1% between the voltage across the switches  $S_3$  and  $S_4$ , which are attributed to the non-idealities of the power semiconductors.

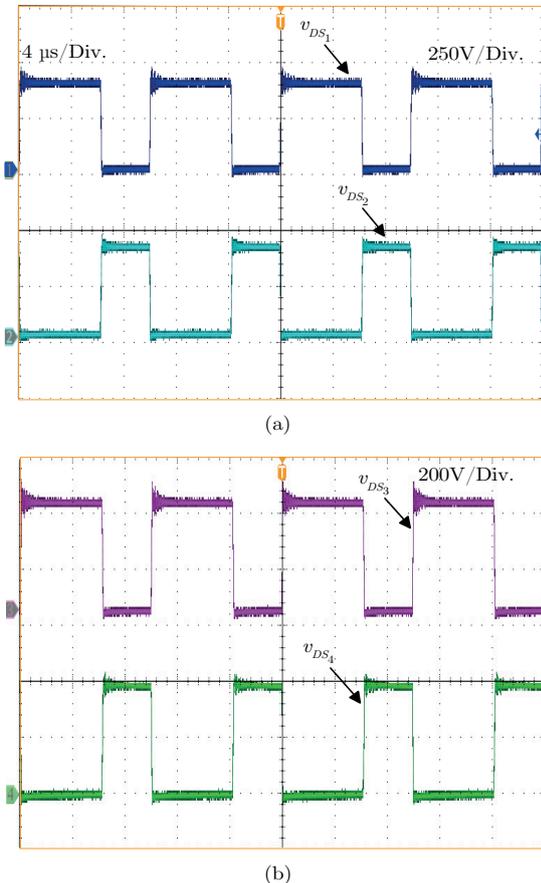


Fig. 14. (a) Voltages across semiconductors  $S_1$  and  $S_2$ . (b) Voltages across semiconductors  $S_3$  and  $S_4$ .

The switching capacitance and inductance are designed for the converter to operate with ZVS for the power range between 25% and 100% of the rated output power. The inductance value is defined according to two criteria: 1) the maximum loss of the duty cycle, defined by the second term of (8), where  $I'_o$  it is replaced by the value of the output current considering that the converter operates with 25% of its load nominal; 2) energy flow between the capacitor and the inductor: the energy stored in the inductor must be sufficient to discharge the switching capacitors during the dead time.

Figure 15 shows the gate signals and the voltages across the switches  $S_1$  and  $S_2$  during turning off for the converter operating at 80% of the rated power. It can be observed that both switches turn off with ZVS. The gate signals and the voltages across the switches  $S_3$  and  $S_4$  presented in Figure 16 show that both switches also turn off with ZVS.

These waveforms show that in the proposed converter, as in the conventional asymmetrical half-bridge converter, the switches operate with soft switching. The minimum value for the processed power with soft switching is dependent on the

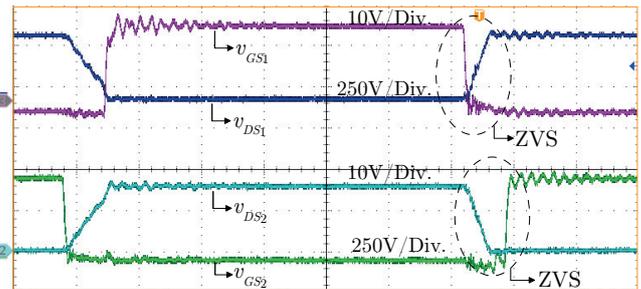


Fig. 15. Gate signals and voltage stress of semiconductors  $S_1$  and  $S_2$ .

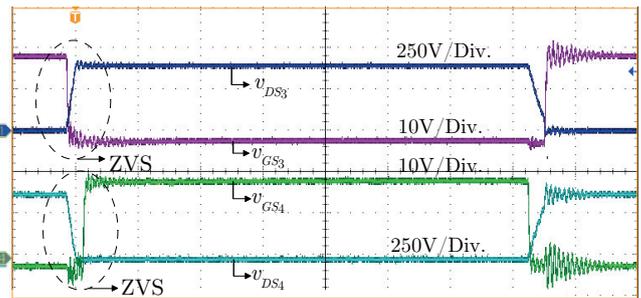


Fig. 16. Gate signals and voltage stress of semiconductors  $S_3$  and  $S_4$ .

parameters of the converter design, as is the case for all other PWM converters with soft commutation.

Figure 17 present the waveforms of the voltage on the bus capacitors, a small difference between the voltage values on the capacitors is observed, this occurs due to the internal resistance of the capacitors and the trails resistense present on the PCB. However, this 8 V variation (2%) is not large enough to interfere with the voltage equalization between the capacitors.

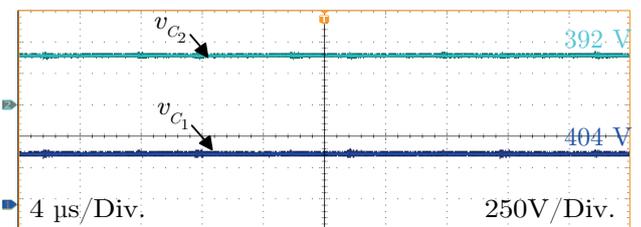


Fig. 17. Efficiency of the experimental prototype of the proposed converter.

The efficiency of the experimental prototype, for different power values, was measured with the aid of a Tektronix power analyzer (PA3000), and the resulting curve is shown in Figure 18. The maximum efficiency obtained is equal to 93.6% for a power load of 1 kW. The aim of building the prototype was to demonstrate its functioning and validate the theoretical analysis and it was not optimized to reduce losses.

The theoretical distribution of the losses, defined through the equation of losses of each component that delivers the prototype is shown in Figure 19, where it is noted that half of these losses occur in the diodes of the output rectifier stage. Therefore, the replacement of the full bridge rectifier with four diodes, by a midpoint rectifier with two diodes, should contribute to reduce losses and increase efficiency. It is also observed that these losses can be reduced with the use of a

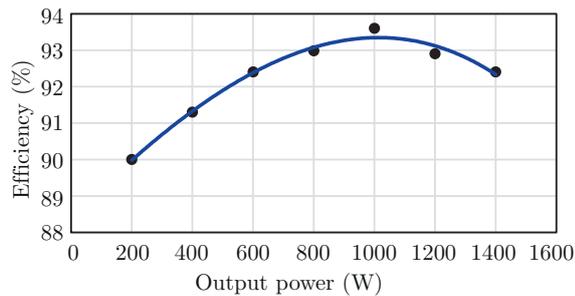


Fig. 18. Efficiency of the experimental prototype of the proposed converter.

better material in the design and construction of the magnetic devices.

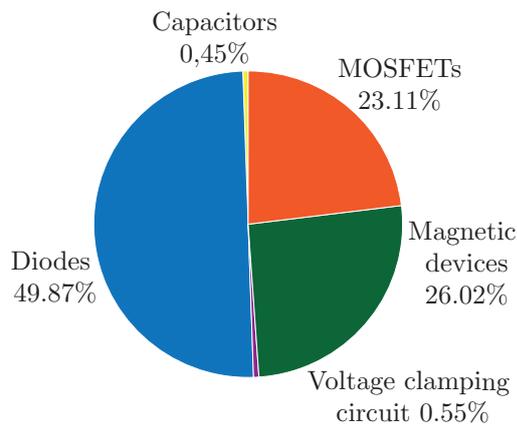


Fig. 19. Theoretical distribution of losses in the converter power stage.

## VII. CONCLUSIONS

A new isolated dc-dc converter topology, generated by the integration of the asymmetrical half-bridge dc-dc converter and the switched-capacitor ladder cell, for high input voltage operation with soft switching has been proposed. The advantage of the proposed converter with respect to the conventional asymmetrical half-bridge dc-dc converter is the reduction of the voltage stress across the power switches to the half of the input dc bus voltage, enabling the utilization of lower voltage rating power semiconductors. Moreover, in contrast to the isolated three-level dc-dc converters, there is a natural balance of the voltages across the input voltage dividing capacitors, without the need for control. An experimental prototype has been designed, constructed and tested in the laboratory to verify the converter operation principle and the theoretical analysis results. The authors believe that the proposed converter, like the series asymmetrical half-bridge converter with voltage autobalance for high input-voltage introduced in [16], can be a competitive candidate for low-to-medium power and high input voltage applications.

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## BIOGRAPHIES

**Ivo Barbi** (Life Fellow, IEEE) was born in Gaspar, Brazil. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree in electrical engineering from the Institut National Polytechnique de Toulouse (INPT), Toulouse, France, in 1979. He founded the Brazilian Power Electronics Society (SOBRAEP), the Brazilian Power Electronics Conference (COBEP), in 1990, and the Brazilian Power Electronics and Renewable Energy Institute (IBEPE), in 2016. He is currently a Researcher with the Solar Energy Research Center and a Professor Emeritus in electrical engineering with UFSC. Prof. Barbi received the 2020 IEEE William E. Newell Power Electronics Award. He serves as an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON POWER ELECTRONICS for several years.

**Angélica Paula Caús** was born in Rondinha, Brazil. She received the B.S. degree in electrical engineering from the University of Passo Fundo (UPF), Passo Fundo, Brazil, in 2018, and the M.S. degree in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 2020. She is currently a PhD student in Electrical Engineering at UFSC, in the Power Electronics and Electrical Drives area.