# A HIGH STEP-UP ISOLATED DC-DC CONVERTER BASED ON CASCADED GREINACHER VOLTAGE MULTIPLIER

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***Abstract* – High step-up converters are required and used in photovoltaic applications, due to low voltage of photovoltaic modules. In this paper, an isolated dc-dc high step-up SEPIC with a Greinacher voltage quadrupler cell is proposed. It has the advantage of continuous input current, high efficiency, high voltage gain, isolation and demands a single switch, being suitable for low power grid-tie photovoltaic systems. The derivation of converter, the operating principles and steady-state analysis are presented, including the detailed analysis of resonant stage, where the value of primary side capacitor is taken into account. Besides that, effects of transformer winding capacitances on converter operation are investigated. Experimental results on a 37.4/400 V, 50 kHz and 200 W prototype are presented to validate the proposed topology and concept, where the maximum efficiency obtained is 97.75%.**

***Keywords* – Isolated SEPIC, Magnetizing Current, Voltage Step-up Cells.**

## I. INTRODUCTION

The increase of photovoltaic systems, specifically low power grid-tie systems with two converters, makes high-step up dc-dc converter very important. These systems, as shown in Figure 1, are also known as ac photovoltaic modules (module-integrated-converter – MIC), where a high step-up converter, in first stage, provides a high voltage gain and is connected to a grid-tie inverter. The output voltage of the photovoltaic module is low, typically 20-40 V [1], and this low voltage level has to be boosted to a high dc-bus voltage in order to allow grid connection [2]. Therefore, a high number of isolated and non-isolated topologies have been proposed for this application.

Several classic step-up converters can be used, such as dc-dc boost converter, due to simple structure and input current feature [3], however, many of them present reduced voltage step-up ratio [4]. To solve this problem, those converters employ cascade, voltage multipliers, and/or coupled inductors techniques in order to elevate static gain [5]. In this work, since the focus is on first stage (dc-dc converter) of an ac photovoltaic module, galvanic isolation is desirable in order to maintain security of the whole system, besides mitigating leakage current and electromagnetic interference (EMI) [6].

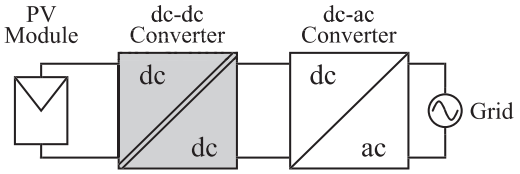


Fig. 1. MIC converter with emphasis on first stage.

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Isolated converters using those aforementioned techniques are found in [7]-[9], through the integration of cascaded boost with a buck-boost converter, or adding a voltage multiplier on secondary side. It is important to highlight that single switch converters are more suitable for low power applications, reducing volume, costs and complexity. A several number of isolated single switch converters are found in literature, however, many of them have the problem of high leakage inductance, requiring the use of a snubber circuit associated to a voltage step-up technique in order to increase the static gain [9]-[12].

Leakage inductance on isolated converters causes several spikes over semiconductors and may harm them, besides reduce converter's efficiency. These high values of leakage inductance occur on isolated converters with coupled inductor for isolation, like flyback, where leakage flux is necessary to store energy, resulting in a dc component on magnetizing current [13]. This problem is considerable reduced with the use of a well-designed transformer, where theoretically there is no dc component on magnetizing current. Another isolated converters are ZETA, SEPIC and Ćuk, on isolated versions. Isolated ZETA (iZETA) always uses a coupled inductor for isolation and has discontinuous input current, while isolated Ćuk (iĆuk) is the only option that intrinsically uses a transformer instead of coupled inductor, and also has continuous input current, however, it also has the higher component count in standard version and with the addition of voltage step-up techniques [14]. Isolated SEPIC (iSEPIC) has lower component count in comparison with iĆuk and, although the use of coupled inductor on standard version, it has the possibility of use transformer instead of coupled inductor. The three aforementioned converters (iĆuk, iSEPIC and iZETA) are shown in Figure 2.

To achieve this, the appropriate choice of cells and techniques has to be performed. In this way, voltage multiplier cells (VMCs) applied on secondary side provide the advantages of increased converter static gain and clamped voltage spikes on diodes without elevating voltage stress over the switch, unlike techniques applied on primary side.

These VMCs used on secondary side are based on switched capacitor techniques and the most commonly used are known as voltage doubler (VD) and voltage tripler (VT), with the possibility of expansion to raise voltage gain. It is important to highlight that voltage step-up techniques used

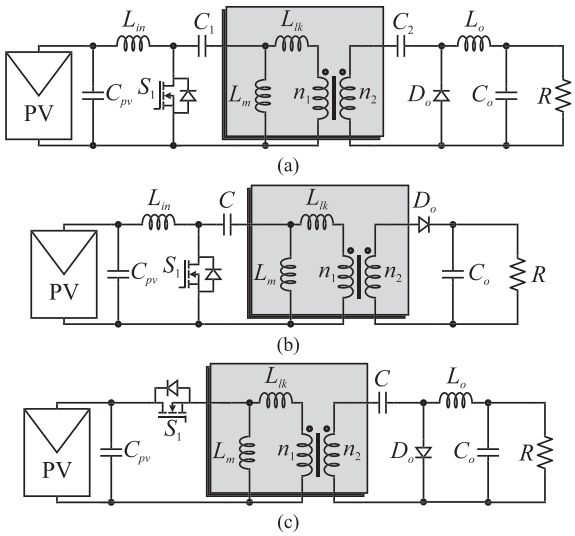


Fig. 2. Three dc-dc converters on isolated versions: (a) iĆuk; (b) iSEPIC and (c) iZETA. .

on primary side do not present the possibility of changing the coupled inductor to transformer. To better understand this, the derivation of proposed converter is presented in Section II.

Therefore, this paper proposes an isolated single switch dc-dc converter achieving high voltage gain and high efficiency using a transformer for galvanic isolation without using a snubber circuit, which significantly reduces volume and cost of the whole system. Moreover, a cascaded version of VD cell is chosen to be used on secondary side, since it increases static gain of the proposed converter, reducing turn ratio of transformer, which reduces leakage inductance and does not decrease converter efficiency.

The converter has the following features: 1) qZCS turn-on of switch disregarding the use of snubber circuit; 2) Possibility of ZCS turn-off for all diodes, mitigating losses associated with diode reverse recovery; 3) Clamp of voltage spikes over the diodes; 4) Small input current ripple due to input inductor; 5) Reduced voltage spikes over the switch, without use of snubber circuit, due to low leakage inductance of transformer; 6) High efficiency with low cost, achieving high voltage gain. 7) Low turn ratio of transformer due to the elevated static gain. Experimental results on a 50 kHz, 200 W prototype are presented to validate these features.

In Section II, the derivation of the proposed converter is presented, justifying its choice. In Section III, theoretical analysis of proposed converter is performed, with special attention to resonant stage and effect of winding transformer capacitance on converter operation. Experimental results are shown in Section IV, validating the proposed concept and verifying the effects shown on previous sections. Section V concludes the paper.

## II. DERIVATION OF CONVERTER

The isolated SEPIC converter, shown in Figure 3.b is obtained from the classic topology, shown in Figure 3.a. Cantilever model can be used to represent the magnetic element (transformer or coupled inductor) [15]. Figure 3.c shows the converter with VMC on secondary side. Greinacher VD cell, Dickson and Ladder VT cells, shown in Figure 4, are interesting options that can be used on secondary side [16]-[18]. As mentioned before, an appropriate choice of VMC can significantly reduce the dc magnetizing current, guaranteeing that the magnetizing inductance, $L_m$, does not store energy. Thus, a transformer is used for galvanic isolation instead of a coupled inductor, consequently providing a better utilization of BxH curve, reducing its volume and its leakage inductance, $L_{lk}$ [19]. To better understand this, Kirchhoff current law (KCL) is applied on indicated node in Figure 5, where classical isolated SEPIC is presented with and without voltage cells on secondary side. Since dc current is theoretically null in a

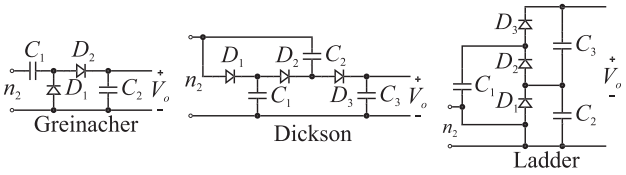


Fig. 4. Cells applied on secondary to increase voltage gain.

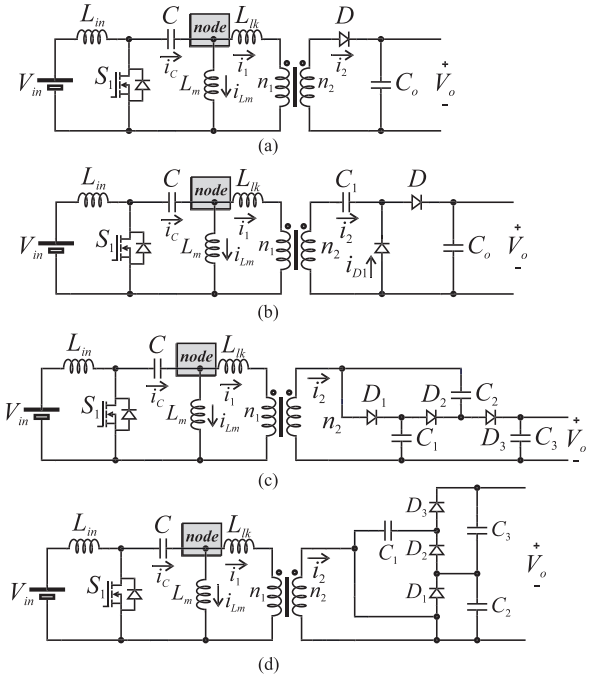


Fig. 5. Isolated SEPIC: (a) classical; (b) with Greinacher cell; (c) with Dickson cell; (d) with Ladder cell.

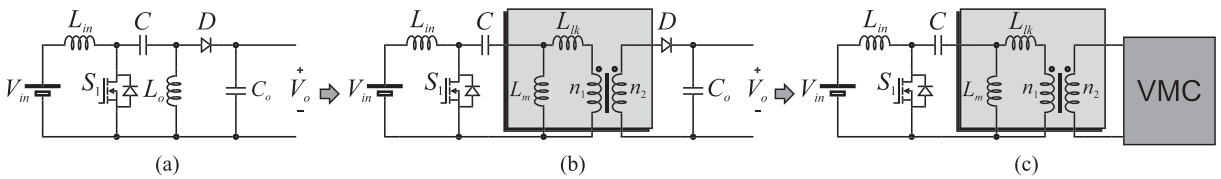


Fig. 3. Isolated SEPIC derivation: (a) Classic SEPIC converter; (b) Isolated SEPIC using cantilever model; (c) Isolated SEPIC with VMC on secondary side.

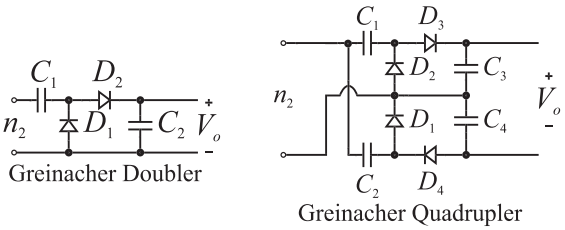


Fig. 6. Greinacher voltage multiplier cells used on secondary.

**TABLE I**
**Voltage and Static Gain of Cells and Converters**

| Cell | Voltage Gain | Topology | Static Gain |
|---|---|---|---|
| - | - | SEPIC | $D/(1\text{-}D)$ |
| - | - | iSEPIC | $nD/(1\text{-}D)$ |
| Greinacher VD | $1/D$ | VDiSEPIC | $n/(1\text{-}D)$ |
| Greinacher VQ | $2/D$ | VQiSEPIC | $2n/(1\text{-}D)$ |

capacitor, magnetizing current, $i_{Lm}$, has no dc component only on iSEPIC with VD cell. The main advantage of this feature is the use of transformer instead of coupled inductor. It is important to highlight that this cell can be cascaded, as shown in Figure 6, obtaining a voltage quadrupler (VQ), increasing components but also increasing the static gain, which reduces turn ratio of transformer. Table I summarizes the voltage gain of cells and the static gain of converters obtained with the insertion of these VMCs.

In Figure 7 the voltage gains of three converters are compared, in order to analyze the static gain using low values of turn ratio, equal to one and three, respectively. In comparison with VDiSEPIC, VQiSEPIC has more components, however, its static gain is higher, allowing to design a transformer with smaller turns ratio and, besides that, the voltage stress across diodes and secondary capacitors are smaller [19]. Therefore, Greinacher VQ cell applied on secondary of iSEPIC increases converter static gain and efficiency while reduces volume and cost. The detailed analysis of the converter is covered in next section.

## III. THEORETICAL ANALYSIS OF CONVERTER

The circuit of isolated SEPIC with VQ Greinacher cell (VQiSEPIC) is shown in Figure 8. In order to evaluate the theoretical performance of this converter, the following features are approached in this section: principle of operation with detailed analysis of resonant stage, voltage gain derivation, voltage stress, current stress, and analysis of winding transformer capacitance effects.

### *A. Principle of Operation*

In order to simplify the steady-state analysis, the following assumptions are made:

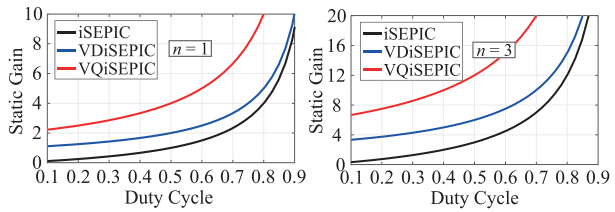


Fig. 7. Voltage gain of converters with and without VMCs on secondary side.

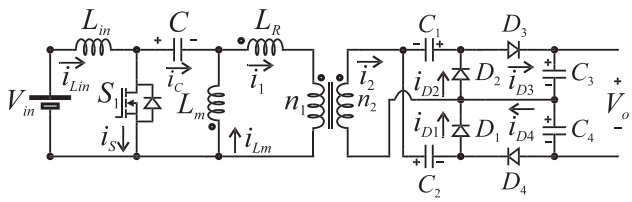

Fig. 8. Topology circuit of VQiSEPIC.

1) All power devices are ideal;
2) The magnetizing inductor, $L_m$, is taken into account on the analysis for higher accuracy, however, using a transformer with high quality material and good design, its impact is small, once its inductance is much higher than leakage inductance, $L_{lk}$;
3) Output voltage is constant, therefore, capacitors $C_3$ and $C_4$ are not taken into account on the analysis;

The converter has three different resonant operation modes, according to resonant period ($T_r$), switching period ($T_s$) and duty cycle. This can be better understood with Figure 9, where these modes are presented. The best option is the first mode, nearly to second mode, where total switching losses are smaller, since that ZCS condition is obtained in all diodes and the value of switch current on turn-off transition is smaller than in third mode. This will receive more attention during the description of operation stage II and in experimental results. Figure 10 shows the key waveforms of the converter in one switching period, in continuous-conduction-mode (CCM). It is important to mention that these waveforms are obtained for operation below resonance frequency. The converter has four operation stages in one switching period, as shown in Figure 11. The converter operation is given as follows:

*Stage* I ($t_0 - t_1$): This stage begins when switch $S_1$ is turned on, and the primary current $i_1$ begins its linear decreasing, as well as current $i_2$, while switch current, $i_s$, slowly increases also linearly. This results in a quasi-ZCS turn on of the switch. This stage ends when current $i_1$ reaches 0 A and diodes $D_1$ and $D_3$ are turned off under ZCS condition. The duration of this stage is considerably smaller than stage II and, because of this, voltages across capacitors are constant on this stage.

*Stage* II ($t_1 - t_2$): This stage begins when current $i_1$ changes its direction, so diodes $D_2$ and $D_4$ are turned on. At this instant, a resonance occurs, hence currents and voltages are sinusoidal, charging the capacitor $C_1$ and discharging $C$ and $C_2$. Voltage across $L_{in}$ still being equal to $V_{in}$, and voltage across $L_m$ is equal to $v_C$, so, both currents are increasing

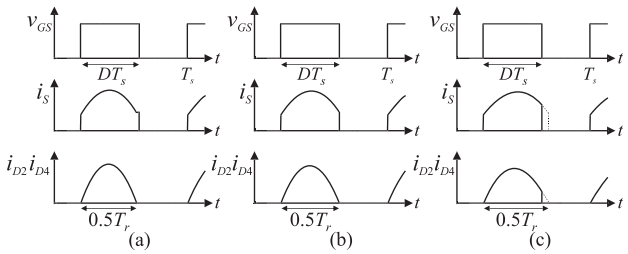


Fig. 9. Converter operation according to variation of resonance: (a) below resonance operation – first mode: $DT_s > 0.5T_r$; (b) exactly resonance operation – second mode: $DT_s = 0.5T_r$; (c) above resonance operation – third mode: $DT_s < 0.5T_r$.

linearly. To analyse this resonance, it is necessary to obtain

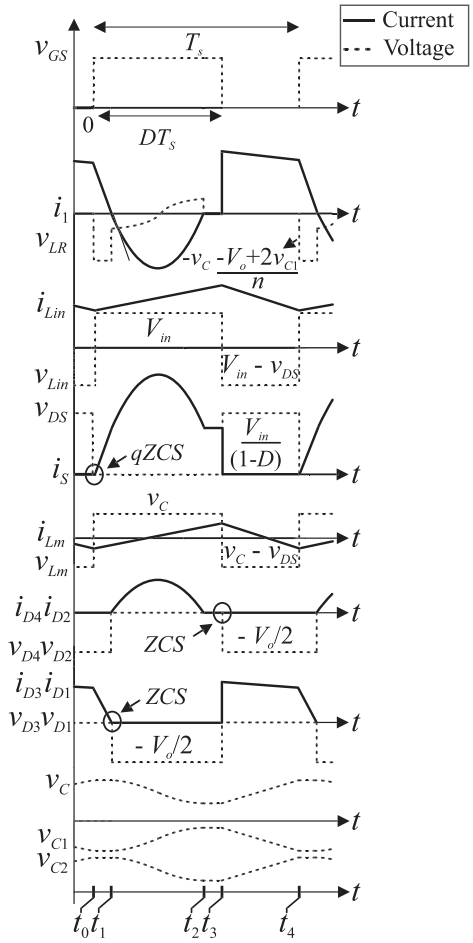


Fig. 10. Key waveforms of VQiSEPIC in CCM.

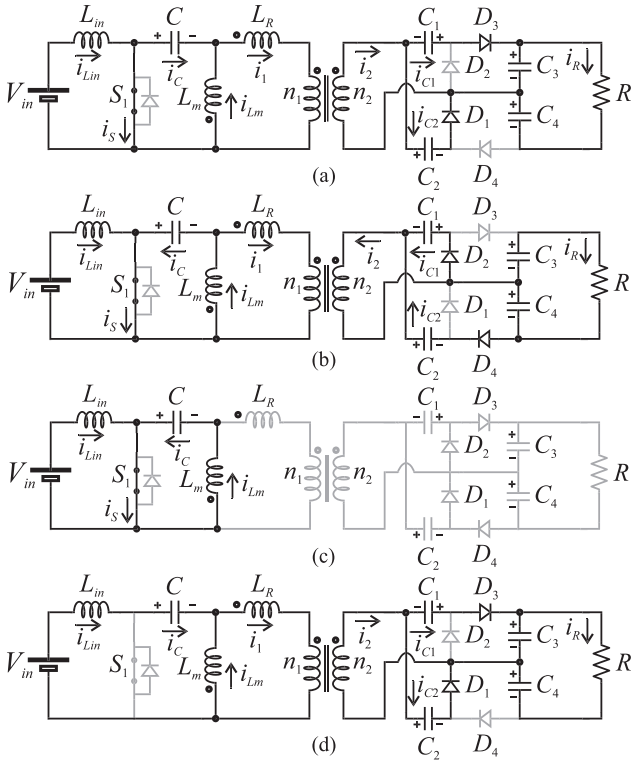


Fig. 11. Current flow path in four stages during one switching period in CCM operation: (a) stage I; (b) stage II; (c) stage III; (d) stage IV.

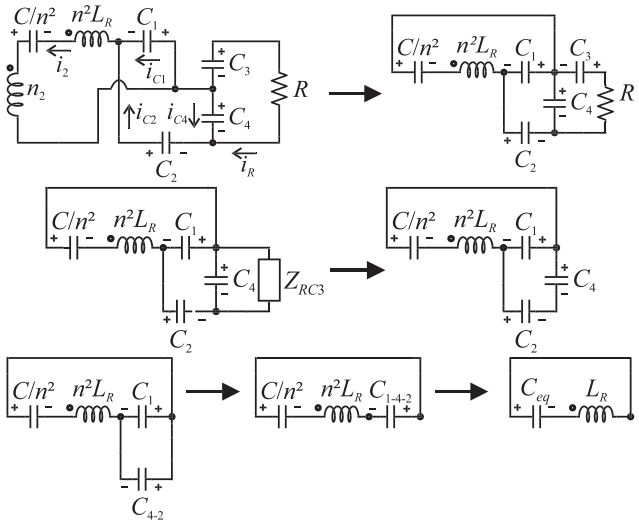


Fig. 12. Steps to obtain equivalent resonant circuit of Stage II.

the equivalent circuit for this stage, shown in Figure 11.

In Figure 12, inductance $L_R$ is referred to secondary multiplying its inductance by square of turn ratio, $n^2$, and $C$ is referred to secondary dividing its capacitance by $n^2$. Impedance $Z_{RC3}$ can be approximated by resistance $R$. The parallel association with $C_4$ can be approximated by the capacitive impedance of $C_4$. So, following the steps shown in Figure 11, the equivalent capacitance, $C_{eq}$, resonance frequency, $f_r$, and resonant impedance, $Z_r$, are given by

$$C_{eq} = \frac{\frac{C}{n^2}\left(C_4C_2 + C_4C_1 + C_2C_1\right)}{C_4C_2 + C_4C_1 + C_2C_1 + \frac{C}{n^2}C_4 + \frac{C}{n^2}C_2}. \quad (1)$$

$$f_r = \frac{1}{2\pi\sqrt{C_{eq}n^2L_R}}; \quad Z_r = \sqrt{\frac{n^2L_R}{C_{eq}}}. \quad (2)$$

Hence, as mentioned before, there are three possibilities of operation regarding to resonant period, switching period and duty cycle. The best choice are values of $T_r$, $T_s$ and $D$ that make converter operates in first mode, near to second mode. In this case, ZCS condition is guaranteed to $D_2$ and $D_4$, besides $D_1$ and $D_3$, that also have ZCS regardless of operation mode. Besides that, root mean square (RMS) and peak value of $i_s$, $i_{D2}$ and $i_{D4}$ are considerable smaller than in fist operation mode far away from second mode. Finally, the main problems of third mode are the loss of ZCS on $D_2$ and $D_4$ and higher switch current on its turn-off transition, increasing the converter switching losses.

*Stage* III ($t_2 - t_3$): This stage begins when switch is still on, but there is no current left on transformer and diodes are off, so, voltages $v_{C1}$ and $v_{C2}$ are constant, equal to the value at the end of stage II. Once the duration of this stage is considerable smaller than previous stage, and $C$ is in series with $L_m$, its voltage, $v_C$, also can be considered constant. This stage ends when $S_1$ is turned off, with losses, without soft-switching. Similar to stage I, this stage is very small and it happens in first and second modes of operation, but not in third.

*Stage* IV ($t_3 - t_4$): This stage begins when switch is turned off and diodes $D_1$ and $D_3$ are turned on, and there is current flux on transformer. Differently from stage II, this one occurs without resonance, and, consequently, currents and voltages are not sinusoidal, charging capacitors $C$ and $C_2$ and discharging $C_1$. During this stage, the voltage across $L_{in}$ is the difference between $V_{in}$ and $V_{DS}$, resulting in a linear decreasing of $i_{Lin}$, while voltage across $L_m$ is the difference between $v_C$ and $V_{DS}$, also resulting in a linear decreasing of $i_{Lm}$.

*B. Voltage and Current Stress*

The voltage stress over the switch is given by

$$V_{DS} = \frac{V_{in}}{1-D}. \tag{3}$$

For all diodes, the voltage stresses are given by

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = -\frac{V_o}{2}. \tag{4}$$

It can be seen that even with the increase in static gain, voltage stress on switch is the same of classical iSEPIC, while voltage stress on diodes is smaller compared to classical isolated and to VDiSEPIC, where voltage stress across diodes are equal to output voltage [20].

Average voltage over capacitors is given by

$$V_{C1} = nV_{in};\ V_{C2} = \frac{nDV_{in}}{1-D};\ V_{C3} = V_{C4} = \frac{nV_{in}}{1-D}. \tag{5}$$

In comparison with the VDiSEPIC, voltage over $C_1$ is equal, however, in VQiSEPIC the output voltage is equally divided over $C_3$ and $C_4$. It is important to highlight that average current through diodes, which directly impacts on conduction loss, is the same for both converters and is equal to load current, $i_R$. Average voltage over primary capacitor, $C$, is equal for all aforementioned converters.

As to RMS current values on diodes, it can be used the theory of general piecewise waveform, where a periodic waveform, composed of $N$ piecewise segments has a RMS value of

$$\text{RMS} = \sqrt{\sum_{k=1}^{N} D_k u_k}, \tag{6}$$

where $D_k$ is the duty cycle of segment $k$, and $u_k$ is the contribution of segment $k$. The contribution depends on the shape of the segment.

According to [21], $i_{D1}$ and $i_{D3}$ have a trapezoidal segment, while $i_{D2}$ and $i_{D4}$ have a sinusoidal segment. From analysis of operation stages, it can be affirmed that $i_{D2}$ and $i_{D4}$ are equal to half of $i_1$ referred to secondary in stage II. In the same way, $i_{D1}$ and $i_{D3}$ are equal to half of $i_{Lin}$ referred to secondary in stage IV. The portion of $i_{D1}$ and $i_{D3}$ during the stage I is neglected, since the duration of this stage is considerably smaller than the duration of stage IV and, therefore, it does not affect the RMS current evaluation. $D_k$ of segment $u_k$ of $i_{D2}$ and $i_{D4}$ is equal to $0.5T_r/T_s$, resulting in a RMS equation given by

$$i_{D2(rms)} = i_{D4(rms)} = \frac{\sqrt{\frac{1}{2} i^2_{1(pk)} \frac{0.5T_r}{T_s}}}{2n}, \tag{7}$$

where $i_{1(pk)}$ is equal to

$$i_{1(\text{pk})} = n\sqrt{\frac{C_{eq}}{n^2 L_R}}(v_{Ceq}(0)). \tag{8}$$

$D_k$ of segment $u_k$ of $i_{D1}$ and $i_{D3}$ is equal to (1-$D$), resulting in a RMS equation given by

$$i_{D1(rms)} = i_{D3(rms)} = \frac{\sqrt{\frac{1}{3}\begin{pmatrix} i^2_{Lin(\text{min})} + \dots \\ +i_{Lin(\text{min})} i_{Lin(\text{max})} + .. \\ +i^2_{Lin(\text{max})} \end{pmatrix}(1-D)}}{2n}. \tag{9}$$

Following the same methodology, the RMS equation of $i_{Lin}$ is given by

$$i_{Lin(\text{rms})} = \sqrt{\left(\frac{1}{3}\left(i_{Lin}{}^2{}_{(\text{mín})} + i_{Lin(\text{mín})} i_{Lin(\text{máx})} + i_{Lin}{}^2{}_{(\text{máx})}\right)\right)}. \tag{10}$$

The RMS equation of $i_1$ is given by

$$i_{1(\text{rms})} = \sqrt{\left(\frac{i_1{}^2{}_{(\text{pk})}}{4}\frac{T_r}{T_s}\right) + \left(\frac{1}{3}\left(i_1{}^2{}_{(mín)} + i_{1(mín)} i_{1(máx)} + i_1{}^2{}_{(máx)}\right)(1-D)\right)}. \tag{11}$$

Where

$$i_{1(\text{máx})} = \underbrace{\left(I_{in} + \frac{DT_s V_{in}}{2L_{in}}\right)}_{i_{Lin(\text{máx})}} + \underbrace{\frac{DT_s V_{in}}{2L_m}}_{i_{Lm(\text{máx})}} \tag{12}$$

$$i_{1(\text{mín})} = \underbrace{\left(I_{in} - \frac{DT_s V_{in}}{2L_{in}}\right)}_{i_{Lin(\text{min})}} - \underbrace{\frac{DT_s V_{in}}{2L_m}}_{i_{Lm(\text{min})}}. \tag{13}$$

Finally, as to switch RMS value, it is necessary to use the classical equation of RMS variable, once $i_s$ waveform does not have a defined equation, given by

$$i_{s(rms)} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_s{}^2 dt} = \sqrt{\frac{1}{T_s}\begin{pmatrix} \left(\int_0^{T_r/2} \left(-i_1 + i_{Lin}\right)^2 dt\right) + .. \\ +\left(\int_{T_r/2}^{DT_s} i_{Lin}{}^2 dt\right) \end{pmatrix}}. \tag{14}$$

The solution of this equation will give

$$i_{s(rms)} = \sqrt{\frac{1}{T_s}\left(a - \frac{\left(\frac{b+c}{3}\right)}{L_{in}{}^2} + d + e - f - \left(\frac{g+h}{L_{in}}\right)\right)}, \tag{15}$$

where the complete definition of all these parameters can be found in [20], since the primary of both converters are the same. It is important to mention that the average current of all diodes is equal to the output current, $I_o$.

*C. Winding Transformer Capacitance*

Cantilever model can be used to represent a transformer, however, stray capacitances are not taken into account. A real transformer has windings self-capacitances and interwinding capacitances. Self-capacitances can be represented on primary side by a single equivalent capacitance, similar to what is done with leakage and magnetizing inductances [21], and has an important impact

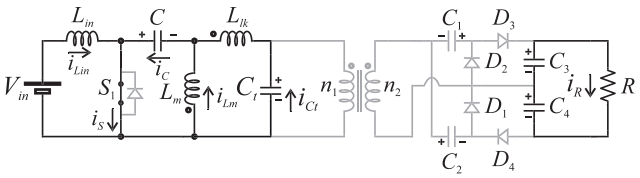


Fig. 13. Discharge of capacitance $C_t$.

on converter operation, specifically affecting the resonance of stage II. Interwinding capacitance couples primary and secondary voltages and gives an indication of how much common mode noise is allowed, but can be disregarded on four stages of converter's operation.

Therefore, referring self-capacitance of secondary to primary and disregarding interwinding capacitance in this case, results in an additional stage, shown in Figure 14, when $i_1$ reaches 0 A, starting the discharge of equivalent capacitance, $C_t$. Ideally, disregarding voltage ripple of capacitors, during this short period, voltage across $C_t$ is changed from $V_o/n - V_{in}$ to $V_{in}$, resulting in a linear current. The impact of $C_t$ is shown in Figure 14.a, where waveforms of $i_{Ct}$, $i_1$, $i_{C1}$, $i_{C2}$, $i_{C3}$, $i_{C4}$, $i_{D1}$ and $i_{D2}$ are shown, giving a zoom between beginning and the end of $C_t$ discharge. In Figure 14.b, key current waveforms are shown for a switching period. It is important to highlight that in ideal conditions, $i_{D2}$ and $i_{D4}$ are equal, as well as $i_{D3}$ and $i_{D1}$.

It can be seen from Figure 14.a that during the discharge of $C_t$, all diodes are off, which means that there is no current flow through capacitors $C_1$ and $C_2$, so, capacitors $C_3$ and $C_4$ are in series with resistance load, $R$. It can be seen in waveforms of Figure 14.b that the main effects of $Ct$ discharge are the reduction of resonant period, once linear

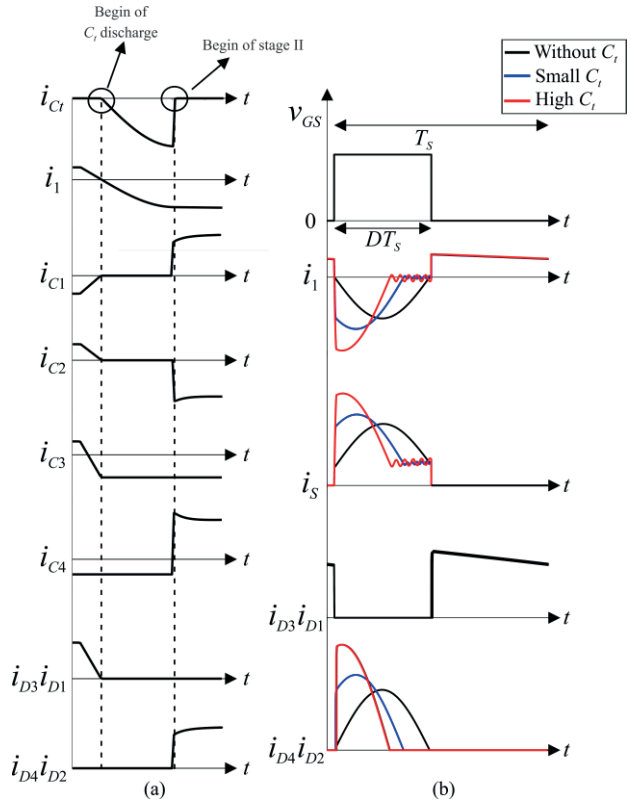


Fig. 14. Impact of $Ct$: (a) before the beginning of stage II; (b) in currents of converter's operation.

current cuts off part of original resonant period compared to when $C_t$ is disregarded, and the increase of peak value of $i_s$ and $i_{D2}$ and minimum value of $i_1$. These effects on resonant period and currents directly impact on converter efficiency, therefore, it is important that the converter operates below resonance, in first mode, according to Figure 9, near to second mode.

## IV. EXPERIMENTAL RESULTS

A 200 W prototype of the converter was built and tested to validate the proposed concept, using a switching frequency of 50 kHz. Main parameters of operation and component rating are listed in Table II. As can be seen in Table II, leakage inductance has a small value, while magnetizing inductance is considerable higher, as desirable. Tektronix Encore MD03000 oscilloscope and a Yokogawa WT1600 power meter were used to measure main parameters.

### *A. Experimental Results*

The input voltage was chosen due to voltage at maximum power point of a Canadian photovoltaic module, model CS5A-200M, for an irradiance of 1000 W/m², while output voltage is equal to 400 V, an usual value used in grid-tie inverters. Therefore, the static gain is 10.695. A duty cycle of 0.44 was chosen, keeping balance between efficiency, turn ratio and voltage stress across semiconductors, therefore $n$ has to be equal to three to obtain the specified output voltage.

The power switch device is IPP051N15N5, while MUR860 is selected for diodes. Leakage inductance of transformer is used as resonant inductor. Considering (2), the switching period and duty cycle, $C_{eq}$ and consequently $C_1$ and $C_2$ are obtained so that converter operates in first mode, below resonance operation, near to second mode, according to Figure 9. However, taking into account the effect of $C_t$, capacitance values must be higher, once linear current cuts off part of resonance, reducing its period. The solution is to test the converter using the same value of capacitance for $C_1$ and $C_2$, close to what was obtained with (2) and slowly increase this capacitance until converter is operating near to second mode.

Figure 15 shows waveforms of $v_{GS}$, $V_{in}$ and $V_o$, in order to confirm the obtained static gain. The measured value of $V_{in}$ is

**TABLE II**
**Main Parameters and Component Rating**

| Parameter/Component | Specification/Value |
|---|---|
| Input Voltage | 37.4 V |
| Duty Cycle | 0.44 |
| Output Voltage | 400 V |
| Switching Frequency | 50 kHz |
| Switch $S_1$ | IPP051N15N5 (150 V/120 A, 5.1 mΩ) |
| Diodes $D_1, D_2, D_3, D_4$ | MUR840 (400 V/8 A, $v_f$ = 0.8 V) |
| Transformer $L_{lk}$, $L_m$, $N_1$:$N_2$, Core DCR $N_1$, DCR $N_2$ | 400 nH, 1 mH, 8:24, 2xMMT520T30.20.10B [26] 4 mΩ (6xLitz wire), 40 mΩ (2xLitz wire) |
| Input Inductor $L_{in}$ | 210 µH/ 77777 [25]/ DCR: 20 mΩ (8x Litz Wire) |
| Input Capacitor $C$ | 4x10 µF/100 V Electrolytic ESK106M063AC3 (1 Ω) 3x3.3 µF/100 V film BFC246804335 (10 mΩ) |
| Resonant Capacitors $C_1$, $C_2$ | 1x820 nF/250 V film B32594 (8 mΩ) 2x2.2 µF/250 V film B32594 (14 mΩ) |
| Output Capacitors $C_3, C_4$ | 100 µF/250 V Electrolytic B43851K2107M000 (250 mΩ) |

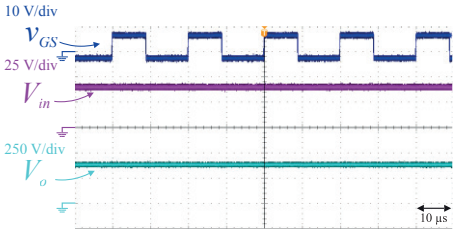


Fig. 15. Experimental waveforms of $v_{GS}$, $V_{in}$ and $V_o$.

37.4 V, while output voltage is 405.5 V. Therefore, the static gain is equal to 10.84, while theoretical is 10.81, a very close value.

Figure 16 shows main waveforms of switch at full-load condition with a zoom on turn-on transition. $i_S$ waveform shows that converter is operating near to second mode, since half of resonant period is lower than the period that switch is on, and the effect of $C_t$ can be seen, being in agreement with theoretical analysis and waveforms of Figure 13. Furthermore, the zoom on turn-on transition shows that turn-on switching losses are negligible. Finally, it can be seen there is a voltage spike across switch due to leakage inductance of transformer, although, this is not a concern, once that maximum voltage across switch is 91 V, while maximum voltage of switch $S1$ is 150 V and there is no need to use an additional snubber circuit. This happens because leakage inductance has a small value, a positive characteristic of well-designed transformers using nanocrystalline core.

Experimental waveforms of $v_C$, $v_{C1}$ and $v_{C2}$ are shown in

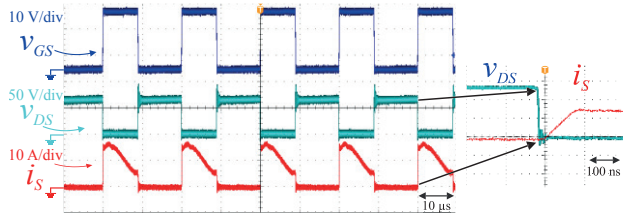


Fig. 16. Experimental waveforms of switch $S_1$ with zoom on turn-on.

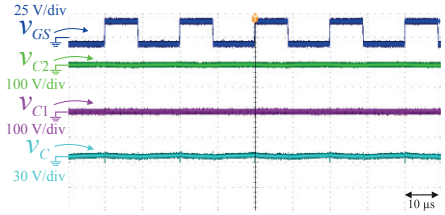


Fig. 17. Experimental waveforms of voltages over $C$, $C_1$ and $C_2$.

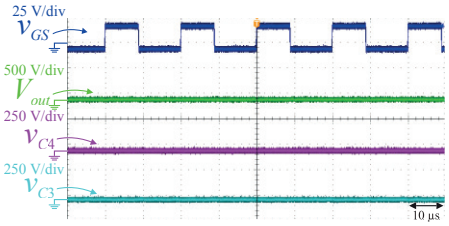


Fig. 18. Experimental waveforms of output voltage and voltages over $C_3$ and $C_4$.

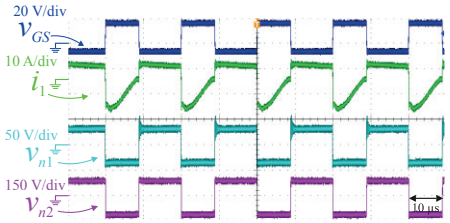


Fig. 19. Experimental waveforms of transformer.

Figure 17, while $v_{C3}$, $v_{C4}$ and $V_{out}$ are shown in Figure 18. The measured average voltage over $C1$ is equal to 110 V, while theoretical value, according to (5), is 112.2 V. The measured average voltage over $C_2$ is 94 V, while theoretical value, according to (5), is 91.8 V, therefore, in both cases the error is less than 3%, which is acceptable, considering imprecisions on measurement and voltage drops on other elements that are not considered in theoretical analysis. Regarding to average voltage over $C_3$ and $C_4$, measured value is practically the same for both and it is equal to 202.5 V, confirming that output voltage is equally divided over these capacitors.

Figure 19 shows main waveforms of transformer. The waveform $i_1$ confirms the converter operation in first mode, besides showing the effect of $C_t$ discharge after its value reaches 0 A. As well as voltage across the switch, there is a voltage spike over primary winding ($v_{n1}$), however, it is not a concern since voltage peak is not high. Differently, the voltage over secondary winding ($v_{n2}$) is clamped because of capacitors, without spikes.

This effect also occurs on diodes voltage, as shown in Figure 20, where secondary current and voltages over $D_2$ and $D_4$ are shown. As can be seen in Figure 19, both diodes conduce the sinusoidal current on secondary while switch is on. The operation in first mode guarantee the ZCS condition for both diodes. In Figure 21, the secondary current and voltages over $D_1$ and $D_3$ are shown, with a zoom on turn-off

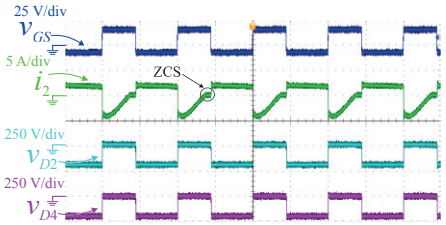


Fig. 20. Experimental waveforms of diodes $D_2$ and $D_4$.

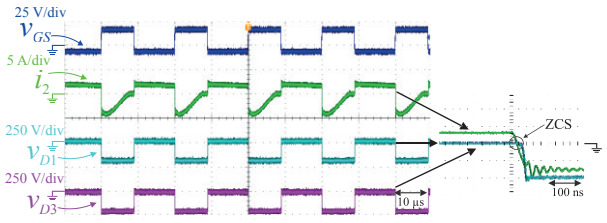


Fig. 21. Experimental waveforms of diodes $D_1$ and $D_3$ with zoom on turn-off.

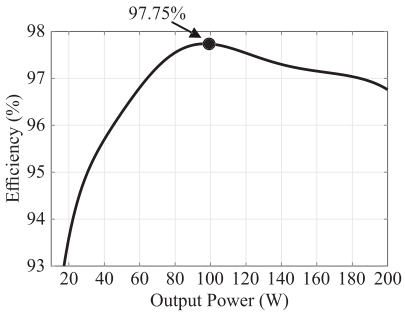

Fig. 22. Measured efficiency of the converter.

transition, in order to present the linear decrease of $i_2$ when switch is turned off, besides the effect of $C_t$ discharge when $i_2$ reaches 0 A. Moreover, it can be seen that both diodes conduce the trapezoidal current on secondary while switch is off.

*B. Efficiency Results and Loss Distribution*

Finally, Figure 22 presents the converter efficiency for different output power levels. The maximum measured efficiency is 97.75% at 100 W, while the full-load efficiency is 96.755%. The European weighted efficiency is 96.77%, while Californian Energy commission weighted is 97.046%. %. It is important to highlight that the converter efficiency is higher than 96.5% for most part of the output power range. To understand the efficiency behavior, the losses estimation is evaluated. In this sense, the losses of each component were calculated. In relation to the switch, the losses can be calculated by

$$P_s = R_{DS(on)} i_{s(RMS)}{}^2 + 0.5 f_s \left[ \left( V_{DS} i_{s(t3)} \left( t_{off} + t_{on} \right) V_{DS}{}^2 C_{oss} \right) \right]. \quad (16)$$

Where $R_{DS(on)}$ is the static drain-to-source ON-resistance, $i_{s(RMS)}$ is the rms current of switch, $f_s$ is the switching frequency, $V_{DS}$ is the maximum voltage stress over the switch, $i_{s(t3)}$ is the switch current at instant $t_3$, $t_{off}$ and $t_{on}$ are the switching time for turn-on and turn-off and $C_{oss}$ is the output capacitance provided by manufacturer [23]. An important issue to highlight in this case: the switch current on turn-off ($t_3$) is equal to the maximum value of $i_{Lin}$. This value is obtained considering $I_{in}$ and the current ripple $\Delta i_{Lin}$. Since there is a qZCS condition, the $t_{on}$ is disregarded on calculation. The losses of diodes are given by

$$P_D = \sum_{x=1}^{4} I_{Dx(avg)} v_f . \quad (17)$$

The $I_{D(avg)}$ is the average current of each diode and $v_f$ is the forward voltage given by the manufacture datasheet [24]. Since both diodes achieve ZCS condition for turn-off transition, these losses can be neglected.

The inductor losses can be calculated by

$$P_{Lin} = DCR_{Lin} i_{Lin(RMS)}{}^2 + P_L A_e l_e . \quad (18)$$

Where $DCR_{Lin}$ is the copper wire resistance and $i_{Lin(RMS)}$ is the RMS current of input inductor. The parameter $P_L$ is the core loss density, defined by $P_L = aB_{pk}{}^b f_s{}^c$, where $a$, $b$ and $c$ are constants given in the datasheet and $B_{pk}$ is the AC magnetic flux density. The value of $P_L$ also can be determined from the chart provided by the manufacture core information [25]. $A_e$ is the transversal core area and $l_e$ is the core medium path length. Both parameters are also available in [25].

The transformer losses are the sum of copper losses and core losses and can be calculated by

$$P_T = DCR_{n1} i_{1(RMS)}{}^2 + DCR_{n2} i_{2(RMS)}{}^2 + P_e + P_h . \quad (19)$$

Where $DCR_{n1}$ and $DCR_{n2}$ are the copper wire resistance of primary and secondary coil, respectively, $i_{1(RMS)}$ and $i_{2(RMS)}$ are the RMS current of primary and secondary coil, respectively. $P_e$ is the eddy current loss and $P_h$ is the hysteresis loss. Usually, the core manufacture datasheet provides a graph relating the power loss density versus peak AC flux density. In this case, the local supplier gives an estimation of core losses based on the peak AC flux density of 0.51 T, considering the graph of power loss density presented in [26].

The capacitor losses are given by

$$P_C = \sum_{x=1}^{5} ESRI_{C(RMS)}{}^2 . \quad (20)$$

In this case, since the input capacitor is composed by some capacitors connected in parallel, including film capacitors, the ESR is significantly reduced so that the losses associated to this element are small. The same occurs for resonant capacitor, since RMS current on secondary is smaller than on primary and only film capacitors were used. Therefore, most of capacitor losses are due to the output capacitor.

In order to validate the currents of converter components, a digital simulation was performed in PSIM®. After that, using all the losses equations and MATLAB software, the losses and efficiency of converter were calculated for full-load condition. The result of the loss distribution is shown in Figure 23.

It is important to highlight that the use of transformer associated to a cell on secondary side enable to choose a switch with a low value of $R_{DS(on)}$, which reduces the conduction losses, while the qZCS reduces the switching losses. The ZCS condition for both diodes associated to a low average current results in less than 500 W of losses for each diode. It can be seen in Figure xx that the loss distribution is more balanced, since the transformer losses are close to the sum of losses on diodes. It is important to highlight that the efficiency curve is very attractive for this converter, which is confirmed by the higher values of the weighted efficiencies. For the full-load condition, the obtained theoretical efficiency is equal to 96.95%, while the experimental efficiency is equal to 96.775%, therefore, there

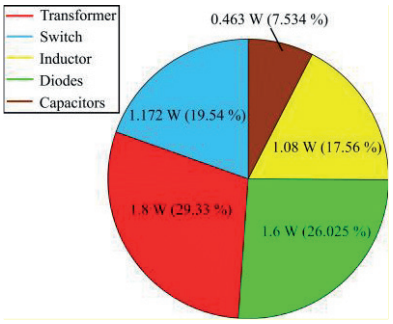

Fig. 23. Efficiency evaluation: Loss distribution.

**TABLE III**
**Comparison Among Proposed Converter with Other Converters Presented in the Literature**

| Converter | Static Gain | Specification | Voltage over main switch | Maximum Efficiency | Full-load efficiency | Isolated |
|---|---|---|---|---|---|---|
| VQiSEPIC | $\frac{2n}{1-D}$ | $f_s = 50$ kHz<br>$P_o = 200$ W<br>$V_{in} = 37.4$ V<br>$V_o = 400$ V | $\frac{V_{in}}{1-D} = \frac{V_o}{2n}$ | 97.75% | 96.75% | Yes |
| [27] | $2n\frac{1+D}{1-2D}$ | $f_s = 50$ kHz<br>$P_o = 300$ W<br>$V_{in} = 25$ V<br>$V_o = 400$ V | $\frac{V_{in}}{1-2D} = \frac{V_o}{2n(1+D)}$ | 95% | 93.3% | Yes |
| [28 ] | $n\frac{1+D}{1-2D}$ | $f_s = 50$ kHz<br>$P_o = 300$ W<br>$V_{in} = 25$ V<br>$V_o = 400$ V | $\frac{V_{in}}{1-2D} = \frac{V_o}{n(1+D)}$ | 93.5% | 92.5% | Yes |
| [29] | $\frac{nD}{1-D}$ | $f_s = 50$ kHz<br>$P_o = 100$ W<br>$V_{in} = 48$ V<br>$V_o = 200$ V | $\frac{V_{in}}{1-D} = \frac{V_o}{nD}$ | 95.8% | 93.8% | Yes |
| [30] | $\frac{1+3D}{1-D}$ | $f_s = 40$ kHz<br>$P_o = 200$ W<br>$V_{in} = 20$ V<br>$V_o = 250$ V | $\frac{V_{in}}{1-D} = \frac{V_o}{1+3D}$ | 94.5% | 93% | No |
| [31] | $\frac{1+nD}{(1-D)}$ | $f_s = 60$ kHz<br>$P_o = 200$ W<br>$V_{in} = 42$ V<br>$V_o = 400$ V | $\frac{V_{in}}{1-D} = \frac{V_o}{(1+nD)}$ | 95% | 93.8% | No |
| [32] | $\frac{1+nD}{(1-D)^2}$ | $f_s = 40$ kHz<br>$P_o = 280$ W<br>$V_{in} = 24$-$40$ V<br>$V_o = 400$ V | $\frac{V_{in}}{(1-D)^2} = \frac{V_o}{1+nD}$ | 93.3% | 92.5% | No |

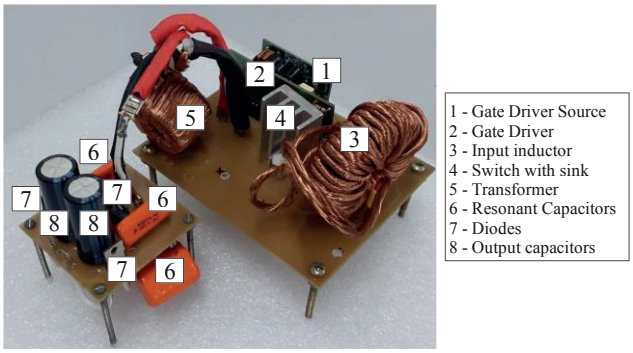

Fig. 24. Photograph of converter prototype.

is a small difference of 0.175%.

Finally, Table III shows a comparison among the presented converter with other converters presented in literature. To perform this, the switching frequency and input and output voltage levels have to be equal or at least has a close value, in order to be able to compare the efficiencies. In general, it can be seen that VQiSEPIC achieve a high static gain and, in most cases, the maximum and full-load efficiency are significantly higher than the other converters. Moreover, due to the low values of leakage inductance, the presented converter shows attractive results without the need of snubber circuits. The converter prototype is shown in Figure 24.

## V. CONCLUSIONS

In this paper, a high voltage gain single switch isolated dc-dc SEPIC converter with voltage quadrupler cell was proposed for primary stage of a MIC for photovoltaic applications. A detailed theoretical analysis, with emphasis on resonant stage, besides the influence of winding transformer capacitance, was performed. In addition, the use of a nanocrystalline core with a well-designed transformer results in a low leakage inductance, which enables the converter to operate without an additional snubber circuit, maintaining the safety of switch. Effects of transformer winding capacitance were investigated, including the impact on current waveforms of converter, which directly influences on resonant stage. Experimental results show the qZCS condition for power switch, besides the ZCS condition for diodes, reducing switching losses of the converter. Despite of the increase of component count in comparison with iSEPIC and VDiSEPIC, turn ratio and voltage over capacitors and diodes are smaller. Finally, maximum efficiency of 97.75% was obtained at 100 W, achieving a high voltage gain with high efficiency, as initially desired.

## ACKNOWLEDGEMENTS

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## BIOGRAPHIES

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